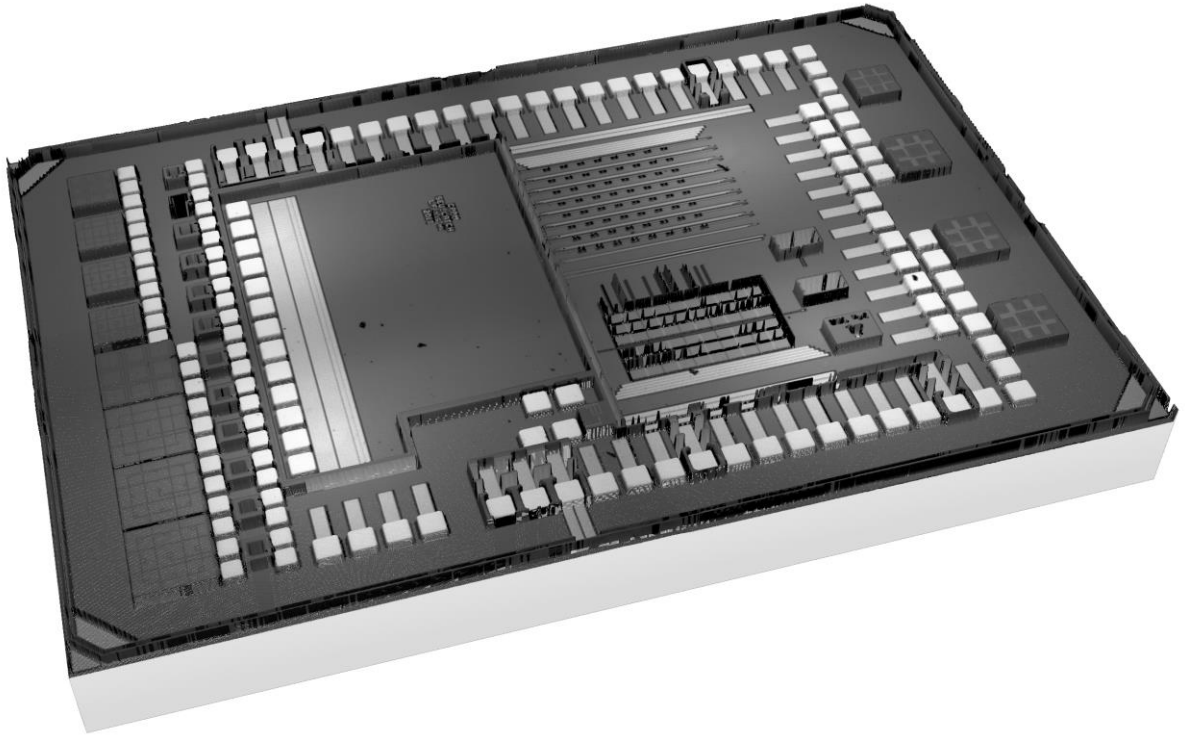

Digital vs Analog on Top

A few considerations...

- Priority 1 is timing.
  - In digital part: guaranteed with synthesis
  - In analog part: “guaranteed” with spice simulations
    - Can we simulate the whole design?
- The problem is the interconnect between matrix + EOCs

Design Flows

Analog on Top

- Fully supported by PDK
- Timing: Full SPICE simulation
  - Input: RC values of transistors
  - Time consuming for huge designs
    - Possible for 128 pixels?
- Strategy to follow: Assume ideal signals from EOCs + Use them as input for SPICE simulation (post-layout!) of the full DCOL
  - Real signals (input/output delay) hard to simulate

Digital on Top

- Hardly supported (Pads, … missing)
- Timing: Liberty files (.lib) -> pre-defined delay per cell (Transistor/ AND gate, …) depending on operation conditions + drive and load
  - Input: .lib files and constraints for ports
  - Meant for huge designs -> verify full chip within reasonable time
    - .lib for matrix needed (Liberate – Plugin for virtuoso)

In any case: Proper constraints needed for pins of the periphery, where no cell with a .lib is available

- Uncritical for bias- and asynchronous signals
- Critical for synchronous signals (mainly configuration: CK1, SHIFT_EN, LD[7:0], …)

Discussion Point

- Can EN_SFOUT_COL and EN_HB_COL be the same signals?
- TS overflow output?
- We need somebody for verify the digital logic

Outlook

- Write Documentation
- Some minor changes on Code missing (MUXing SER_OUT,… -> issues listed in gitlab)
- Cross-check waveforms for shift with Nissar (ongoing)

- Synthesis:
  - hdl and .lib loaded
  - Elaboration done
    - few warnings to be checked, shouldn’t be difficult
  - Currently writing constraints
    - Quite some problems with latches, … -> RTL needs to be re-written