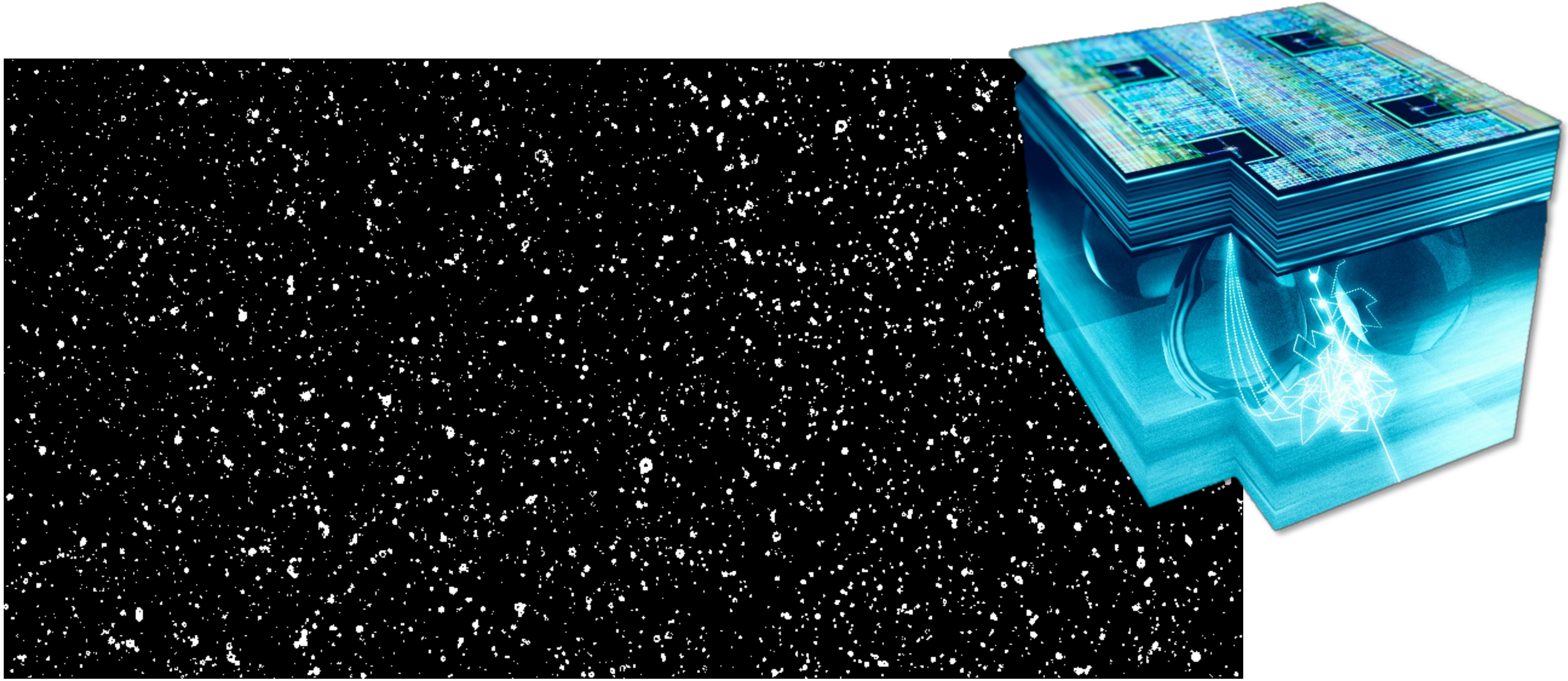
Development of pixel sensors for high energy physics in commercial CMOS technologies



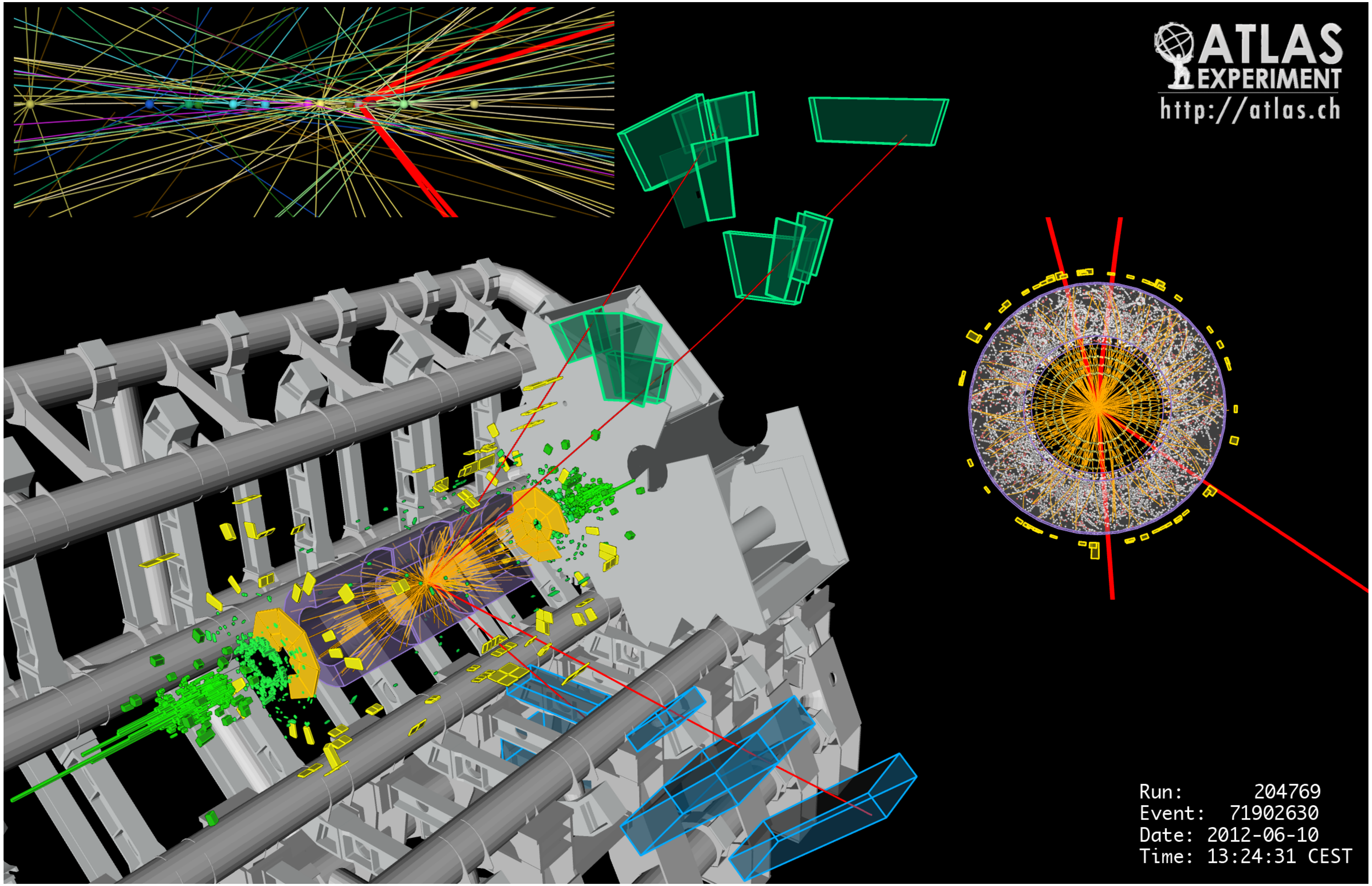
ALPIDE prototype: 200 MeV protons at PSI

W. Snoeys

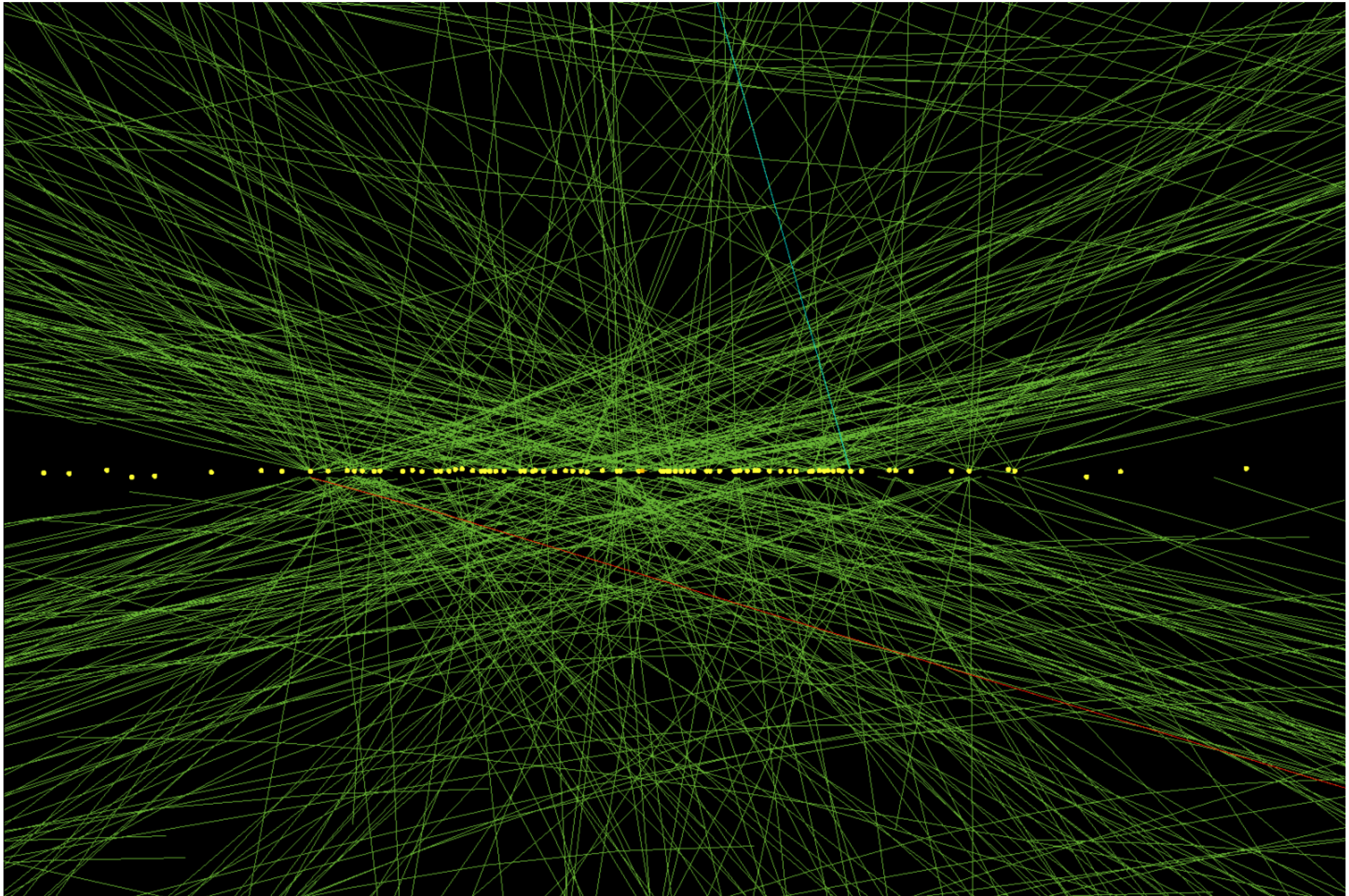
Geneva, Switzerland

RAPID2021, October 27th, 2021

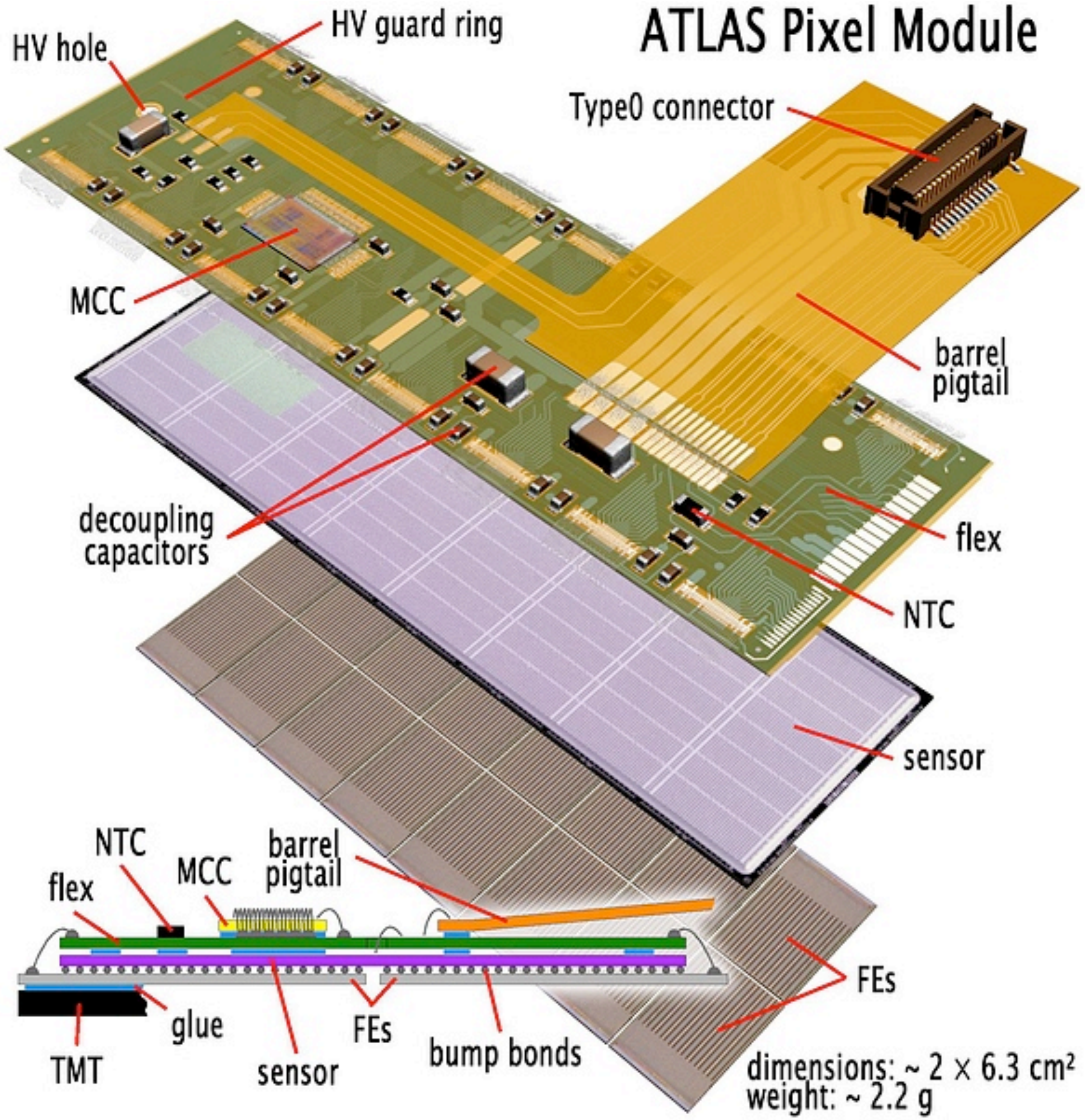
High energy physics: candidate Higgs event in ATLAS



In the center pixels to make sense of this:



ATLAS Presently installed pixel detector: readout

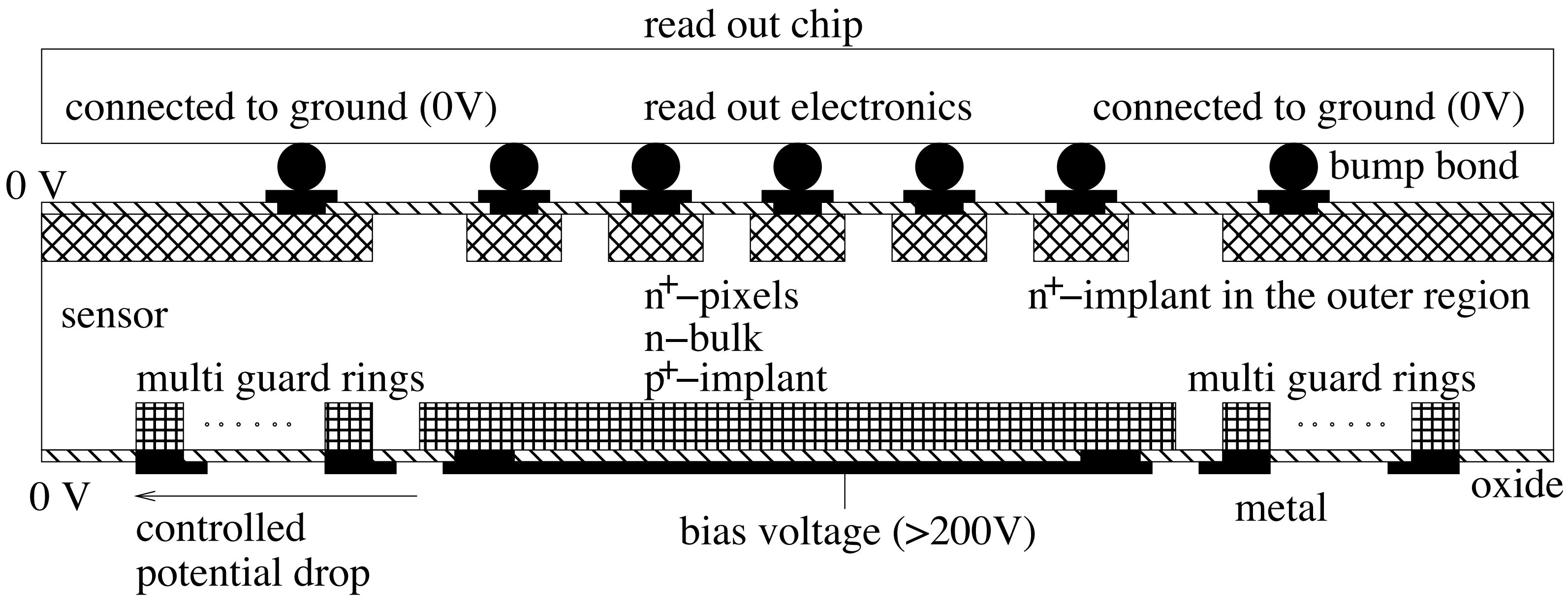


Courtesy D Dobos Ph. D. Thesis

2880 readout cells
of 50 x 400 μm²

16 chips
on the module

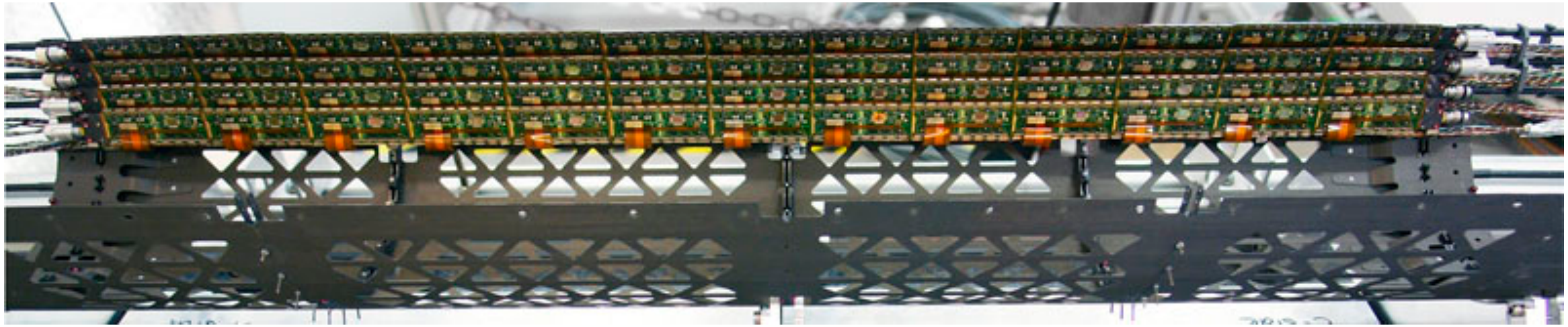
ATLAS Presently installed pixel detector: detector assembly



Courtesy T. Rohe, Ph. D. Thesis and
T. Rohe et al, NIM A 409 (1998) 224

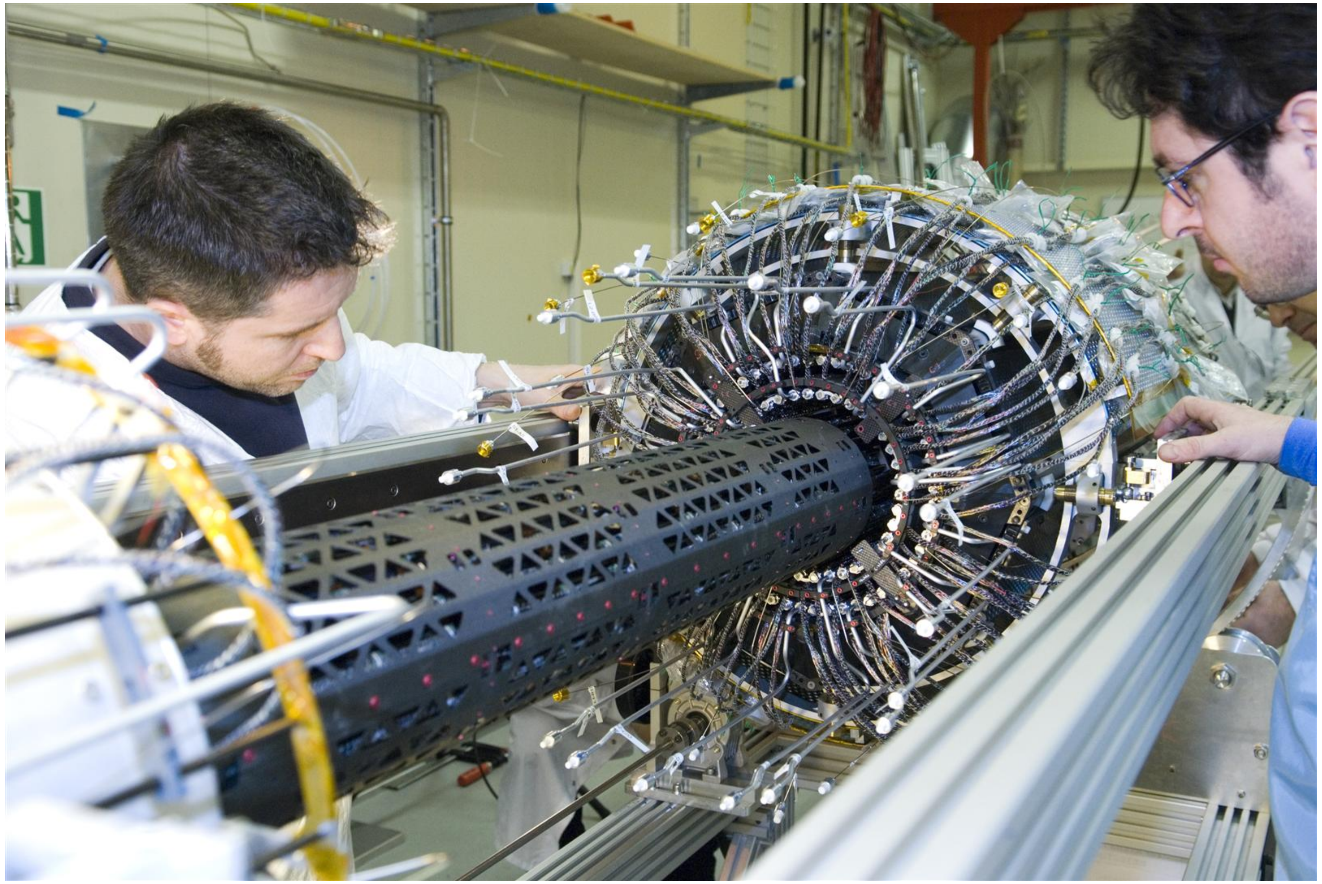
Junction on the back to remove high voltage from the front and reduce the probability for discharges
("N-on-n" pixels)

ATLAS Presently installed pixel detector: construction



Total area ~1.7 m^2

80M channels



RD53 design chips for ATLAS and CMS HL-LHC upgrades

RD53 Collaboration

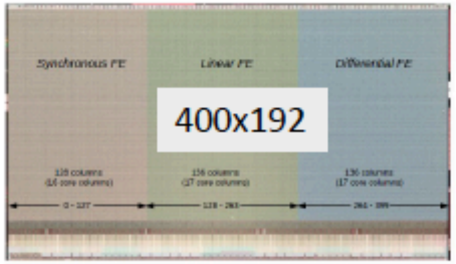
RD53 Collaboration is a joint effort between ATLAS and CMS established in 2013 to develop readout chips for the HL-LHC pixel detectors (24 Institutions from Europe and USA)

1. Characterization of chosen **65nm CMOS** technology in radiation environment
2. Design of a **rad-hard IP library** (Analog front-ends, DACs, ADCs, CDR/PLL, high-speed serializers, RX/TX, ShuntLDO, …)
3. Design and characterization of **half-size pixel chip demonstrator (RD53A)** with design variations
4. Design of pre-production (**RD53B**) and production (**RD53C**) pixel readout chips

   ATLAS and CMS chips are two instances of the same common design, having different size and Analog Front-End, according to specific requirements of the experiments

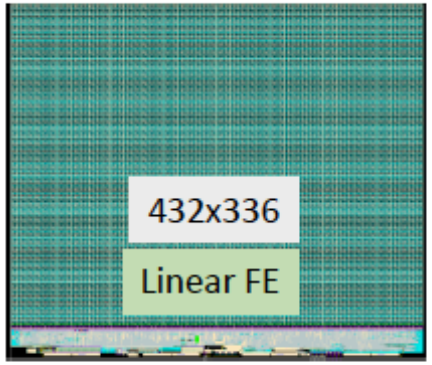
	ATLAS/CMS
Chip size	20x21mm^2/21.6x18.6mm^2
Pixel size	50x50 µm^2
Hit rate	3 GHz/cm^2
Trigger rate	1 MHz/750kHz
Trigger latency	12.5 us
Min. threshold	600 e-
Radiation tolerance	500 Mrad @-15C
Power	< 1W/cm^2

https://cds.cern.ch/record/2663161



RD53A
- submitted in August 2017
- Size: 20 x 11.5 mm2

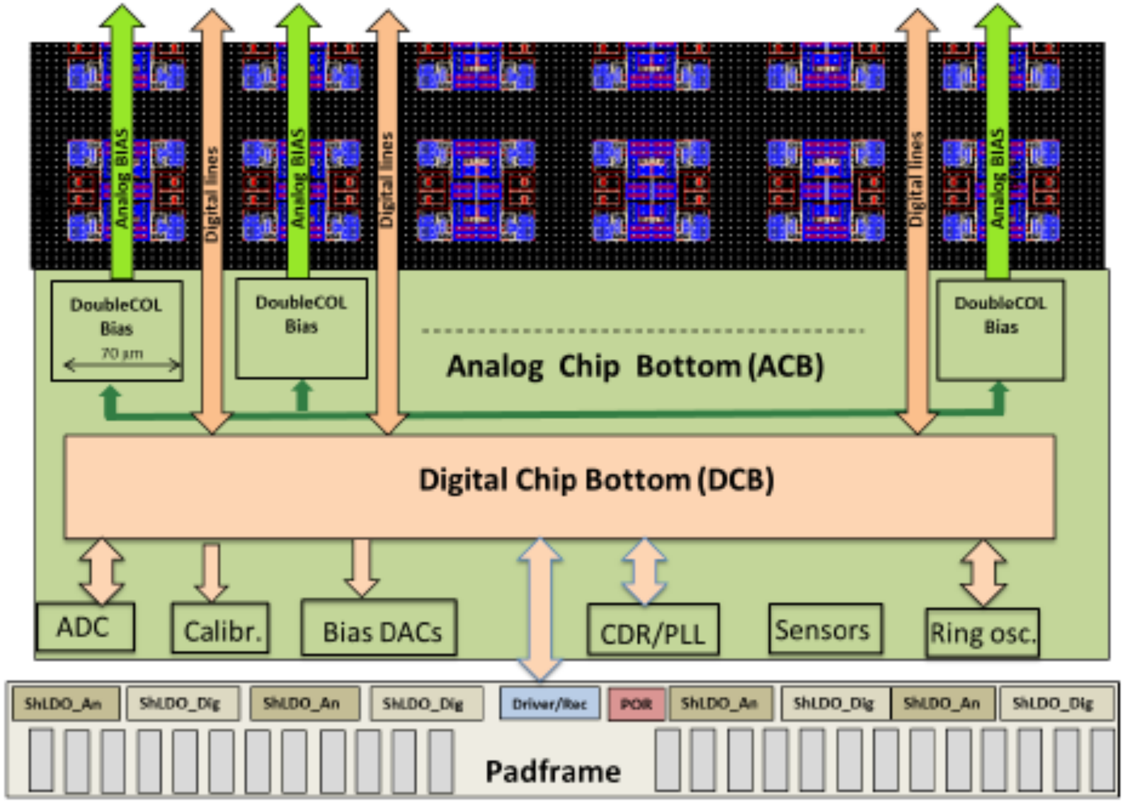
RD53B-ATLAS (ItkPix_V1)
- submitted in March 2020
- size: 20 mm x 21 mm



RD53B-CMS (CROC_V1)
- to be submitted in May 2021
- size: 21.6 mm x 18.6 mm

RD53C-ATLAS: Q1 2022
RD53C-CMS: Q2-Q3 2022

RD53 design chips for ATLAS and CMS HL-LHC upgrades



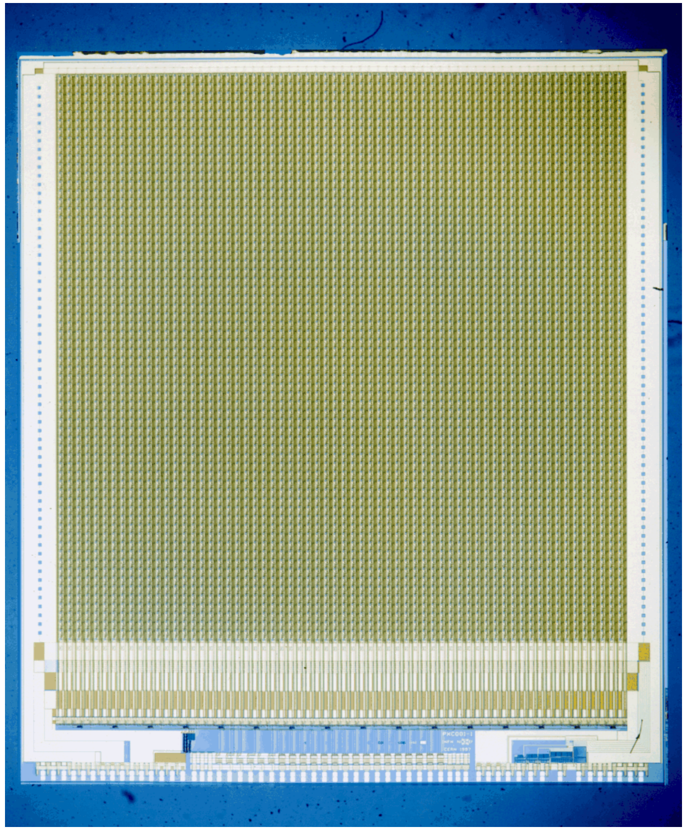
Analog islands in digital sea in the matrix

Significant effort in several areas:

- Architecture and front end
- Radiation tolerance (500 Mrad…)
- SEU mitigation through triplication
- Off-chip data transmission and clock recovery
- Serial powering shuntLDO (Karagounis et al)

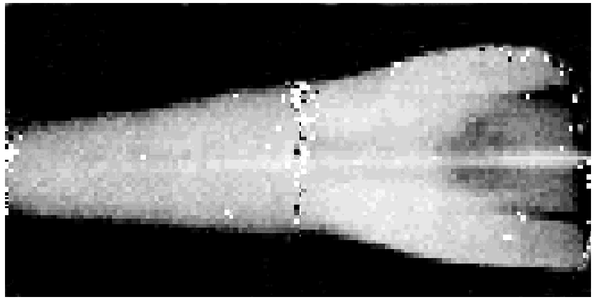
Complex chip, digital on top design

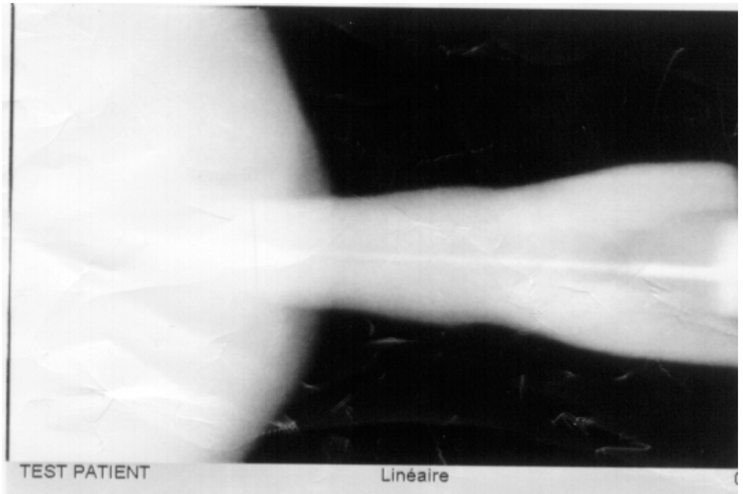
Other applications: photon counting



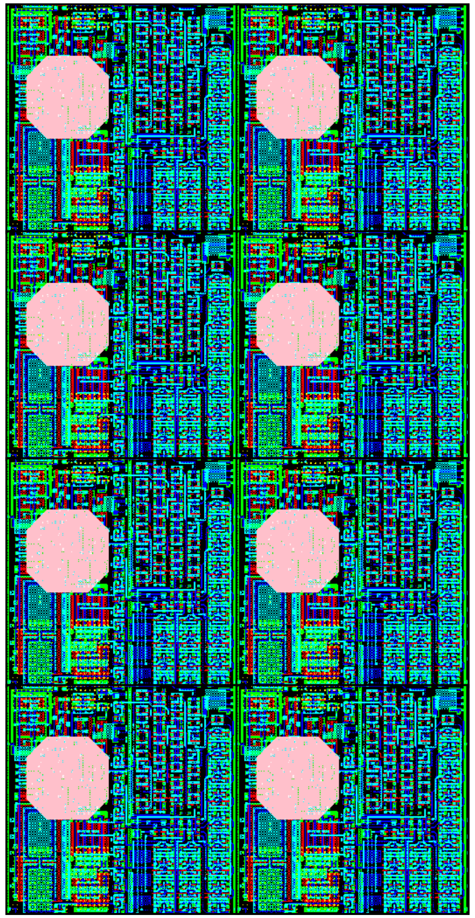
Medipix1 (1997)

- 1 um SACMOS
- 64 x 64 pixels of 170x170 um^2
- 1.2 cm2 sensitive and 1.7 cm2 total area
- 1.6 M transistors

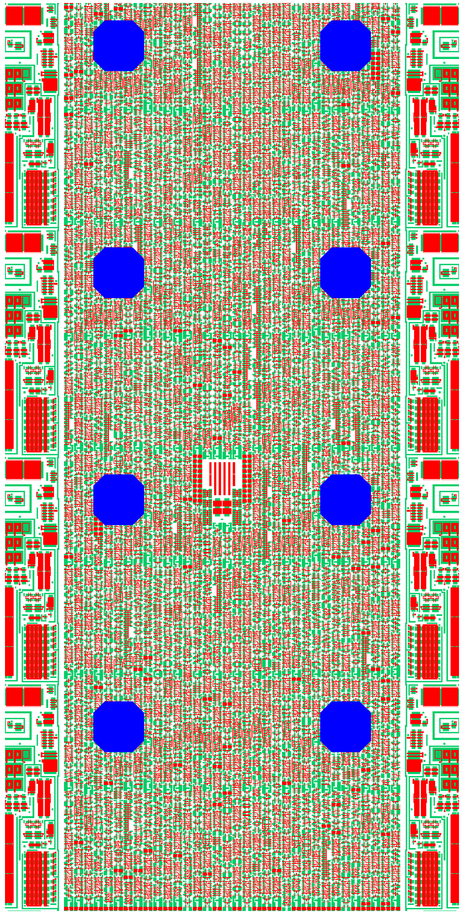




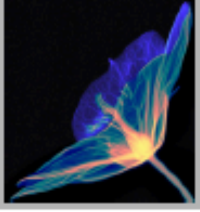
Medipix collaboration
https://medipix.web.cern.ch



Timepix (2006)



Timepix3 (2013)



Timepix3 → Timepix4

			Timepix3 (2013)	Timepix4 (2018/19)
Technology			130nm – 8 metal	65nm – 10 metal
Pixel Size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448
Sensitive area			1.98 cm^2	6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	TOT and TOA
		Event Packet	48-bit	64-bit
		Max rate	<80 Mhits/s	<715 MHz/cm^2/s
		Max pix rate	1.3kHz/pixel	10.6kHz/pixel
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr) CRW (8-bit / 16-bit) Up to 44 KHz frame @8b
		Max count rate	82 Ghits/cm^2/s	~800 Ghits/cm^2/s
TOT energy resolution			< 2KeV	< 1Kev
Time resolution (bin size)			1.56ns	~200ps
Readout bandwidth			≤5.12Gb (8 x SLVS@640 Mbps)	≤163 Gbps (16 x 10.24 Gbps)
Target global minimum threshold			<500 e$^-$	<500 e$^-$

Timepix4 with 4x Timepix3 sensors + NIKHEF Board

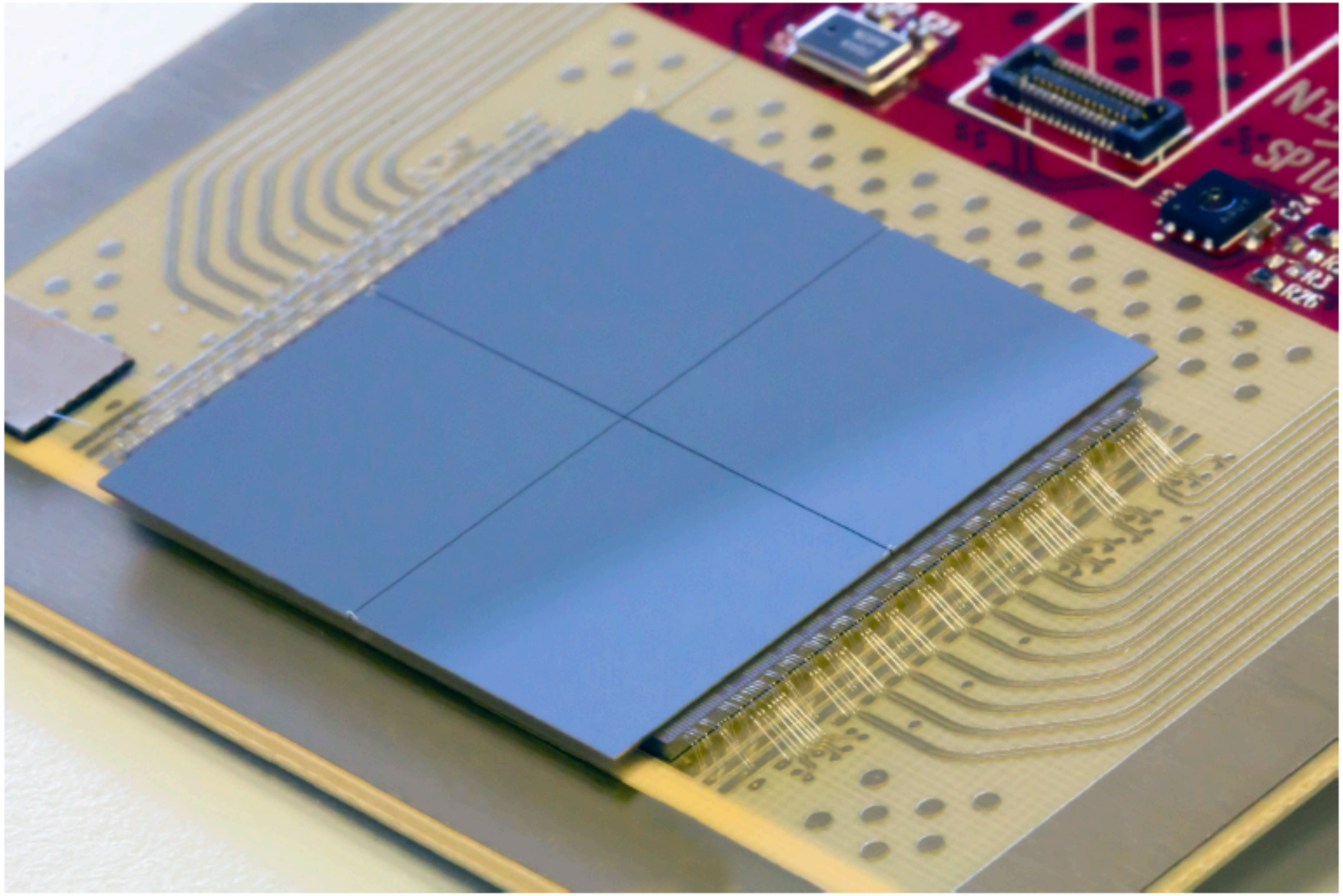
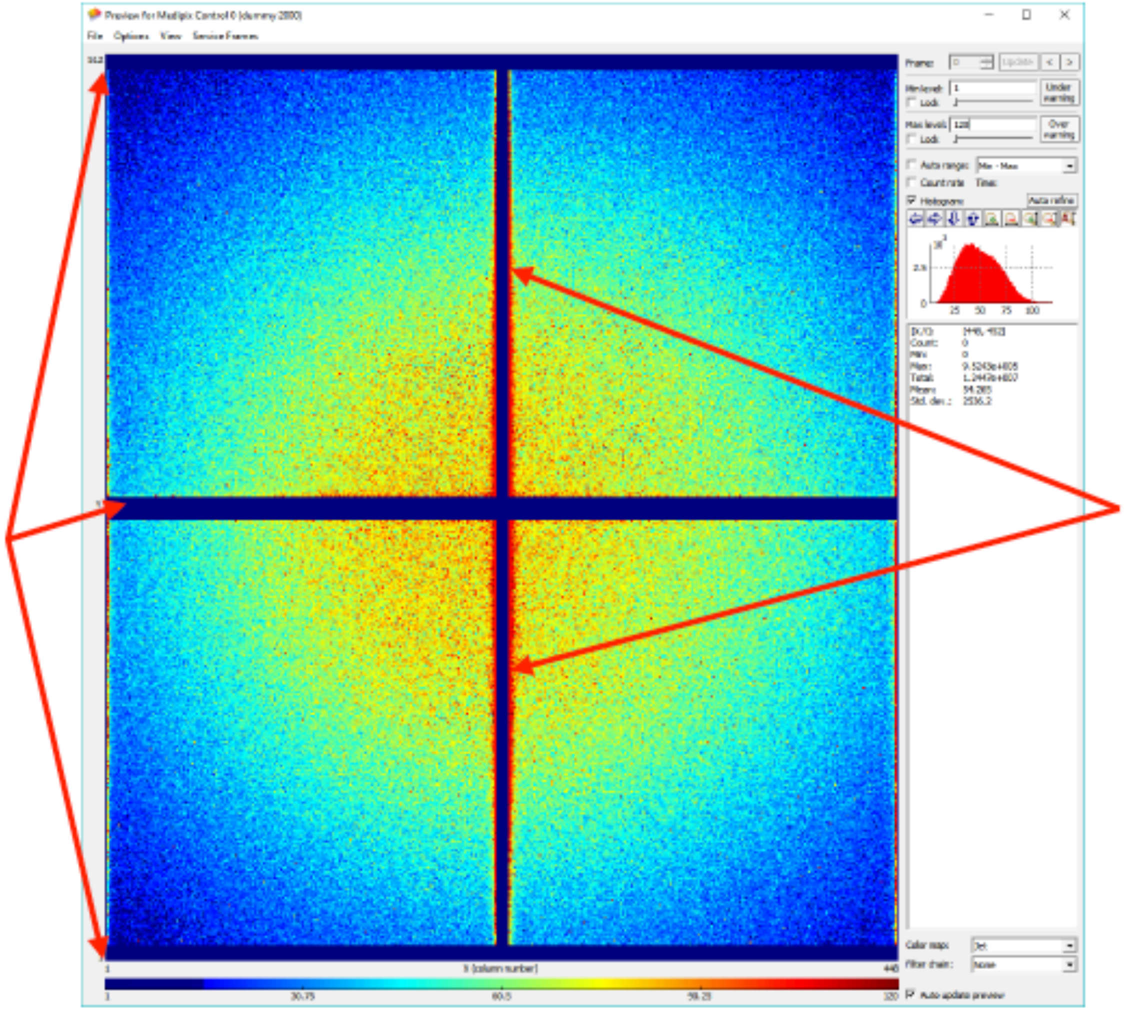


Photo courtesy of M. Fransen, Nikhef

Fe55 1h FB mode Thr=500e-

- PC 8-bit frame based, 3600s acquisition time in CRW but through Slow Control
  - ~1.2 full frame/s → ~3800 individual frames → No visual effect

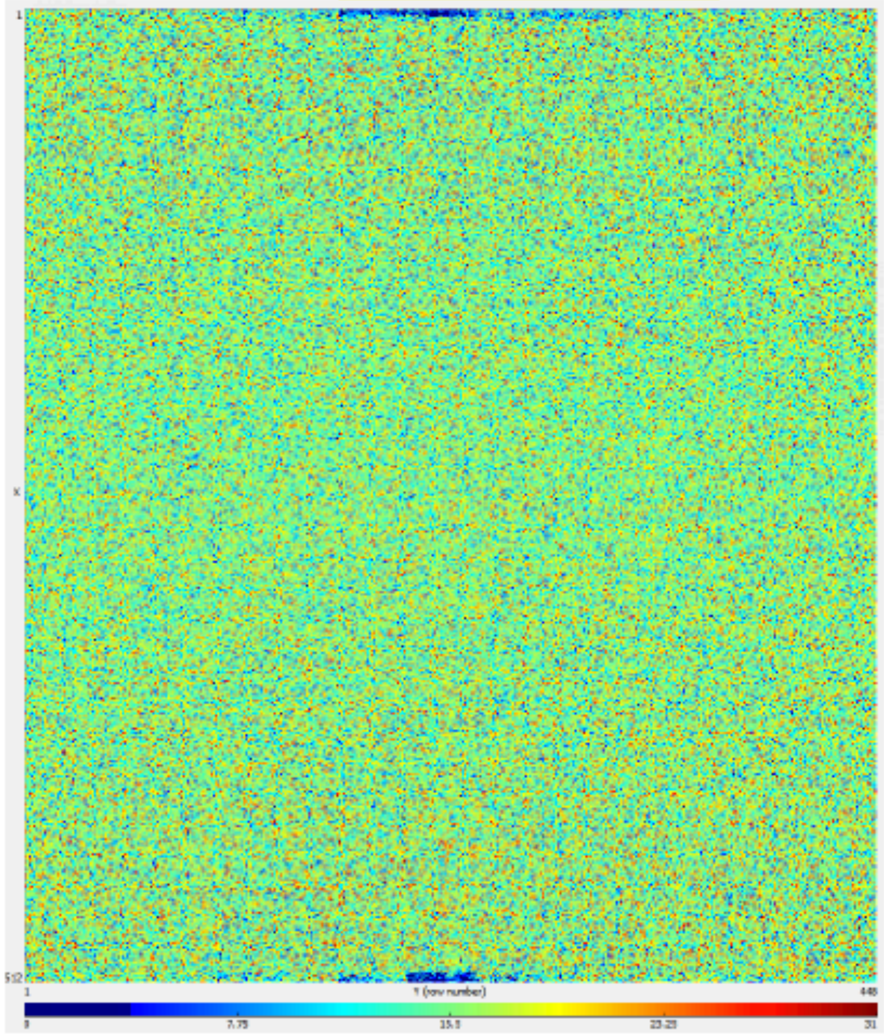


Masked pixels on perpheries:
Top/Bot=8 rows
Center=12 rows

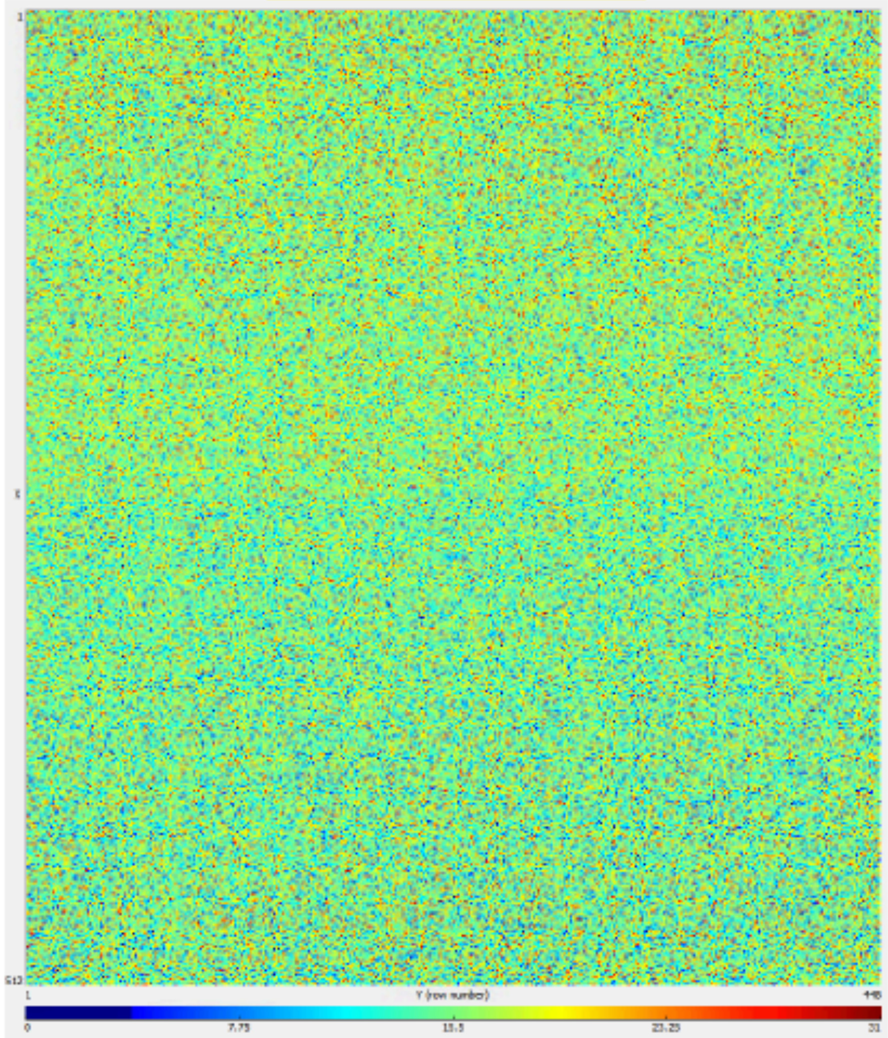
Masked pixels due to sensor edges
7 columns

Threshold Equalization [eq_codes]

Timepix4v0



Timepix4v1



CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

reaching:

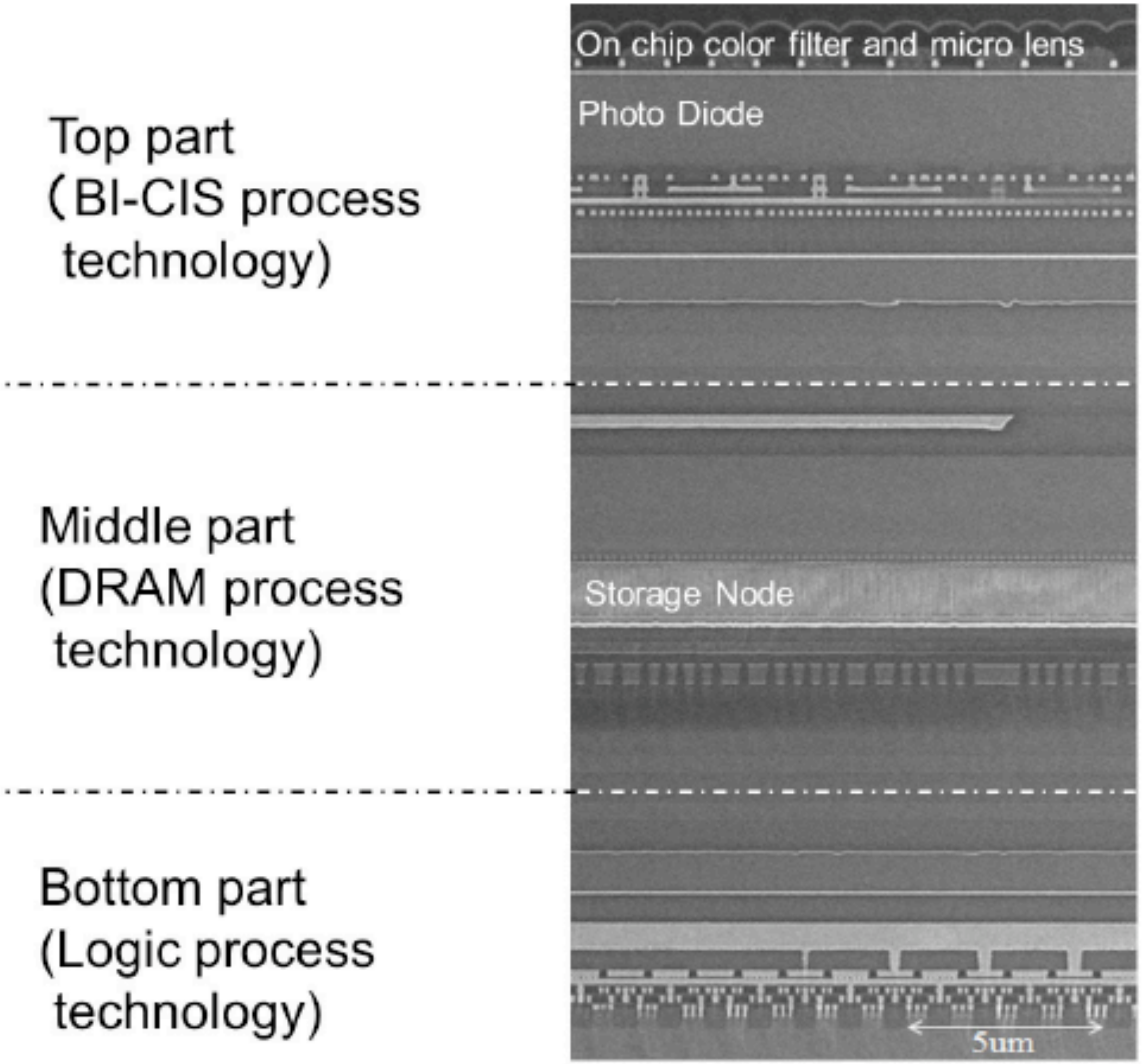
- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking
- …

Silicon has become the standard in tracking applications both for sensor and readout

(see also Prof. Kazuhiko Hara's presentation)

… and now CMOS MAPS make their way in High Energy Physics !

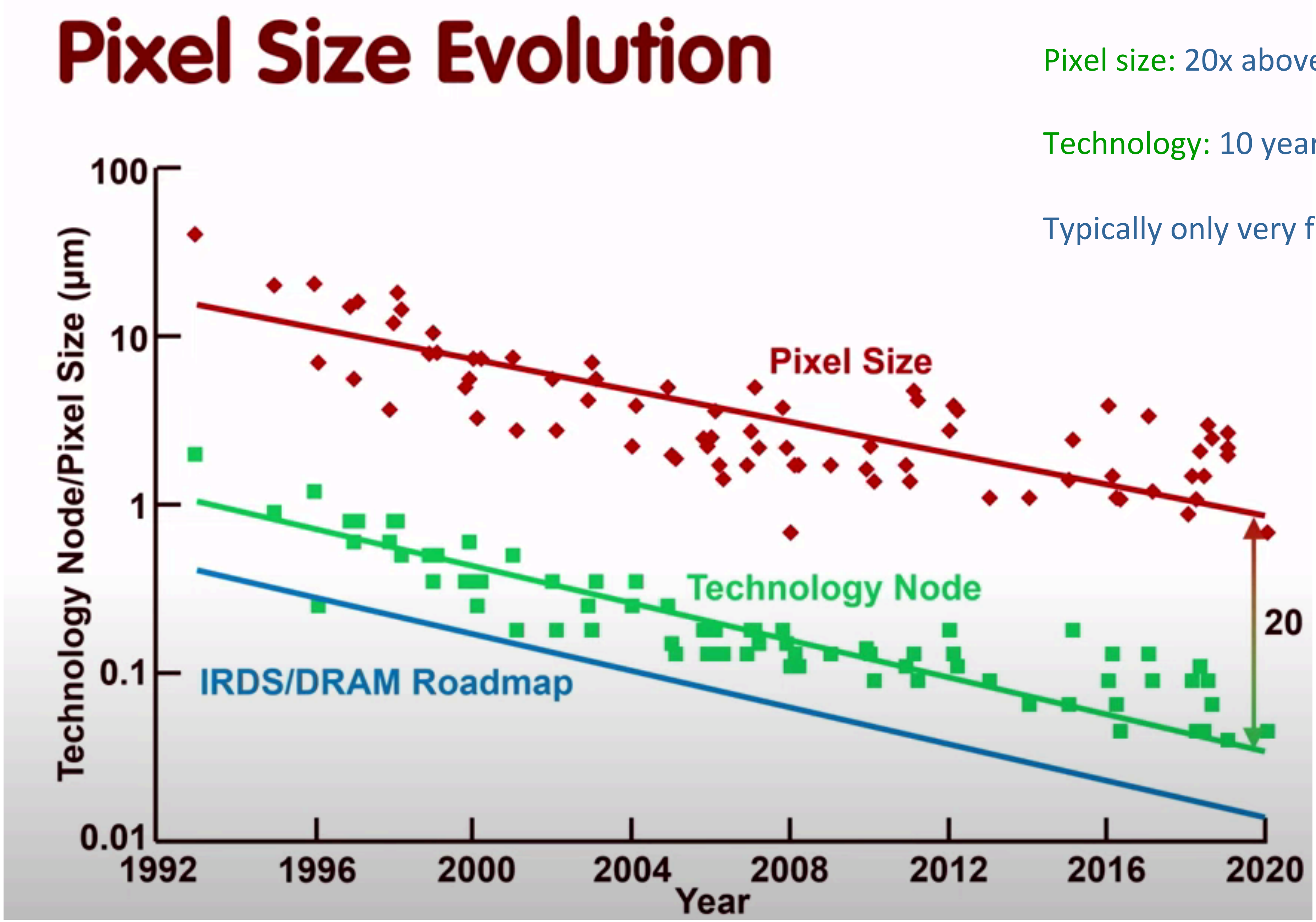
Hybrid still in majority in presently installed systems



Sony, ISSCC 2017

New technologies (TSV's, microbumps, wafer stacking…) make the distinction more vague.

Evolution of pixel size and technology node for visible:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

Typically only very few (1-4) transistors per pixel

Albert Theuwissen, ISSCC 2021

Requirements for High Energy Physics

	Dose (Mgy)	Fluence (10^{16} $1MeVn_{eq}/cm^2$)
ALICE ITS	0.01	10^{-3}
LHC	1	0.1…0.3
HL-LHC $3ab^{-1}$	5	1.5
FCC	10-350	3-100

Radiation tolerance

- CMOS circuit typically more sensitive to ionizing radiation
- Sensor to non-ionizing radiation (displacement damage)

Single particle hits instead of continuously collected signal in visible imaging

- Sparse images < or << 1% pixels hit per event
- Near 100% efficiency, full CMOS in-pixel needed, often circuit (much) more complex

Position resolution (~µm)

Low power consumption is the key for low mass

- Now tens of mW/cm^2 for silicon trackers and hundreds of mW/cm^2 for pixels
- Despite enhanced detector functionality for upgrades, material penalty limits power consumption increase

More bandwidth

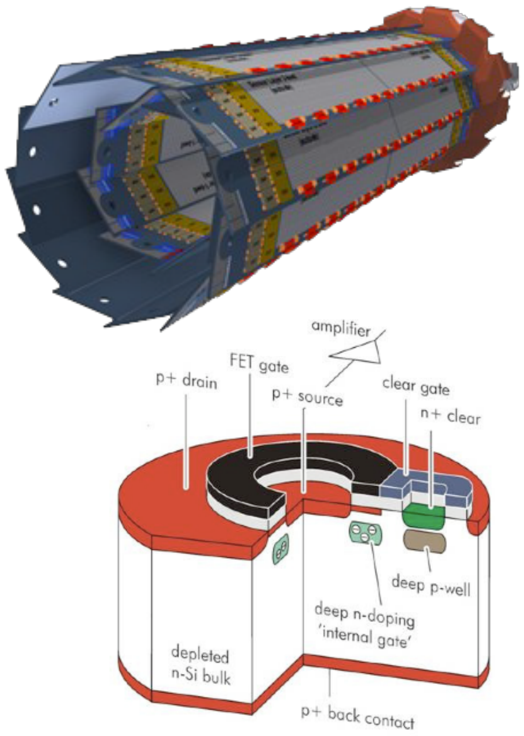
Time resolution

- Time stamping ~ 25 ns or even lower, ... much lower (10s of ps)

Larger and larger areas

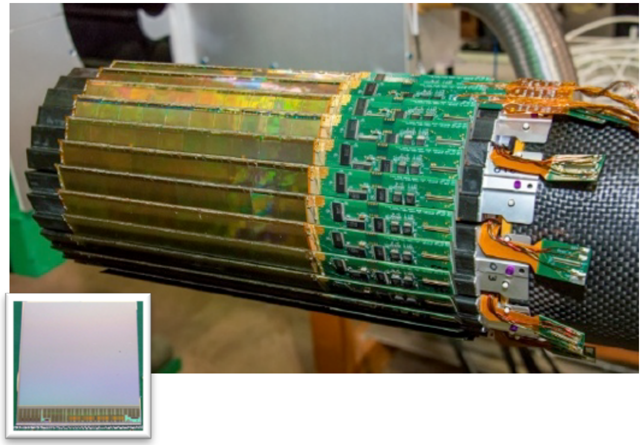
- ALICE ITS2 10 m^2, discussions on hundreds to even thousands square m^2,
- Interest for versatile sensors programmable for different applications (P. Allport CERN EP seminar 2020)

Monolithic sensors in HEP move into mainstream technology



DEPFET in Belle

See also
Prof. Struder's presentation



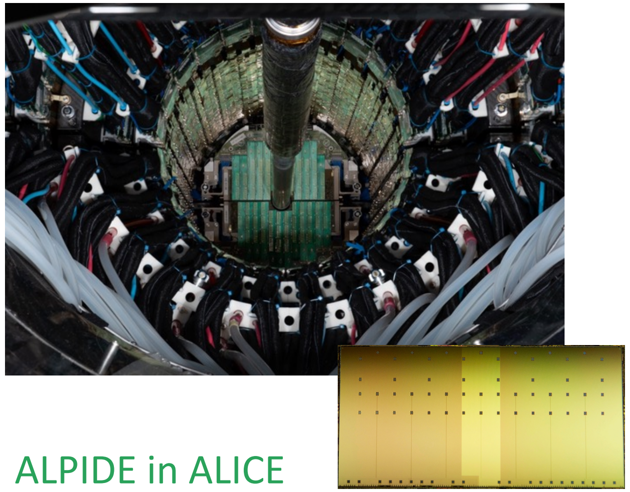
MIMOSA28 (ULTIMATE) in STAR

IPHC Strasbourg

First MAPS system in HEP

Twin well 0.35 µm CMOS

- Integration time 190 µs
- No reverse bias -> NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- Rolling shutter readout



ALPIDE in ALICE

First MAPS in HEP with sparse readout similar to hybrid sensors

Quadruple well 0.18 µm CMOS

- Integration time <10 µs
- Reverse bias but no full depletion -> NIEL ~10^{14} 1 MeV n_{eq}/cm^2

DEPLETED MAPS for better time resolution and radiation tolerance

Large collection electrode

LF Monopix, MuPix,...

Extreme radiation tolerance and timing uniformity, but large capacitance

Small collection electrode

ARCADIA LF, TJ Malta, TJ Monopix, Fastpix, CLICTD, SOIPIX...

- Sub-ns timing
- NIEL >10^{15} 1 MeV n_{eq}/cm^2 and beyond

Commercial deep submicron CMOS technology evolved "naturally" towards

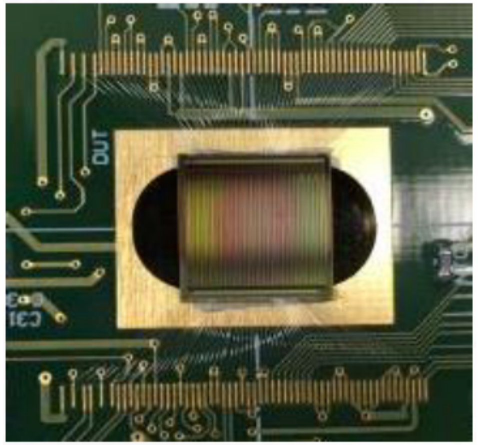
- Very high tolerance to ionizing radiation (some caveats, cfr G. Borghello, F. Faccio et al.)
- Availability of substrates compatible with particle detection
- Imaging technology not absolutely required, but some flexibility/features very beneficial for sensor optimization, both for small and large collection electrode structures.

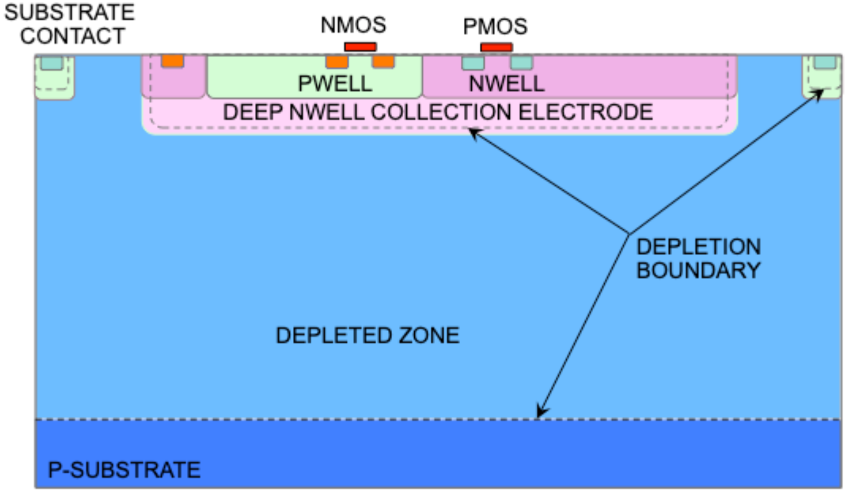
Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)

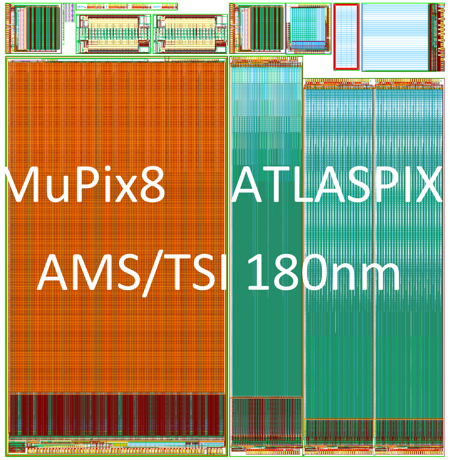
MONOPIX

50 x 250 µm^2 pixel

Lfoundry 150 nm



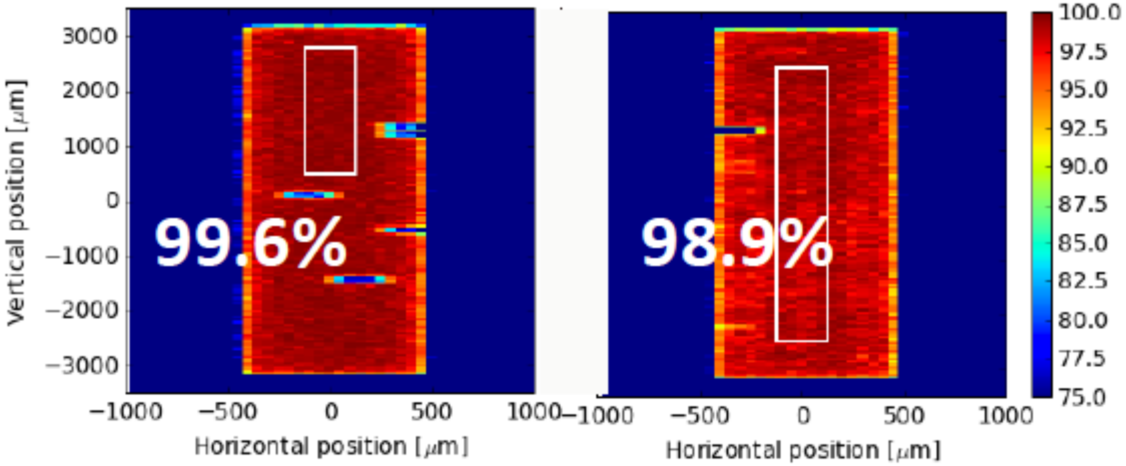


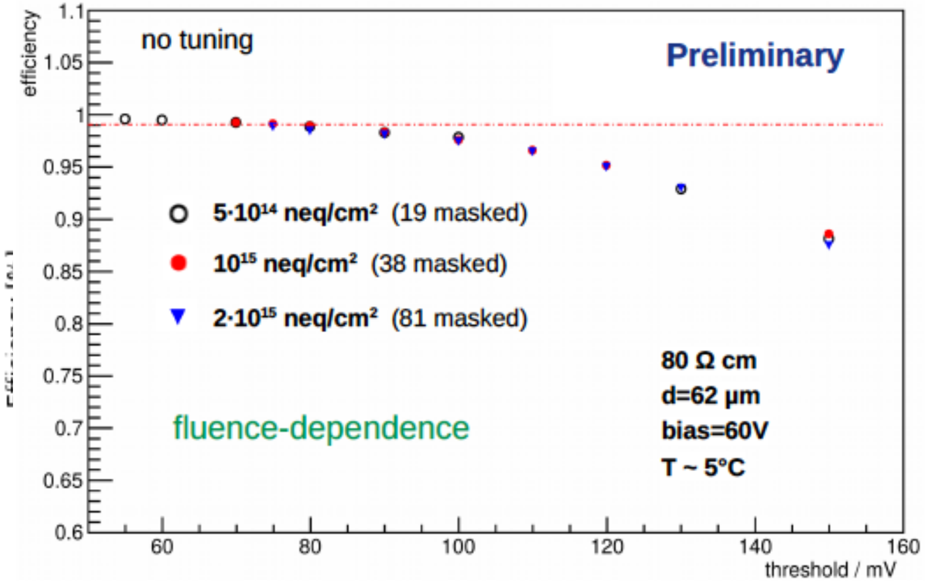


MuPix8 ATLASPIX

AMS/TSI 180nm

Efficiency non-irradiated after 1.14 E15 n_{eq}/cm^2

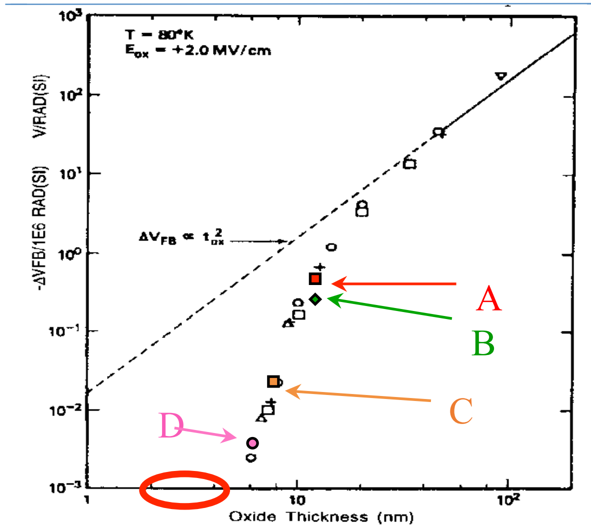




T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059

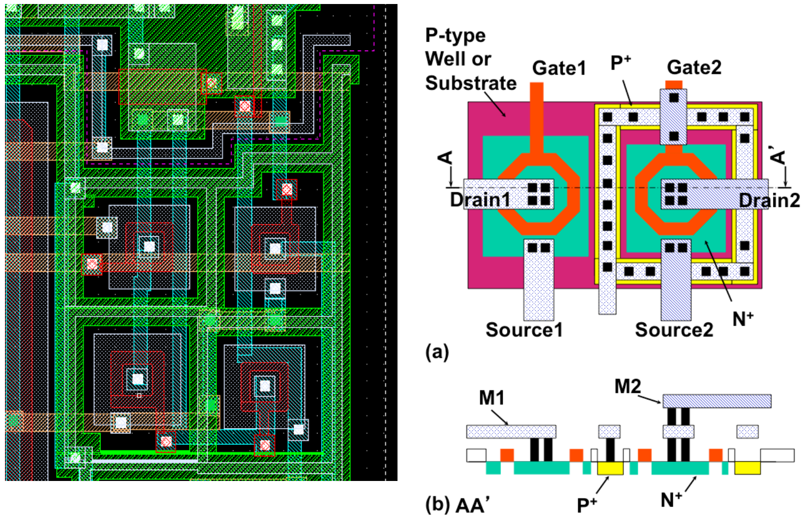
Courtesy I.Peric and A. Schoening

Circuit radiation tolerance: like standard CMOS

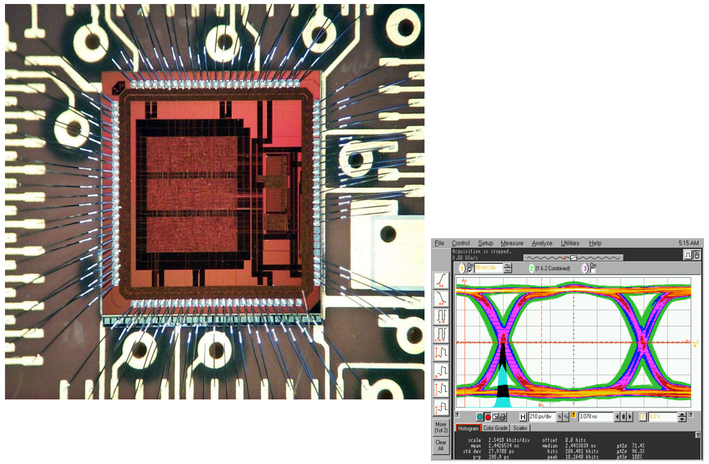


Now here

After N.S. Saks et al, IEEE TNS, Vol. NS-31 (1984) 1249



G. Anelli et al., IEEE TNS-46 (6) (1999) 1690



P. Moreira et al.
http://proj-gol.web.cern.ch/proj-gol/

Total ionizing dose:

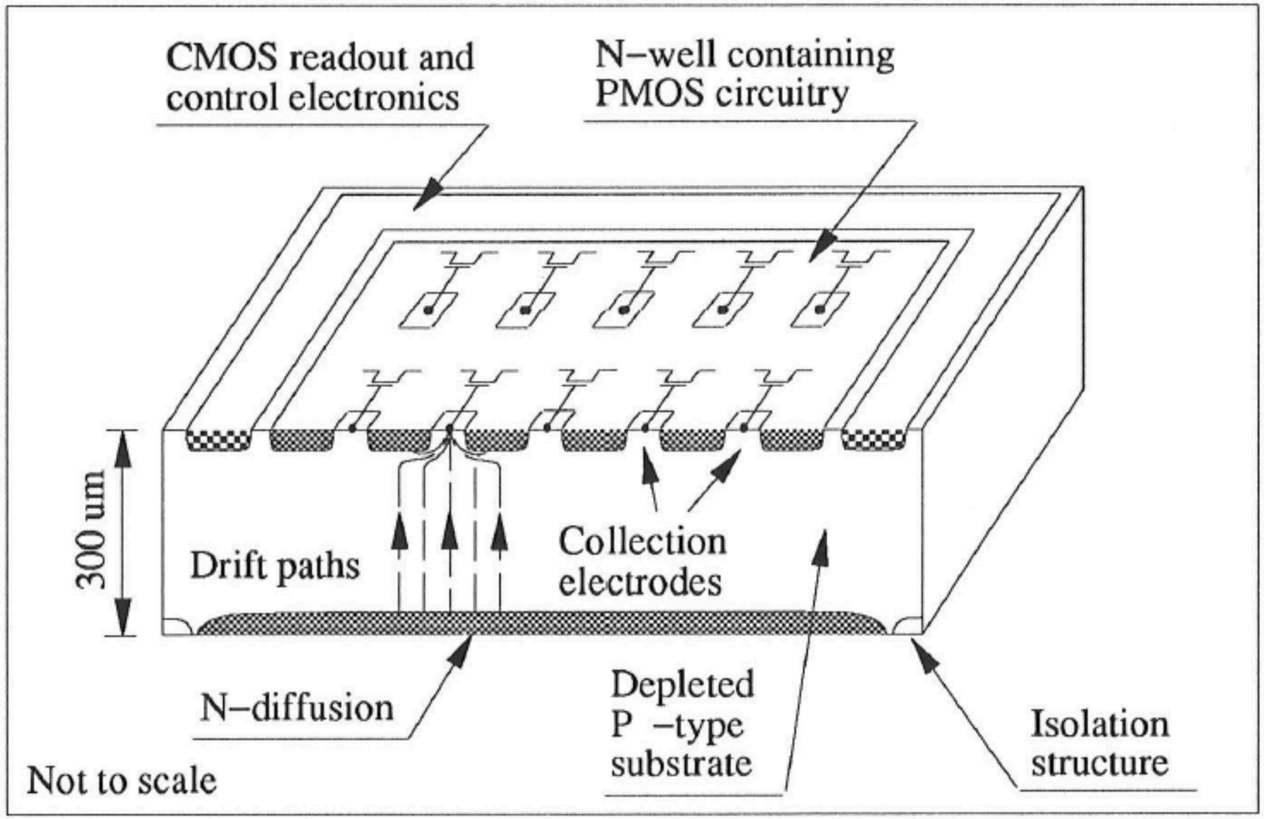
- Intrinsic transistor has become more and more radiation tolerant due to thinner gate oxide
- In LHC enclosed NMOS transistors and guard rings in 0.25 µm CMOS to avoid large leakage current
- In deeper submicron enclosed geometry usually no longer necessary for leakage, but for small dimensions parasitic effects dominate e.g. from spacers, new gate dielectrics, **requires extensive measurement campaigns**

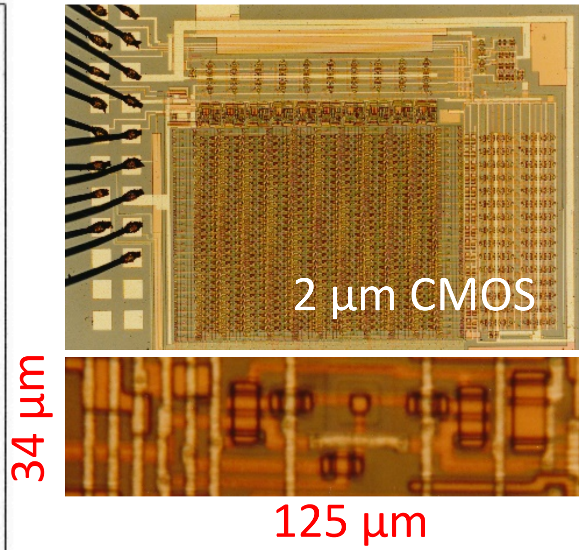
F. Faccio et al. IEEE TNS-65 (1) 164, 2018

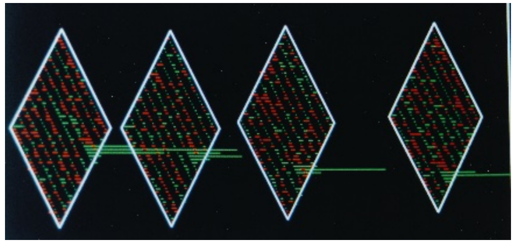
Single event effects:

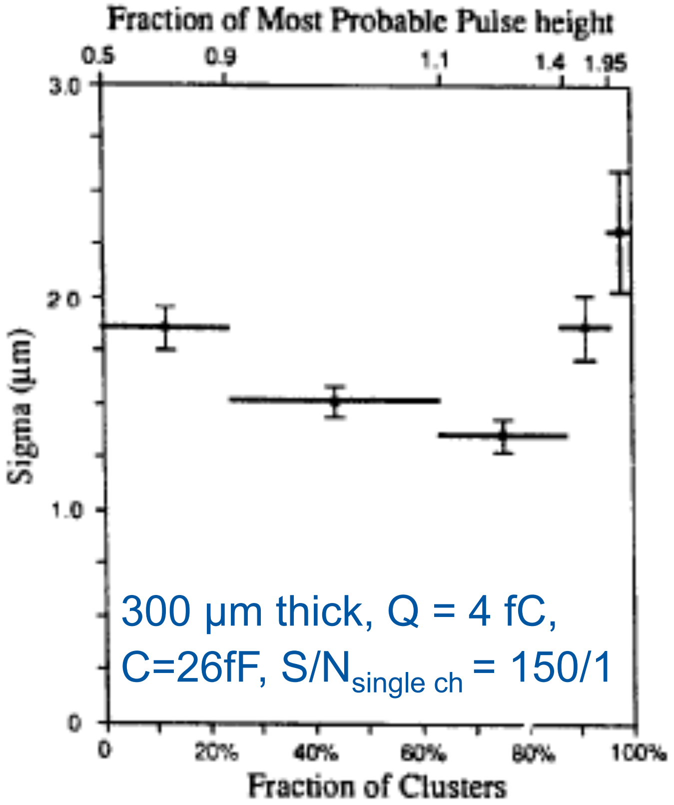
- Single Event Upset : triple redundancy with majority voting (now special scripts S. Kulis)
- Latch-up not observed so far in LHC, but observed on MAPs at STAR, and in new technologies => **need attention in the design**

Towards standard technology, but double-sided processing



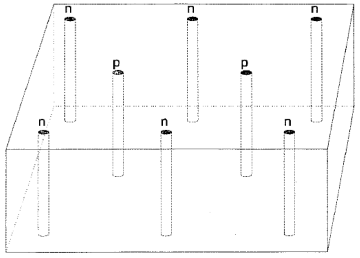






300 µm thick, Q = 4 fC, C=26fF, S/N$_{\text{single ch}}$ = 150/1

- Separation of junction from collection electrode
- Better than 2 µm position resolution even at large pitch due to good S/N
- Improved back side isolation with trenches lead to sensors with 3D electrodes (S.Parker) →

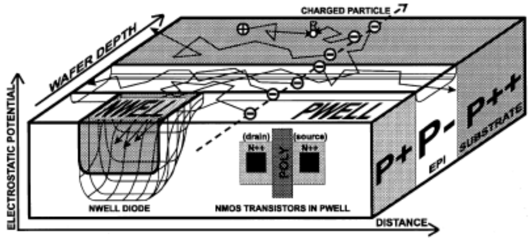


C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

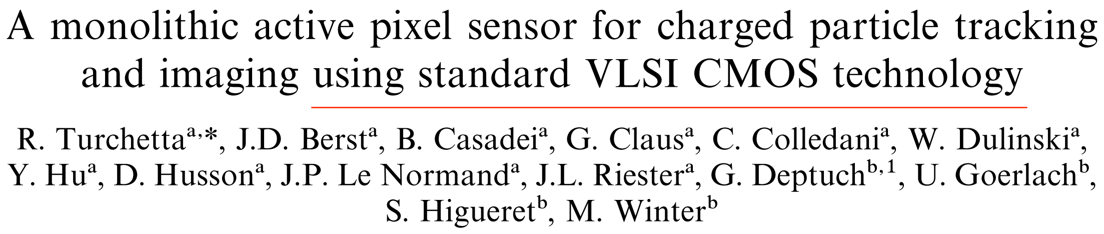
Other examples: ~ 1 µm resolution: SOI sensor, pitch 13.75 µm *M. Battaglia et al. NIM A 654 (2011) 258-265, NIM A 676 (2012) 50-53*

Position resolution: good S/N for interpolation Junction separation and back side processing: see below

Mimosa series – IPHC Strasbourg

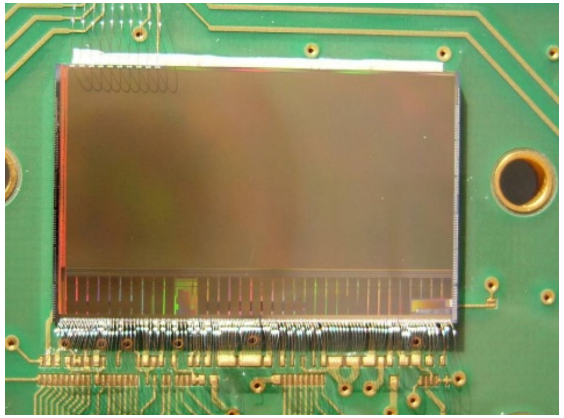


NIM A 458 (2001) 677-689



A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]



Rolling shutter readout

Mimosa26 – 2008

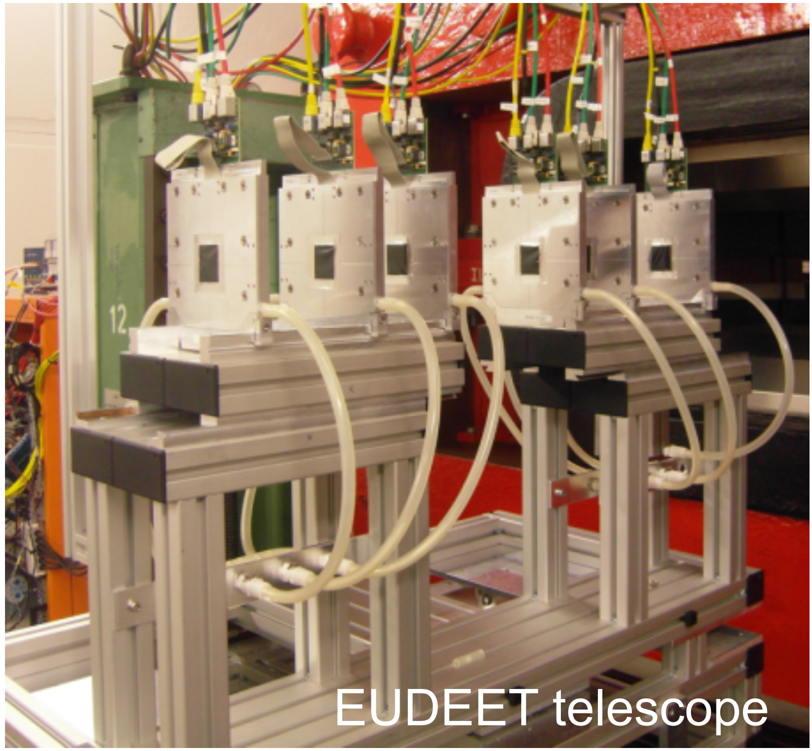
AMS 0.35 µm

18.4 µm pixel pitch 576x1152 pixels

First MAPS with integrated zero-suppressed readout

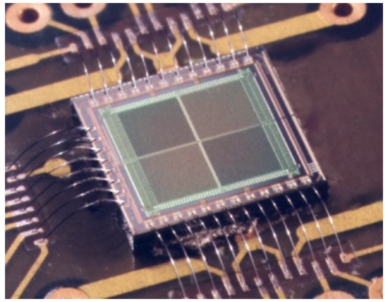
First MAPS used for several applications, also for EUDEET telescope

Courtesy of C. Hu IPHC Strasbourg



EUDEET telescope

Mimosa1 – 1999
AMS 0.6 µm

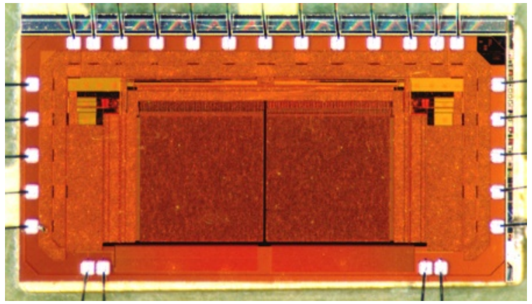


20µm pixel

Mimosa2 – 2000
MIETEC 0.35 µm

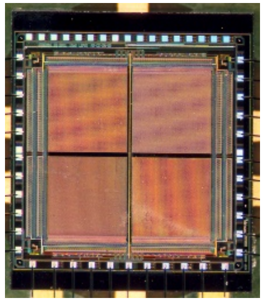
20µm pixel

Mimosa3 – 2001
IBM 0.25 µm



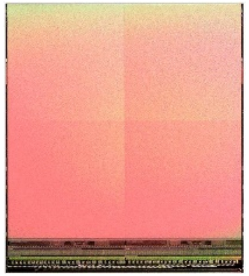
8µm pixel

Mimosa4 – 2001
AMS 0.35 µm



20 µm pixel

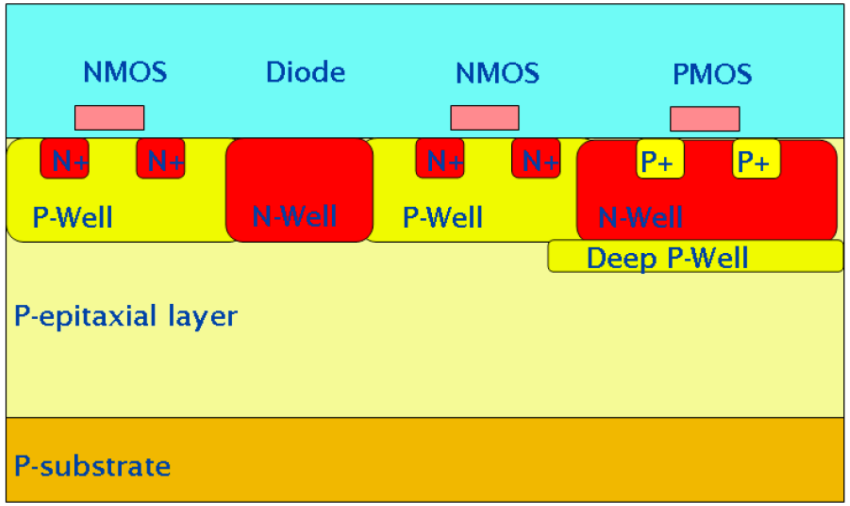
Mimosa5 – 2001
AMS 0.6 µm



17 µm pixel

....

The INMAPS process: quadruple well for full CMOS in the pixel



STFC development, in collaboration with TowerJazz

Additional deep P-well implant allows complex in-pixel CMOS and 100 % fill-factor

New generation of CMOS sensors for scientific applications (TowerJazz CIS 180nm

Also 5Gb/s transmitter in development

Sensors 2008 (8) 5336, DOI:10.3390/s8095336

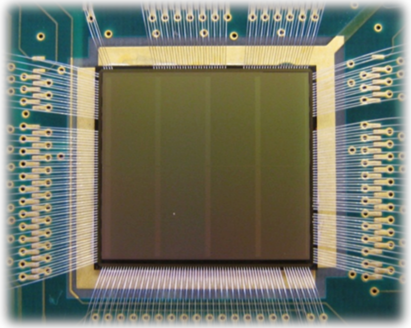
https://iopscience.iop.org/article/10.1088/1748-0221/7/08/C08001/meta

https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01006/meta

http://pimms.chem.ox.ac.uk/publications.php …

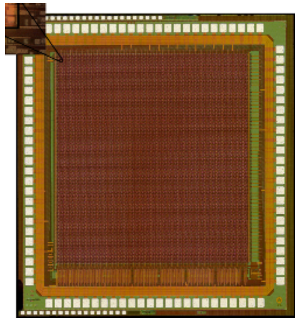
courtesy of N. Guerrini, STFC

TPAC
ILC ECAL (CALICE)



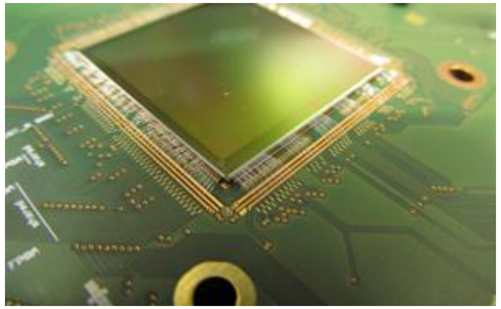
50μm pixel

DECAL
Calorimetry



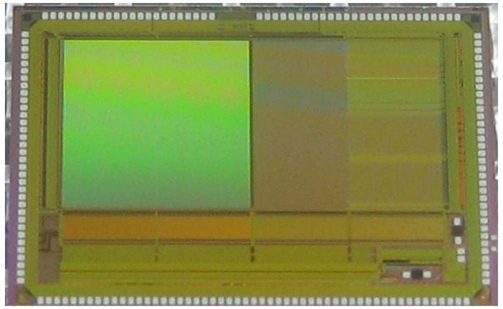
50μm pixel

PIMMS
TOF mass spectroscopy

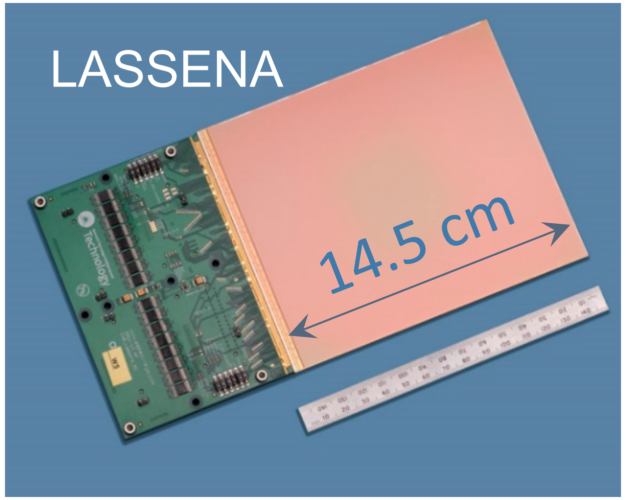


70μm pixel

CHERWELL
Calorimetry/Tracking



48 μm x 96 μm pixel

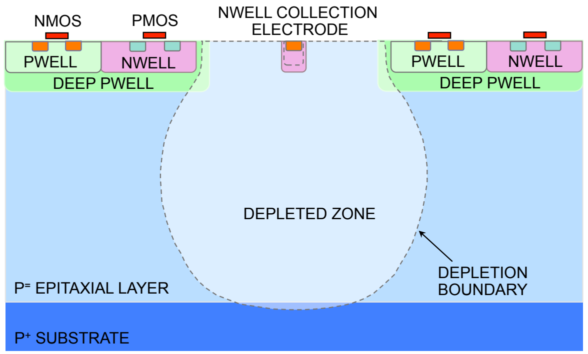


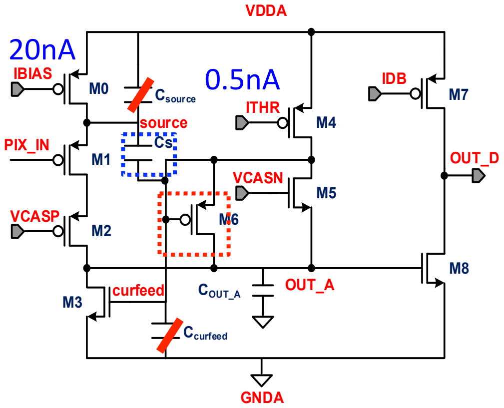
50μm pixel, waferscale

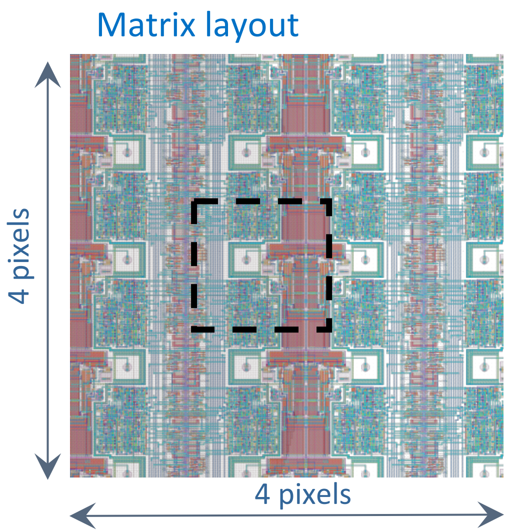
walter.snoeys@cern.ch

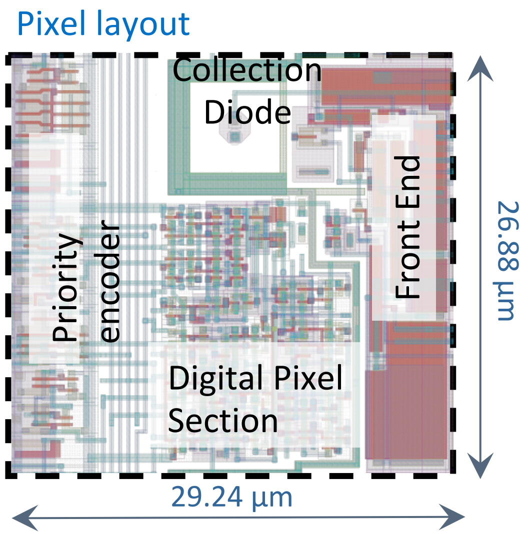
Standard INMAPS process also used for the ALPIDE (27 μm x 29 μm pixel) and MIMOSIS (CBM)

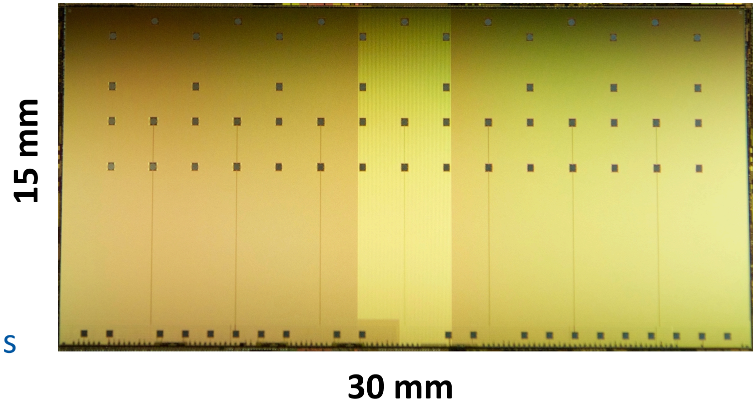
ALPIDE chip in ALICE ITS2



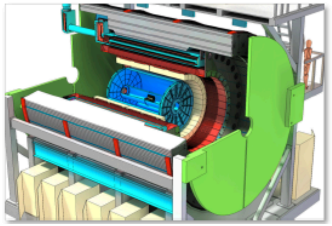


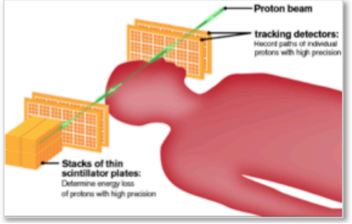




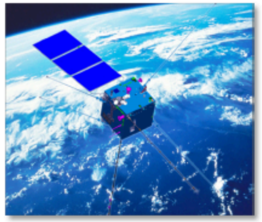


- TJ CMOS 180 nm INMAPS imaging process (TJ) > 1kΩ cm p-type epitaxial layer
- Small 2 µm n-well diode and reverse bias for low capacitance C(sensor+circuit) < 5 fF
- 40 nW continuously active front end D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042
- Q_{in}/C ~ 50 mV, analog power ~ $(Q/C)^{-2}$ NIM A 731 (2013) 125
- Zero-suppressed readout, no hits no digital power G. Aglieri et al. NIM A 845 (2017) 583-587
- Ratio between 15 x 30 mm^2 and 10 m^2 in the experiment not ideal -> stitching -> see below
- ALPIDE (ALICE Pixel Detector) to be used for several other physics experiments, in space and for medical applications


sPHENIX



Proton CT (tracking)


CSES – HEPD2

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys (Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test
1 MPW run and 5 engineering runs 2012-2016, production 2017-2018

ITS2 installed in the ALICE experiment

CERNCOURIER

July/August 2021 cerncourier.com

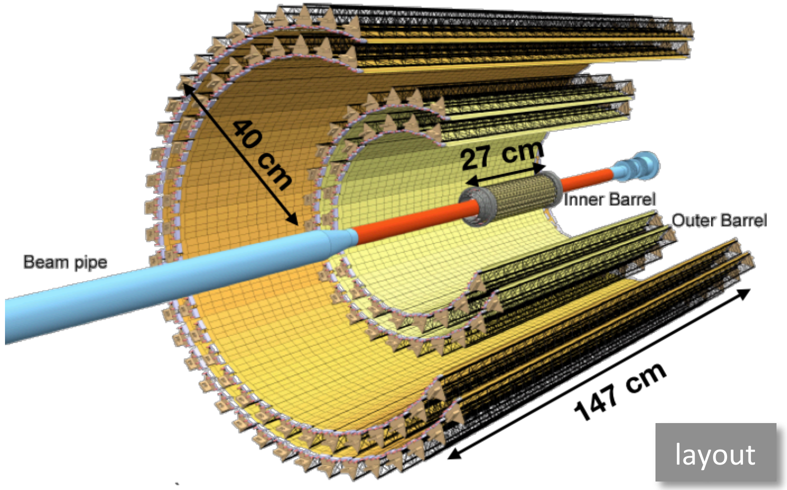
Reporting on international high-energy physics

PIXEL PERFECT

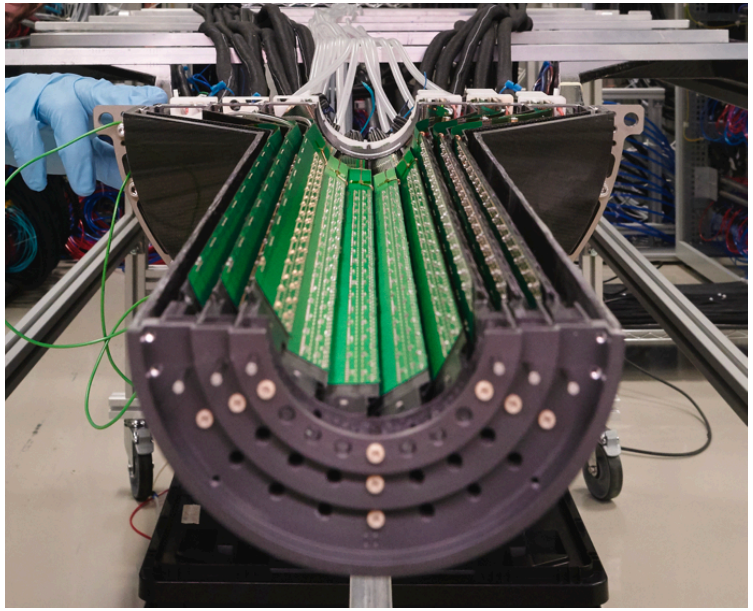
Exploring the Hubble tension

A CERN for climate change

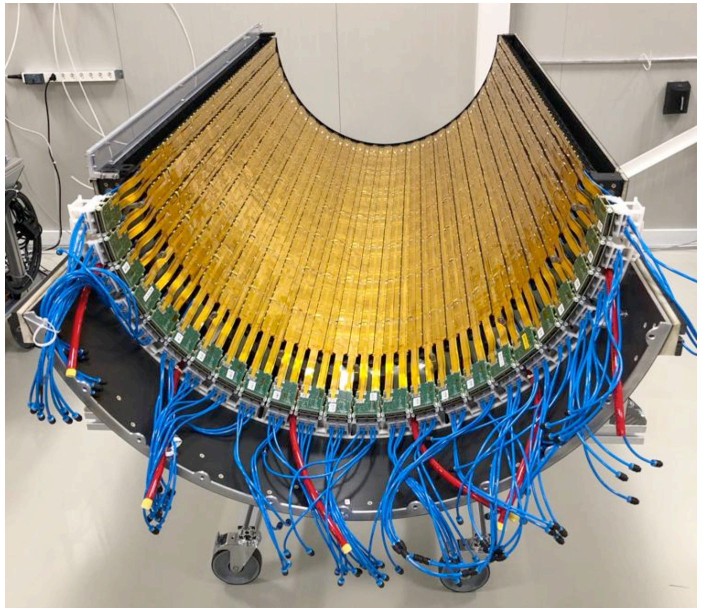
Medical technologies



layout



Assembled three inner-most half-layers

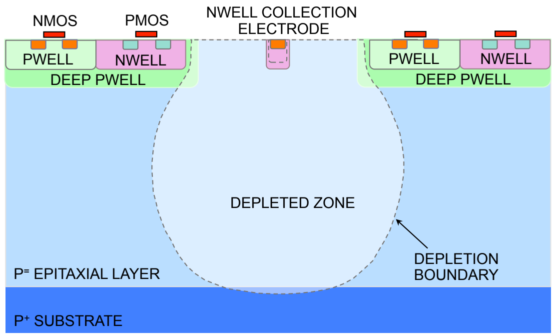


Half outer barrel (layer 6)
~ 2.47 Gpixels covering ~ 2 m^2 sensitive area

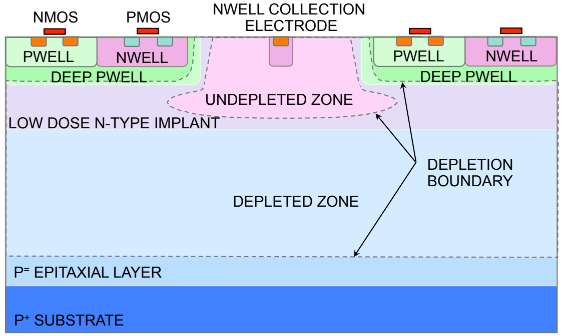
Sensor optimization: Moving the junction away from the collection electrode

for full depletion, better time resolution and radiation hardness… and better efficiency, especially for thin sensors

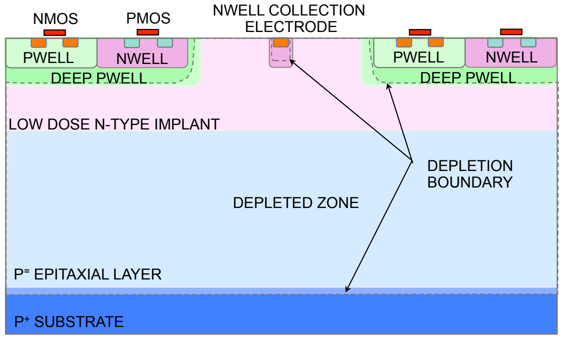
Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)
Collect signal charge FAST before it gets trapped => depletion and large electric field…



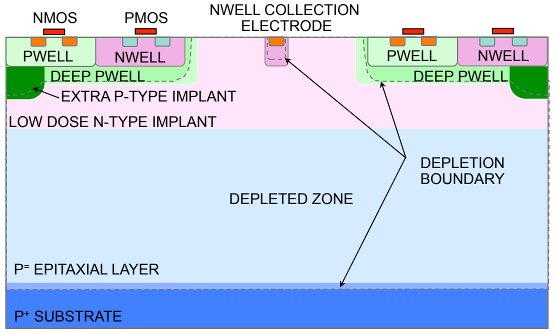
Standard, not fully depleted (ALPIDE)



Not fully depleted at low reverse bias



Depletion at higher reverse bias (MALTA1, MONOPIX)

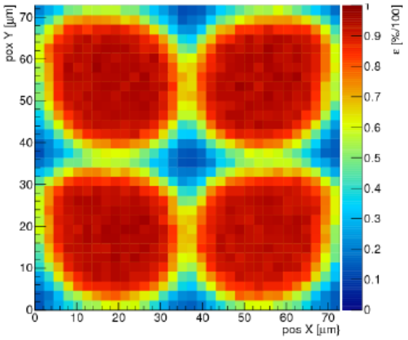


Further improvements by influencing the lateral field

Additional implant for full depletion
=> order of magnitude improvement
Side development of ALICE for ALPIDE
NIMA 871 (2017) pp. 90-96

Triggered development in ATLAS
H. Pernegger et al, 2017 JINST 12 P06008

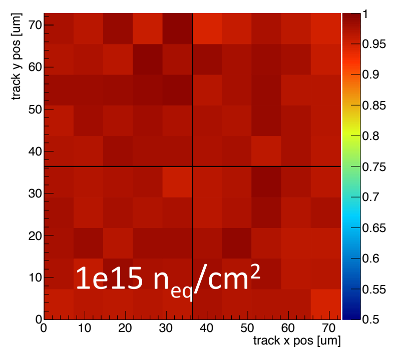
Efficiency drop at pixel edges after 10^{15} n_{eq}/cm^2 irradiation for 36.4 x 36.4 μm^2 pixel needs improvement
E. Schioppa et al, VCI 2019



3D TCAD simulation
M. Munker et al. PIXEL2018

Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019
M. Dyndal et al., arXiv:1909.11987

miniMalta in pixel efficiency, sector 1



1e15 n_{eq}/cm^2

Other similar developments for fast charge collection and depletion:

T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483
H. Kamehama et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027…
L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027
C. Kenney et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

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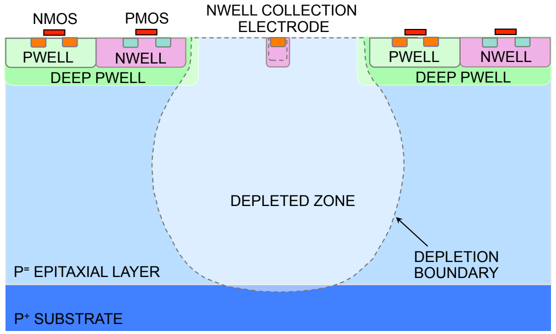

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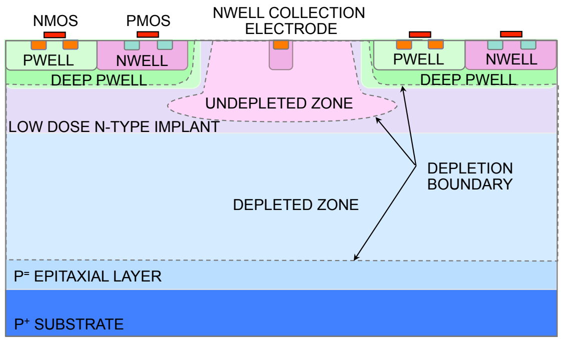
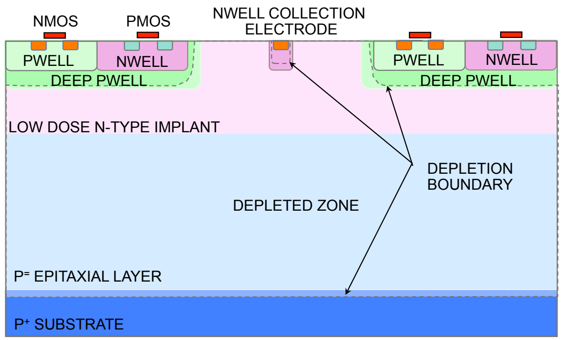


Not fully depleted at low reverse bias



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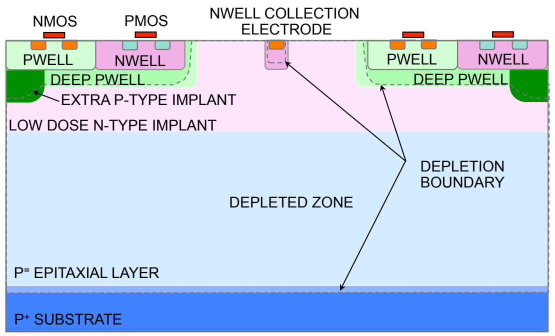
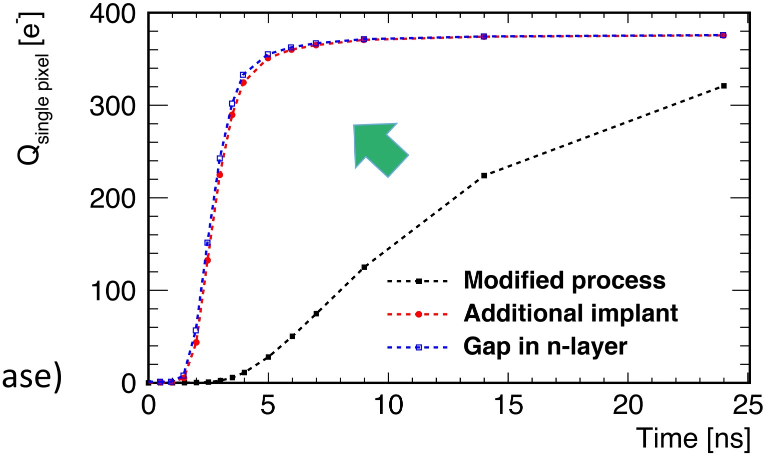


Further improvements by influencing the lateral field

Hit in the pixel corner (= worst case)



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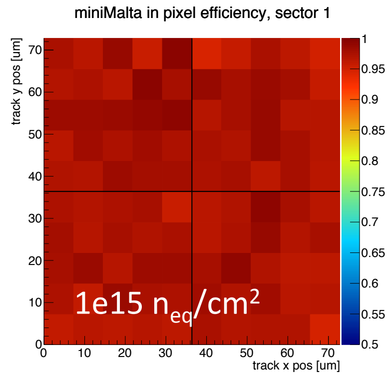

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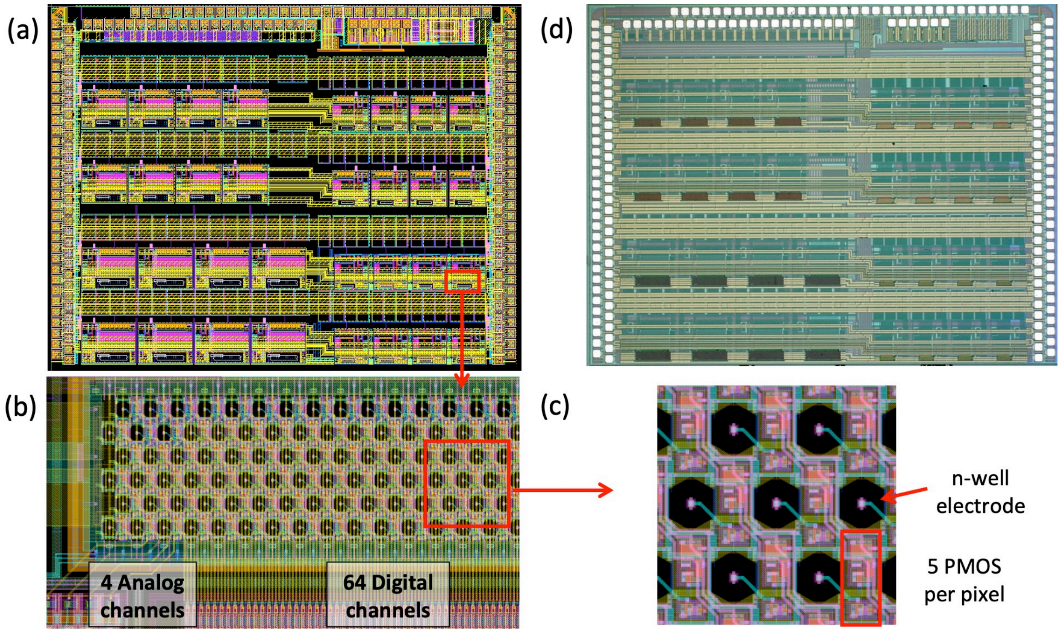
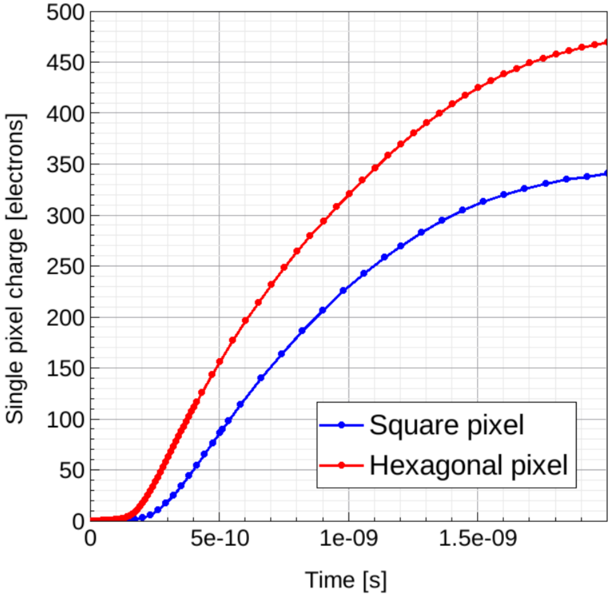
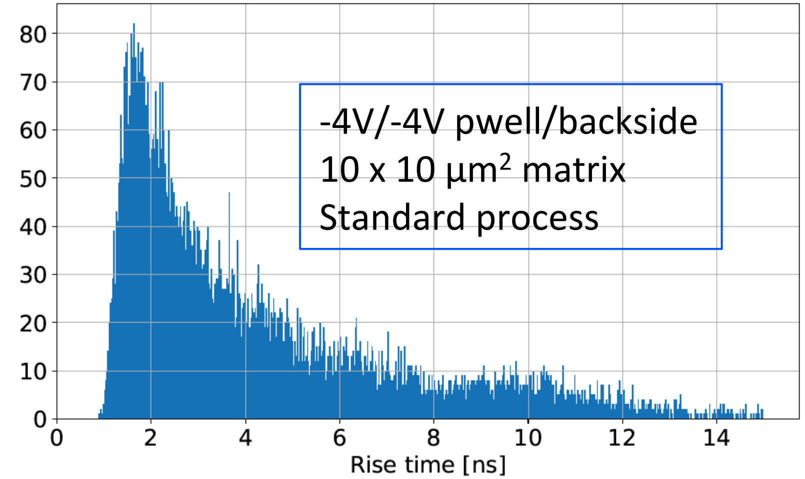
FASTPIX ATTRACT project: ^{90}Sr Risetime distributions

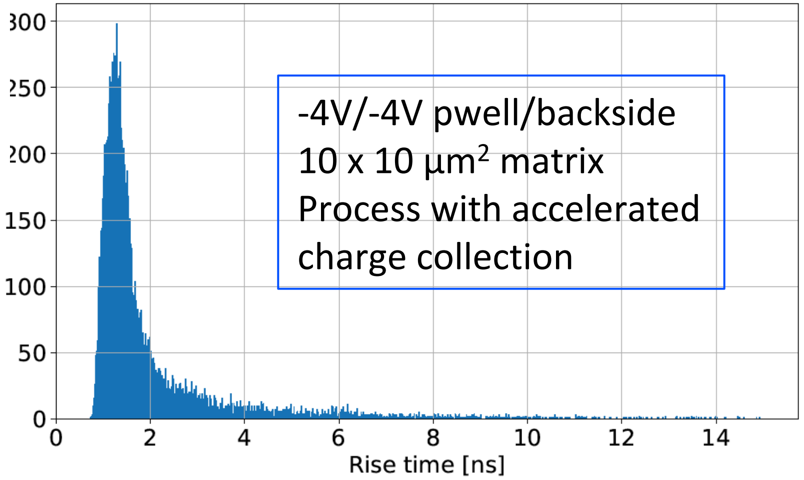


Comparison hexagonal to square pixel cell charge vs. time for MIP incident at pixel corner:



T. Kugathasan et al., https://doi.org/10.1016/j.nima.2020.164461 (ATTRACT: INFN, Ritsumeikan University and CERN)





E. Buschmann, D. Dannheim, K. Dort, M. Muenker

Direct relation between charge collection and process variant (TowerJazz 180nm)

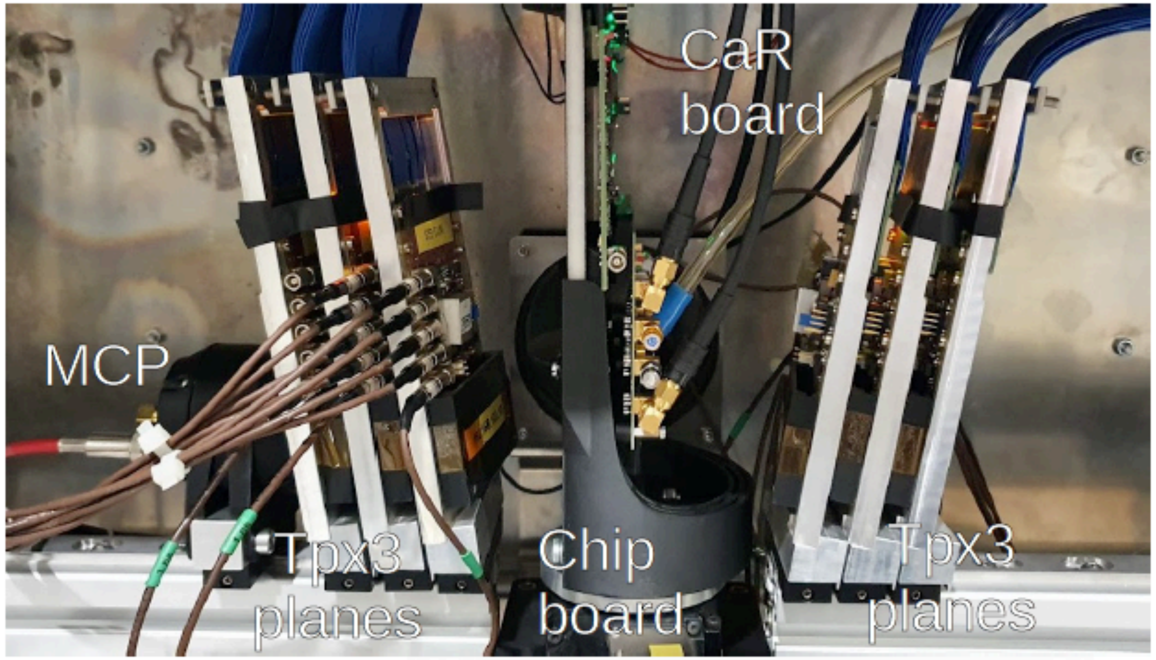
Significant impact even at very small pixel pitch

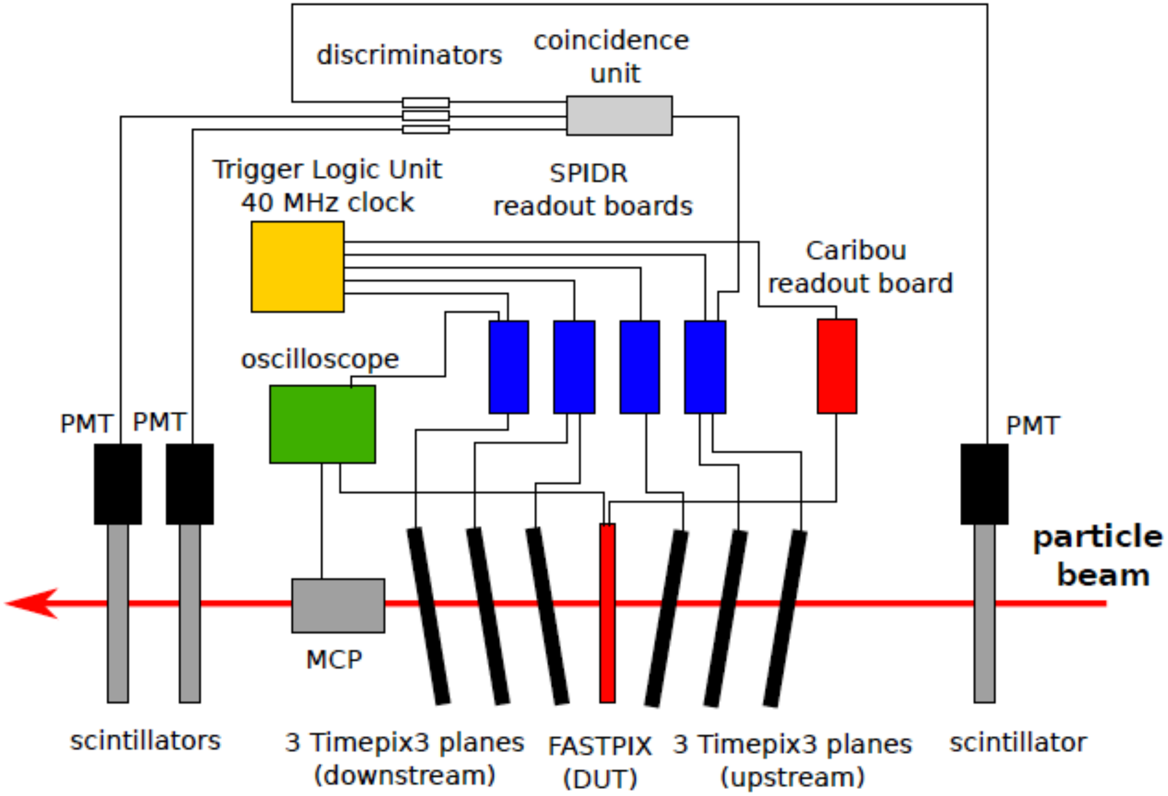
Hexagonal pixels (pitch 8.66, 10, 15 and 20 μm)

- better approximation of a circle
- charge sharing in the corners between 3 pixels instead of 4 -> more margin
- collection electrodes on hexagonal grid, circuit to remain on Manhattan layout

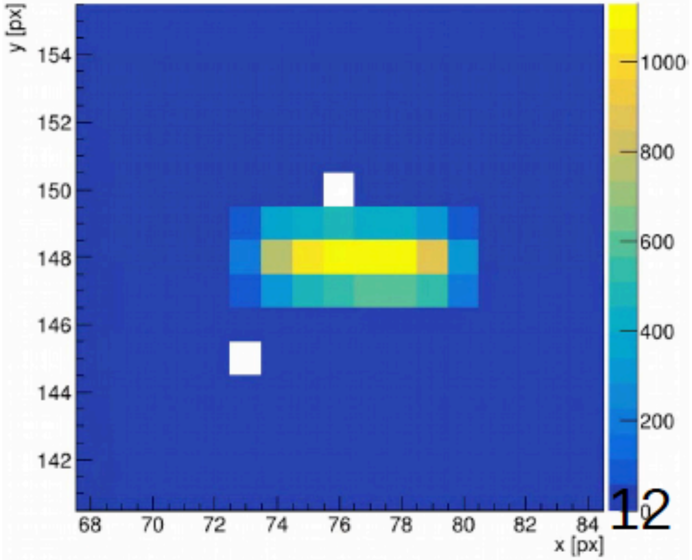
Test-beam Measurements - Setup

- Test-beam at SPS in August and September in Timepix3 telescope
- Micro-channel plate as fast time reference (expected resolution below 10ps, see: J. Bortfeldt et al.)
- New improved chip board for FASTPIX



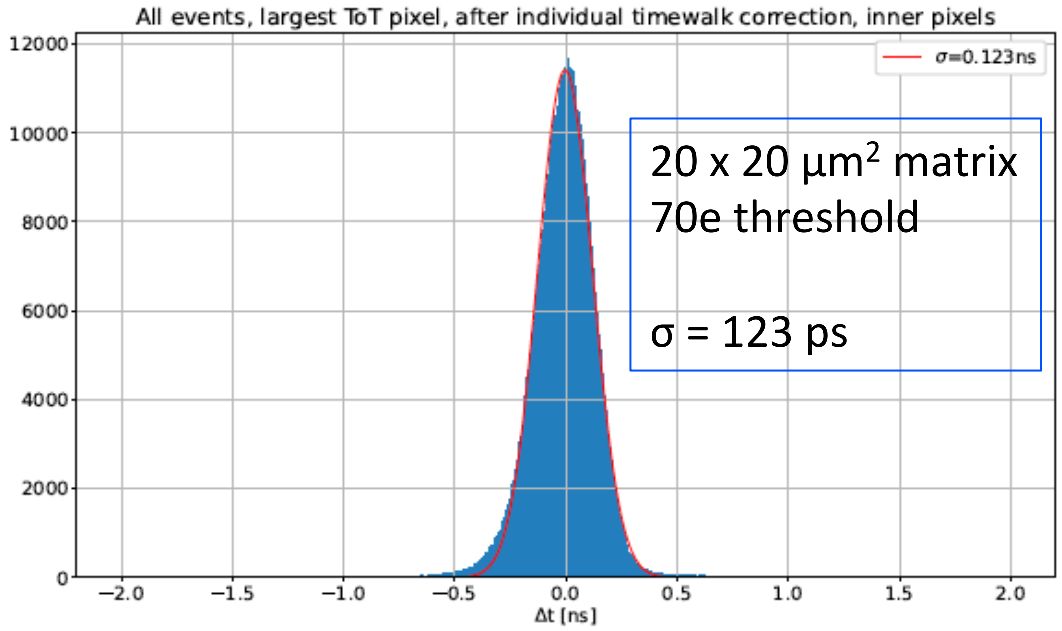


Hitmap of TPX3 plane showing events with associated FASTPIX triggers ($55\times55\text{um}^2$ pixels on TPX3)



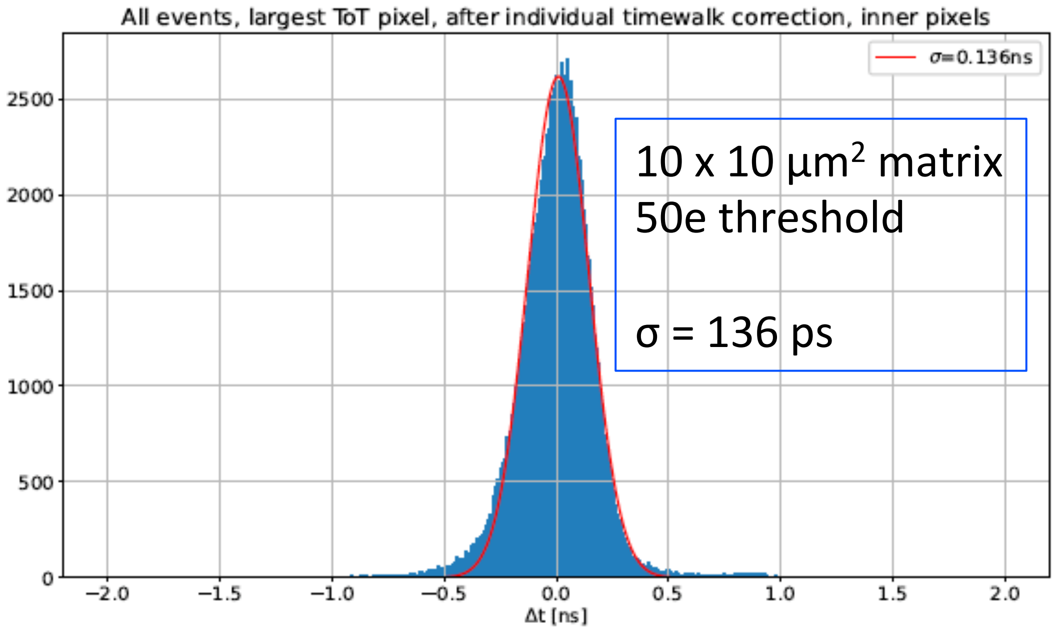
- Readout of FASTPIX and MCP with oscilloscope
- Synchronisation of oscilloscope triggers to telescope DAQ
- **Test-beam still ongoing: only preliminary results**

FASTPIX ATTRACT project: test beam



20 x 20 µm^2 matrix
70e threshold

σ = 123 ps



10 x 10 µm^2 matrix
50e threshold

σ = 136 ps

Wafer 18
-6V/-6V pwell/
backside

20x20 µm^2
matrix (left)
70e threshold

10x10 µm^2
matrix (right)
50e threshold

- Timing after timewalk correction on 20µm (left) and 10µm (right) matrix
- Pixel-by-pixel correction for best results, reaching below 200ps resolution
- 10µm matrix is operated at lower threshold with a few Hz noise rate
- Larger cluster sizes for 10µm leads to lower average seed charge and thereby more time walk and makes decoding more difficult

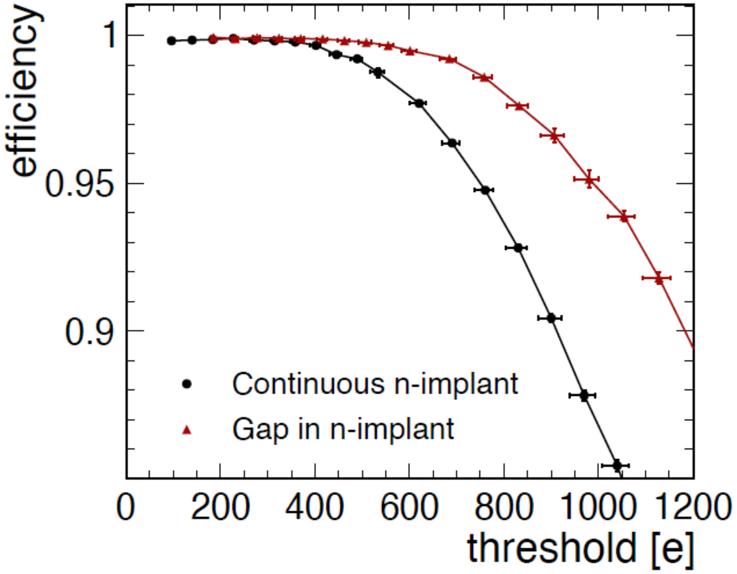
See Eric Buschmann et al. 12th Workshop on Picosecond Timing Detectors for Physics, work in progress !!

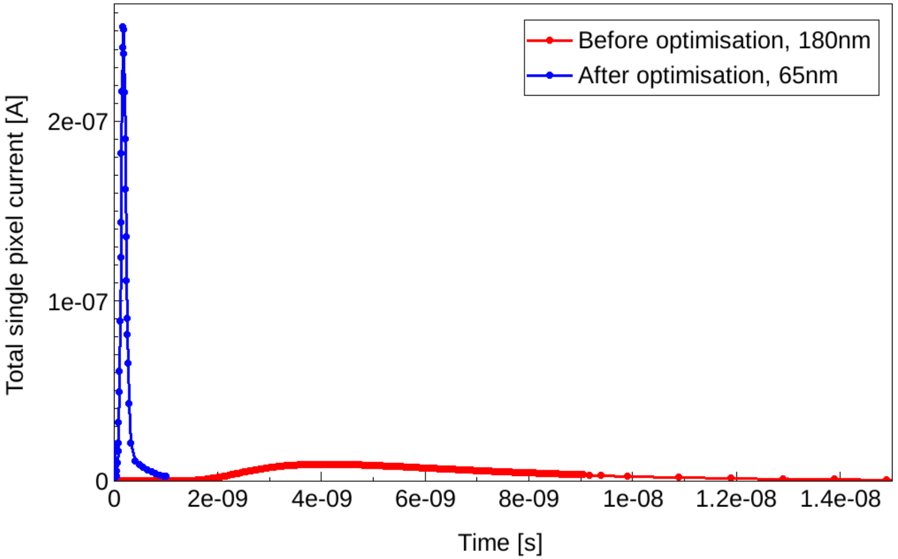
Process optimizations for small collection electrode

Efficiency vs. threshold:

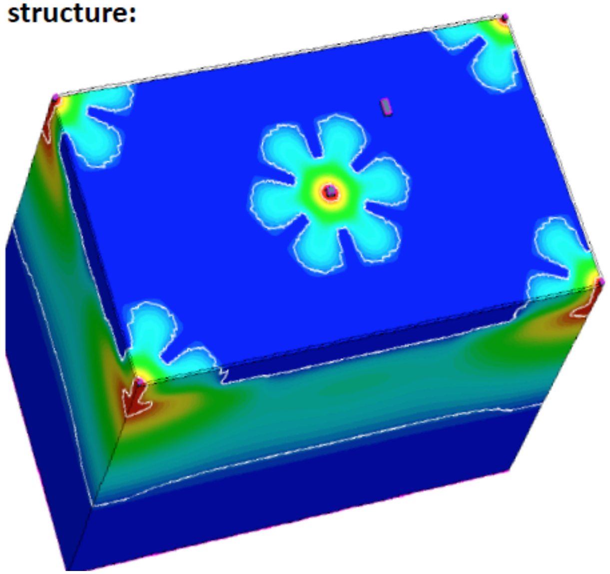
arXiv:2102.04025

~ K. Dort ~





Example of complex 3D TCAD structure:

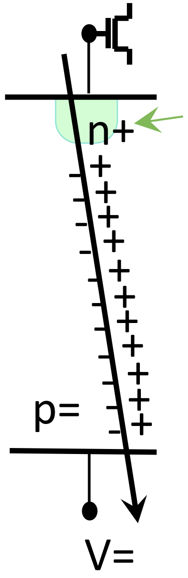


- Efficiency improvement is not only simulated but also measured, even before irradiation (see top left: efficient operating window is almost doubled)
- The optimization over different pixel pitches and flavors, and technologies has improved the timing by several orders of magnitude. Simulations of even more complex structures bring peak-to-peak variations in the order of 50 ps at the moment
- These techniques have now been applied to several chips, and technologies and are generally applicable.

See M. Muenker's CERN EP detector seminar

Power consumption

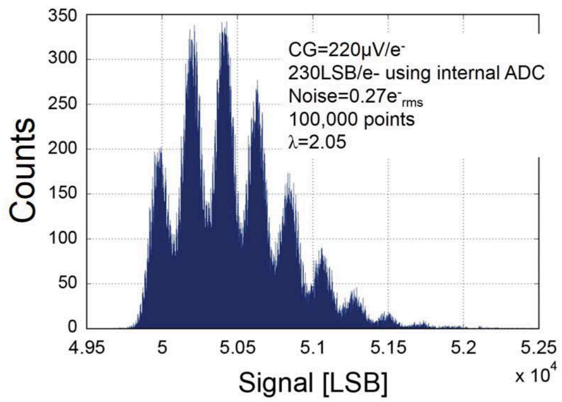
Analog power consumption ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)



$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

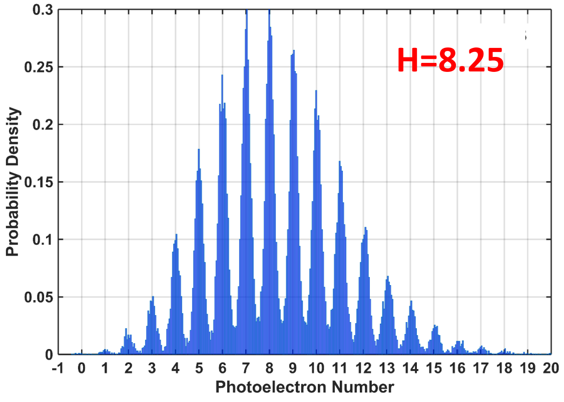
Add connection & circuit

M.W. Seo and S. Kawahito EDL 2015



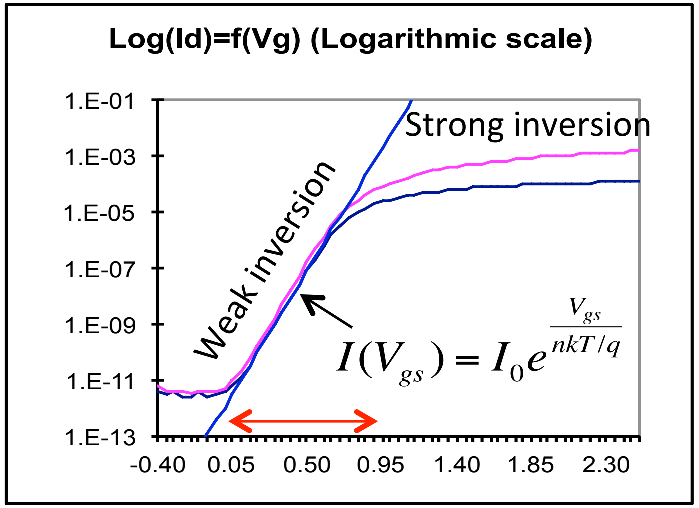
220 μV/e⁻ in 0.11 μm, C=0.73 fF

Ma, Masoodian, Wang, Fossum 2017



350 μV/e⁻ in 45 nm, C=0.46 fF

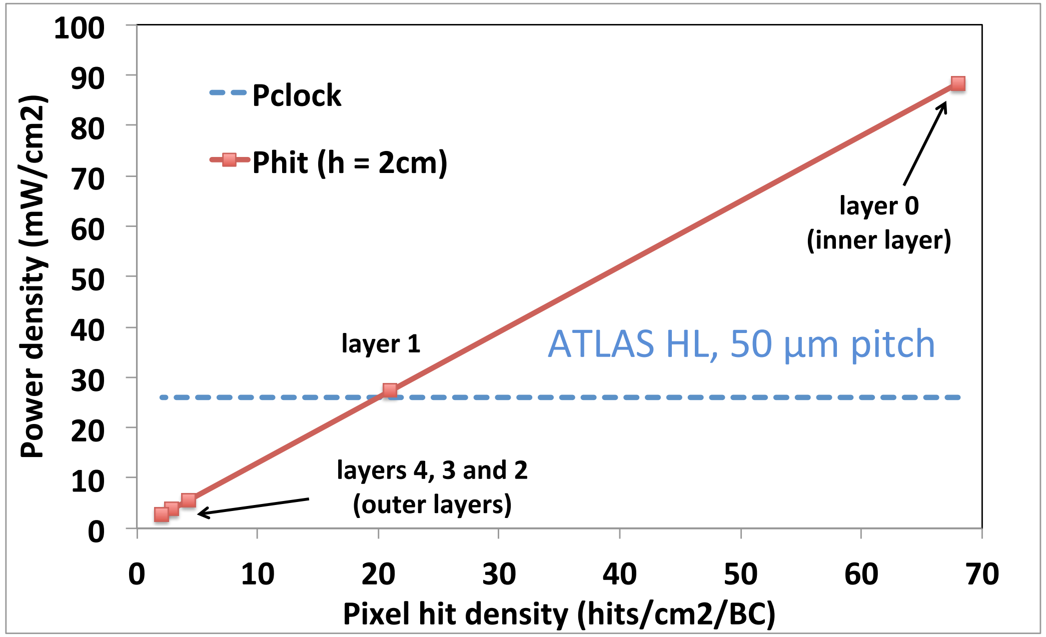
Non-linearity in weak inversion

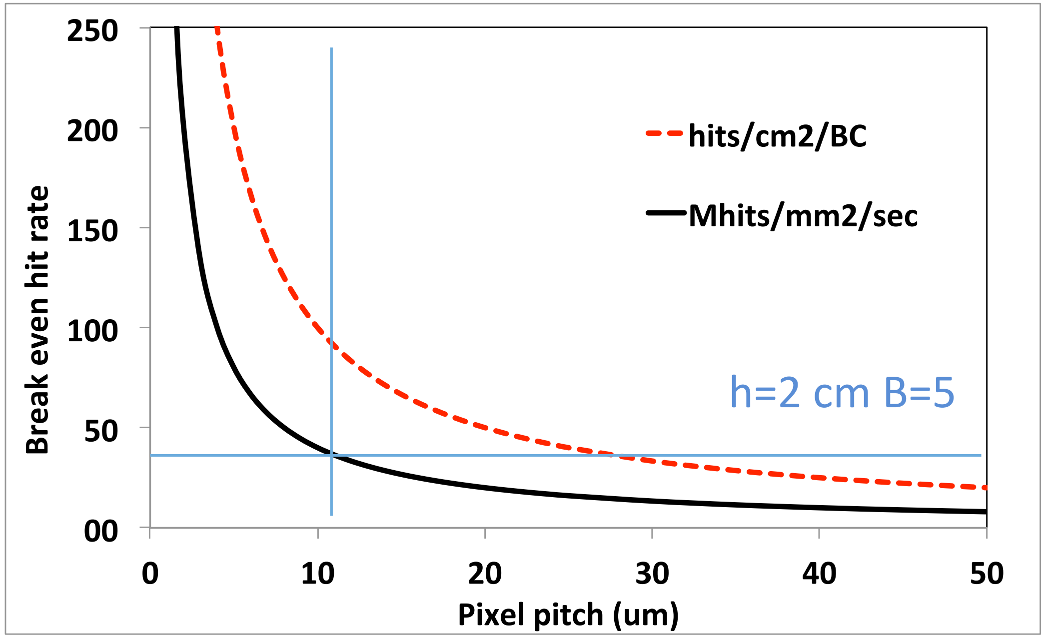


- Q/C several 10's of mV in 180 nm see also Kenji Suzuki's presentation
- "Conventional" approach
  - ITS3 estimate ~ 10-15 nW front end for about 10 mW/cm^2 (ALPIDE in 180nm ~ 40 nW), 5x area reduction
  - Increase power and speed for better timing, μW for < 1 ns F. Piro
- Reduce capacitance further, using:
  - tricks from imaging technology, at present not yet explored
    - now very conventional nwell collection electrode…
    - Still need to extract signal charge from underneath the readout circuit !
  - deeper submicron: 2500 e- to switch inverter in 65 nm, 850 e- in 28 nm, 100 e- in 5 nm A. Marchioro 2019 CERN EP seminar

- Holy Grail: For Q/C > 400 mV, analog power consumption goes to zero.

Digital power consumption





Energy to transfer 1 bit to the periphery (assume line toggle, not step):

1 cm line at 1.8 V = CV^2 = 2 pF x $(1.8\ V)^2$ = **6.5 pJ** Lower VDD in deep submicron = 2 pF x $(1\ V)^2$ = **2 pJ**

Caveat: 2pF/cm can increase depending on line load…

- Defines break-even hit hit rate, where power for the clock = power to transfer hits to the periphery (h is column height, p is pixel pitch, B is number of bits transmitted/hit): $R_{/BC} = (hpB)^{-1}$
- At pitches < 12-13 µm should not distribute the clock over the pixel matrix, even at HL-LHC ATLAS inner pixel, except if extensive clock gating is used
- Break-even decreases with increasing column height but very often rate is lower as well

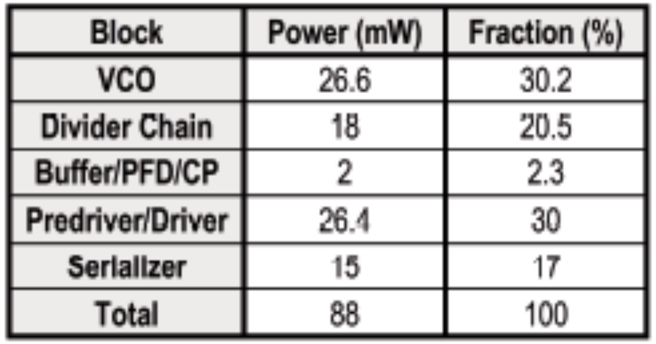
Off-detector transmission:


ISSCC 2013 / SESSION 2 / ULTRA-HIGH-SPEE

2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS

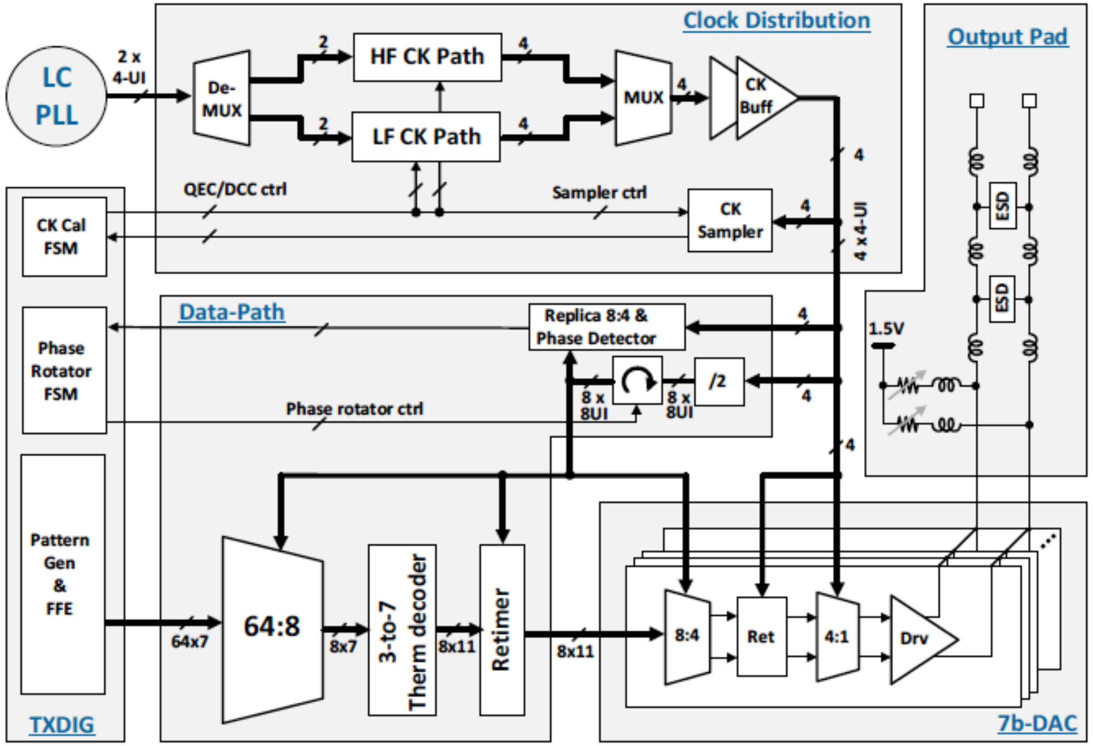
Amr Amin Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang

University of California, Los Angeles, CA



Block	Power (mW)	Fraction (%)
VCO	26.6	30.2
Divider Chain	18	20.5
Buffer/PFD/CP	2	2.3
Predriver/Driver	26.4	30
Serializer	15	17
Total	88	100

INTEL, ISSCC2021, 224Gbps, PAM-4, 1.7 pJ/bit, 10 nm technology



State of the art: a few mW/Gbps, already earlier but also now at much higher bandwidths

Significant circuit complexity

For HEP important penalty for SEU robustness due to triplication/larger devices…

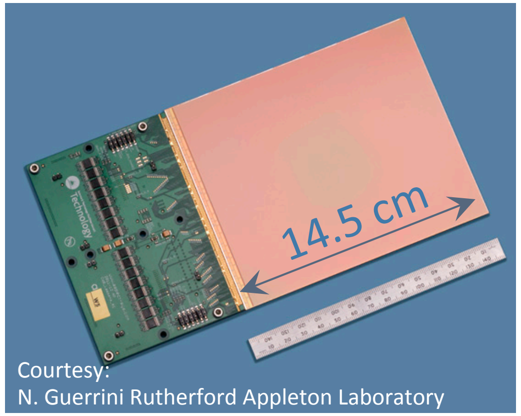
Timepix 30 mW 10Gb/s transmitter in TSMC 65nm (designed by NIKHEF) 3pJ/bit approaches state of the art

Important: data concentration, physical volume for material budget, and technology

Stitching and bending

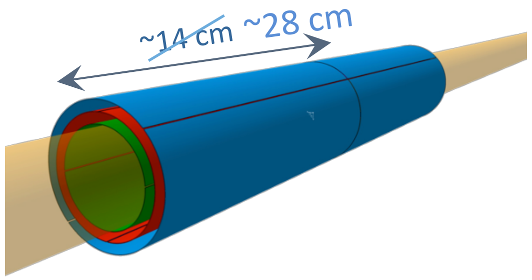
Stitching for better integration, lower mass and constructing larger areas

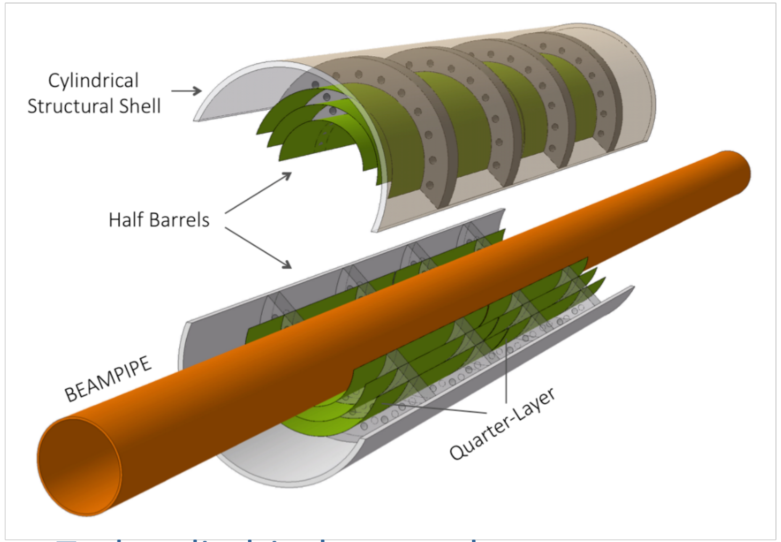
Exploiting flexible nature of thin silicon and stitching



Courtesy:
N. Guerrini Rutherford Appleton Laboratory

20 µm thick wafer
(Silicon Genesis)





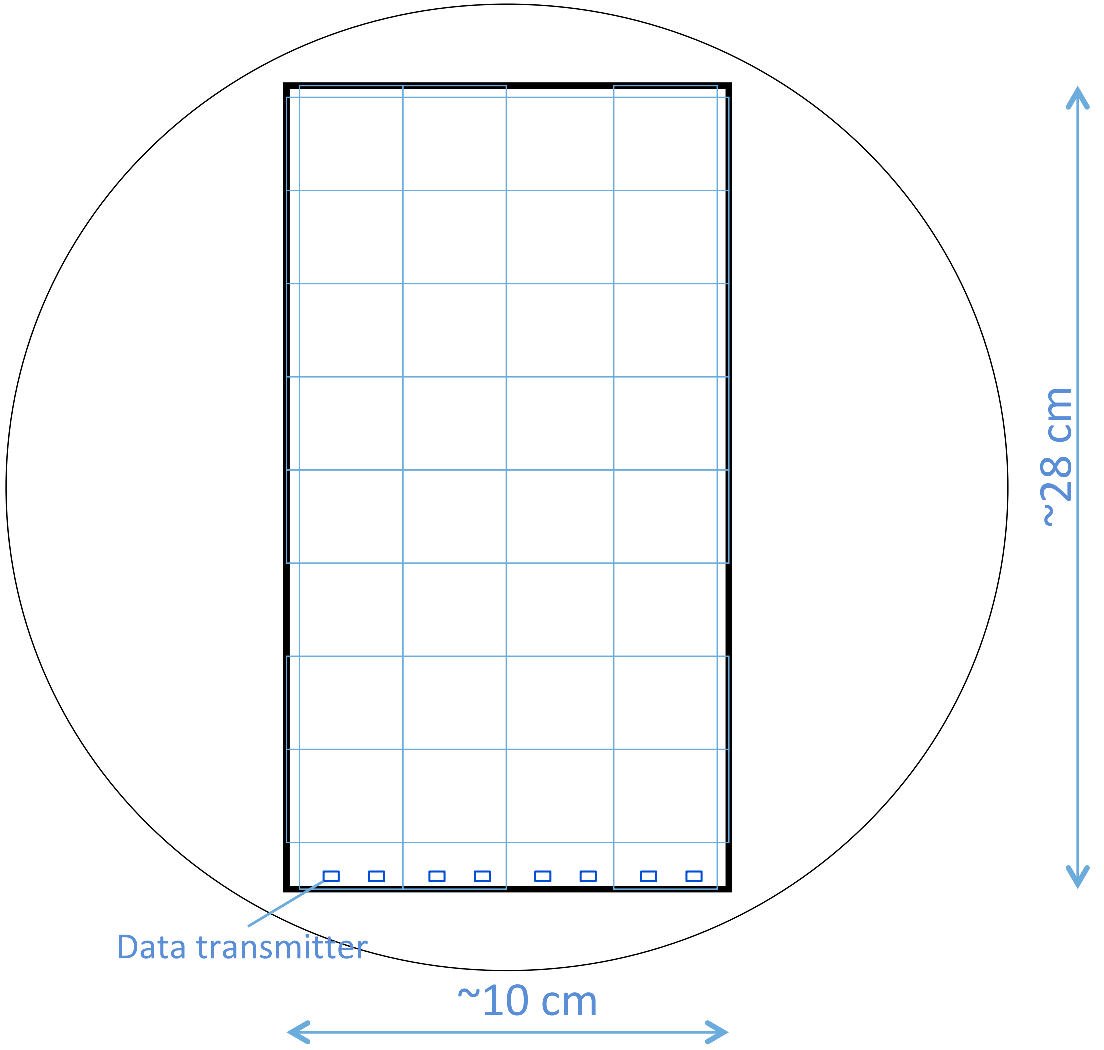
Truly cylindrical vertex detector
New ultra light barrel in LS3 0.05% X/X0 per layer
ALICE-PUBLIC-2018-013

Motivated by lower material budget

Of general interest to cover large areas
Stitching details and bending tool

Work under the assumption of a wafer-scale sensor, ~28 x 10 cm^2, to be revised if needed

Power budget ~ 20 mW/cm^2 for ~2.5 Mhit/cm^2/s



Stitched sensor: challenges

Power consumption: for 10 µm x 10 µm pixel 1nA/pixel = 1 mW/cm^2

Dynamic hit-rate related power density proportional to column height and hit rate

- Dynamic hit-rate related power density proportional to column height and hit rate
- Avoid distribution of a clock over the matrix (150 – 200 mW/cm^2 for 40 MHz)
- Static leakage not negligible at all, analog power determined by sensor Q/C (slow front end ~10-20 nA)

Power distribution:

- Limit and contain voltage drop
- Power regulation for uniformity
- Beyond 50 mW/cm^2 :
  - Power pads no longer only at the bottom, or
  - on-chip serial powering,

    interesting even for lower hit rates, for a single point connection of power/data/slow control

    1mW/cm^2 corresponds to 280 mA…

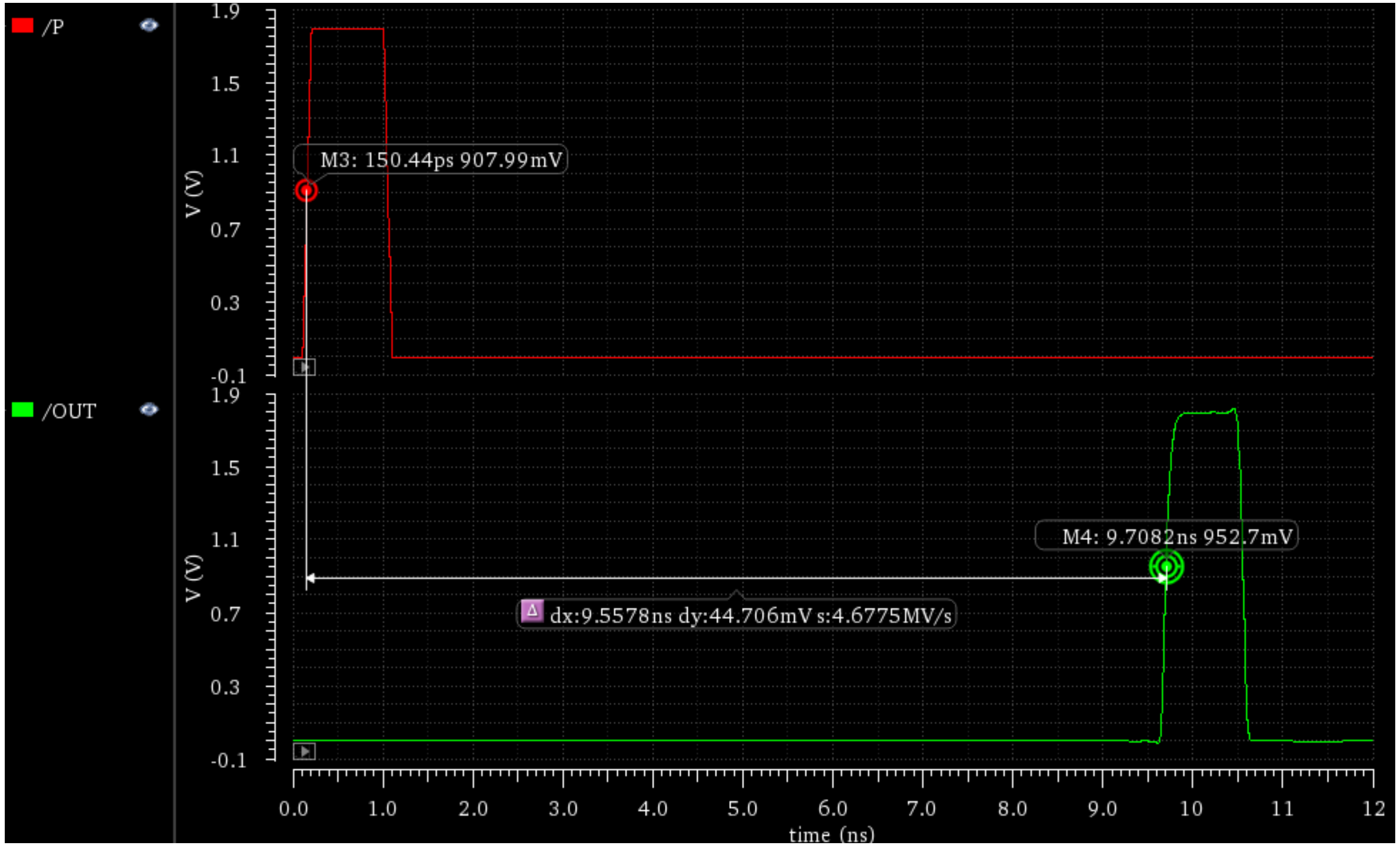
Yield:

- Conservative stitching rules represent a significant area penalty, need to find ways to regain density
- Power regulation for uniformity but also segmented with current limitation to protect against shorts

Very large chip:

- One column ~ 2^{14} pixels, extract hit info with limited number of lines
- Need digital on-top design and verification

Stitched sensor challenges: timing and data bandwidth



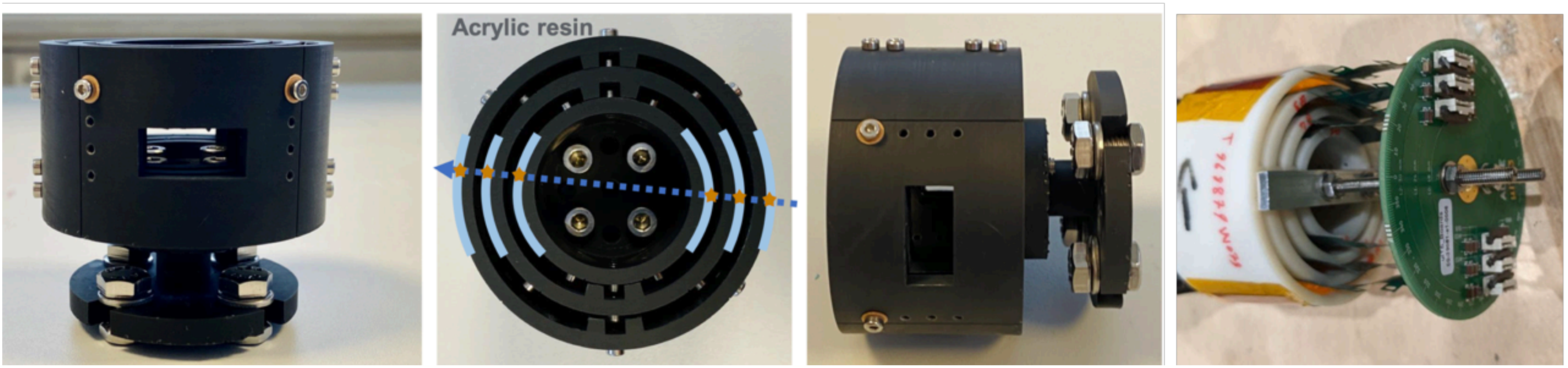
- Monte Carlo simulation of 90 buffer stages
- Timing information maintained:
  - < 10 ps rms (mismatch) variation
  - jitter < 500 fs rms
- For very large matrix more than 90 buffer stages, ~3 x worse…
- Here 1ns pulse width, can decrease to 0.5 ns -> HUGE matrix bandwidth to be matched by periphery and off-chip data transmission
- Machinery to transmit timing information to the periphery available
- To be verified: process – power supply – temperature effects !

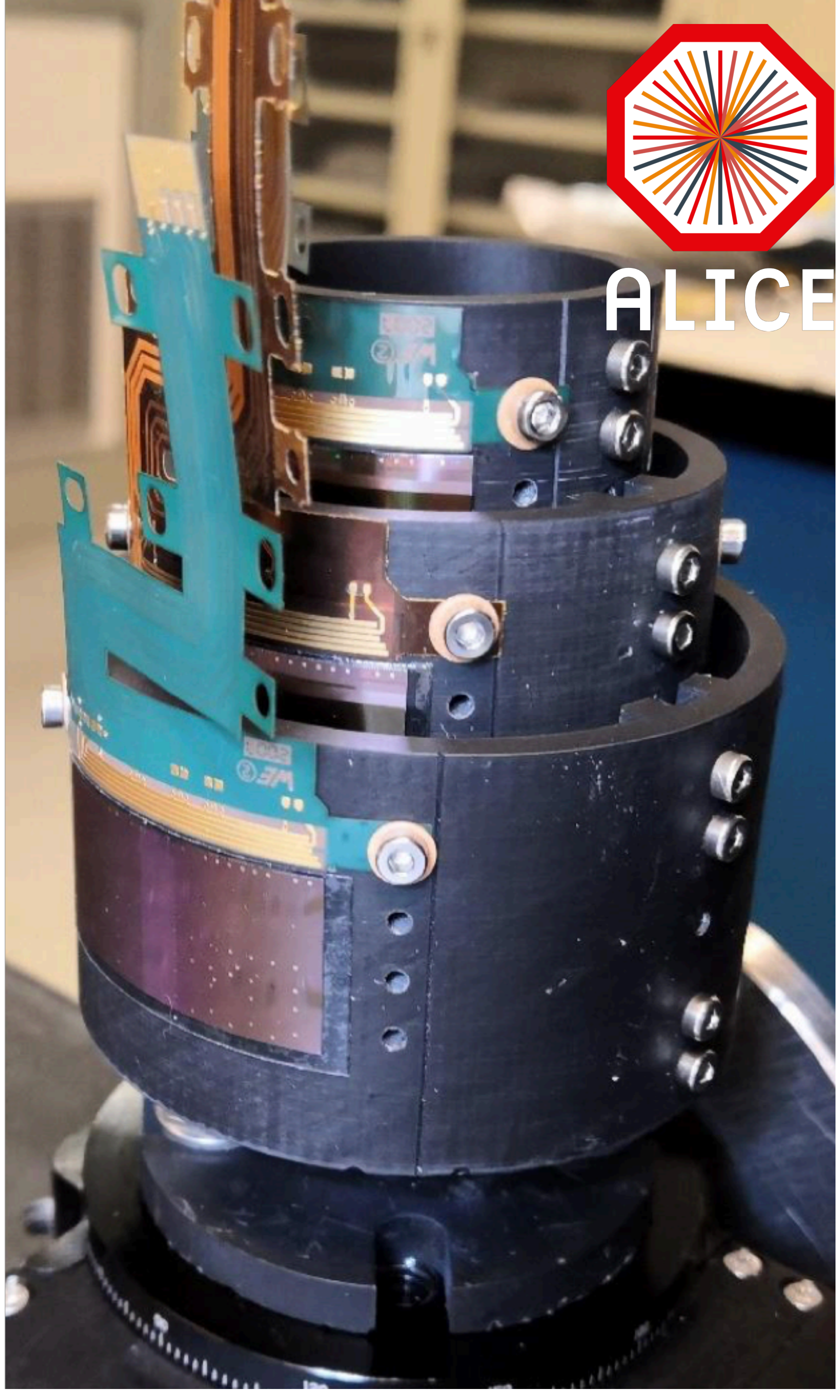
If these challenges can be overcome for a wafer-scale sensor with good yield, we prove we can build modules with single wafer-scale chips and unprecedented integration for large area detectors which would be a major step forward.

R&D thinning and bending MAPS (ALICE, slides courtesy Magnus Mager)

Bent ALPIDEs

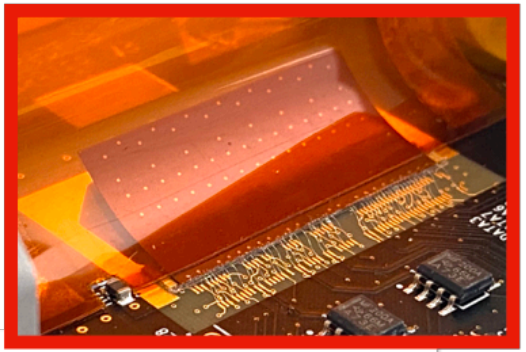
- A number of prototypes with bent ALPIDEs were produced
  - several different ways were explored (bending before bonding, or vice versa, different jigs)
  - “feeling” for handling thin silicon was gained
- By now, we have a full mock-up of the final ITS3, called “µITS3”
  - 6 ALPIDE chips, bent to the target radii of ITS3





Beam tests

1st paper: arxiv:2105.13000



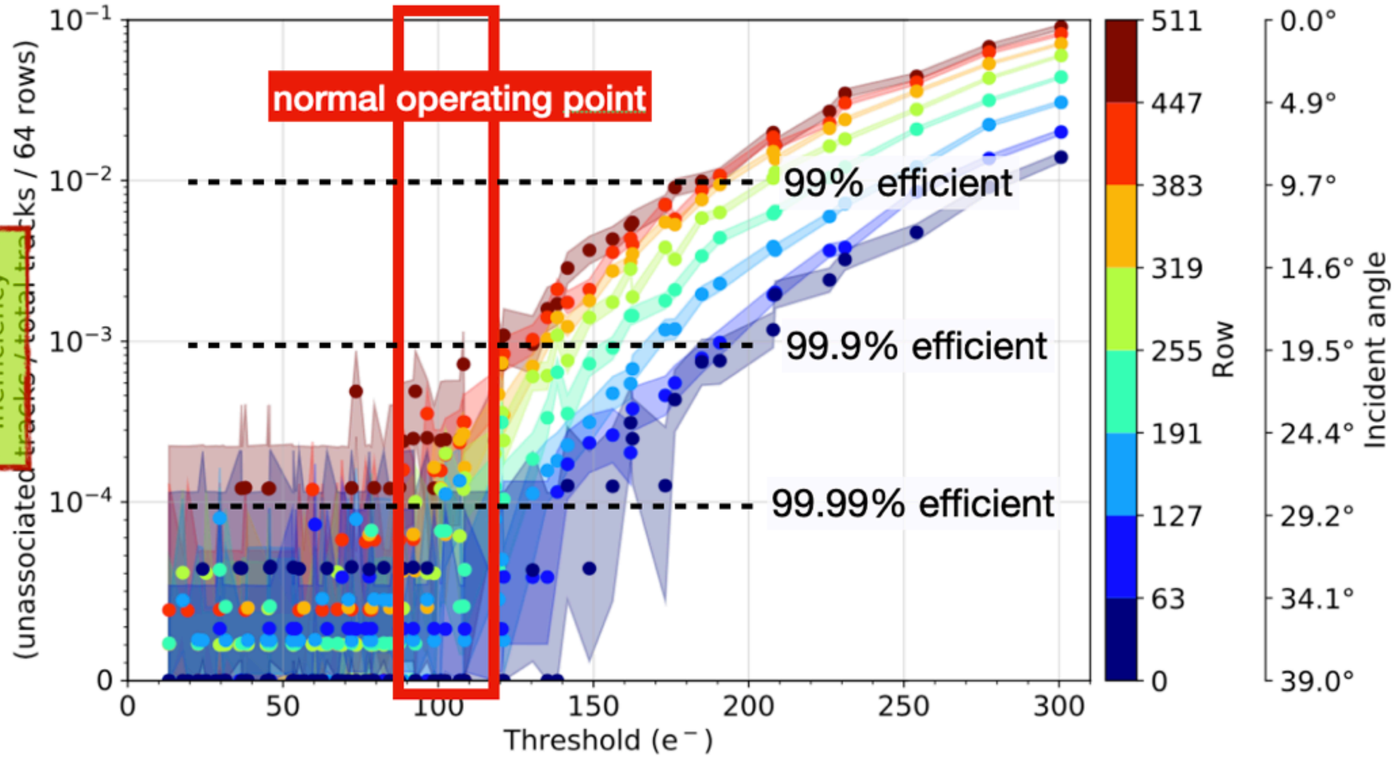


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

First demonstration of in-beam performance of b
Monolithic Active Pixel Sensors

ALICE ITS3

[a] *European Organization for Nuclear Research (CERN), Geneva, Switzerla*
[b] *GSI, Darmstadt, Germany*
[c] *Heidelberg University, Heidelberg, Germany*
[d] *INFN & University of Trieste, Trieste, Italy*

Abstract

A novel approach for designing the next generation of vertex detectors foresees to employ wafer-scale sensors that can be bent to truly cylindrical geometries after thinning them to thicknesses of 20-40 µm. To solidify this concept, the feasibility of operating bent MAPS was demonstrated using 1.5 cm × 3 cm ALPIDE chips. Already with their thickness of 50 µm, they can be successfully bent to radii of about 2 cm without any signs of mechanical or electrical damage. During a subsequent characterisation using a 5.4 GeV electron beam, it was further confirmed that they preserve their full electrical functionality as well as particle detection performance.

In this article, the bending procedure and the setup used for characterisation are detailed. Furthermore, the analysis of the beam test, including the measurement of the detection efficiency as a function of beam position and local inclination angle, is discussed. The results show that the sensors maintain their excellent performance after bending to radii of 2 cm, with detection efficiencies above 99.9 % at typical operating conditions, paving the way towards a new class of detectors with unprecedented low material budget and ideal geometrical properties.

Keywords: Monolithic Active Pixel Sensors, Solid state detectors, Bent sensors

1. Introduction

The precision of barrel vertex detectors is mainly determined by three contributions: their radial distance to the interaction point, their material budget, and their intrinsic sensor resolution. In order to achieve hermiticity, they are typically built out of detector staves placed in layers around the beam pipe. This arrangement effectively sets a practical limit on the first two factors. ALICE,

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*Corresponding author

Preprint submitted to Nucl. Instrum. Methods Phys. Res. A *February 22, 2021*

Clearly proving that bent MAPS are working!

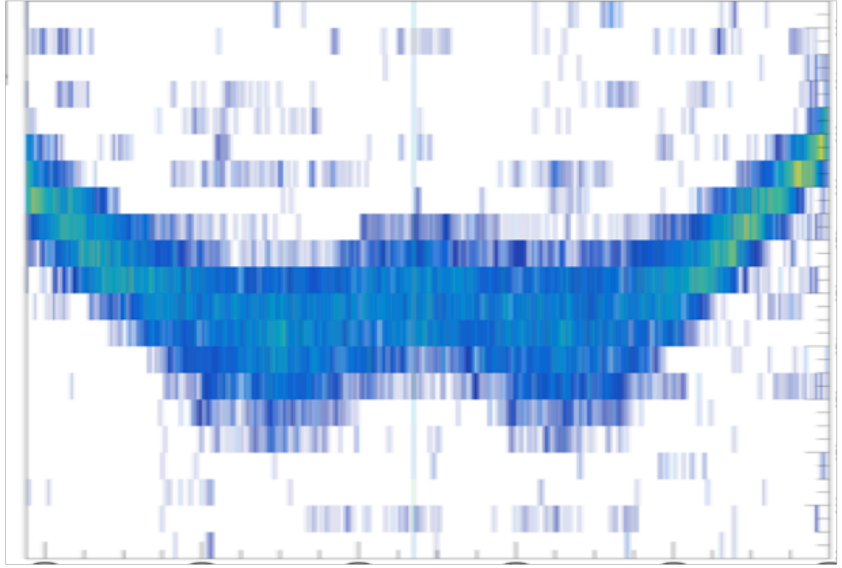
Beam tests

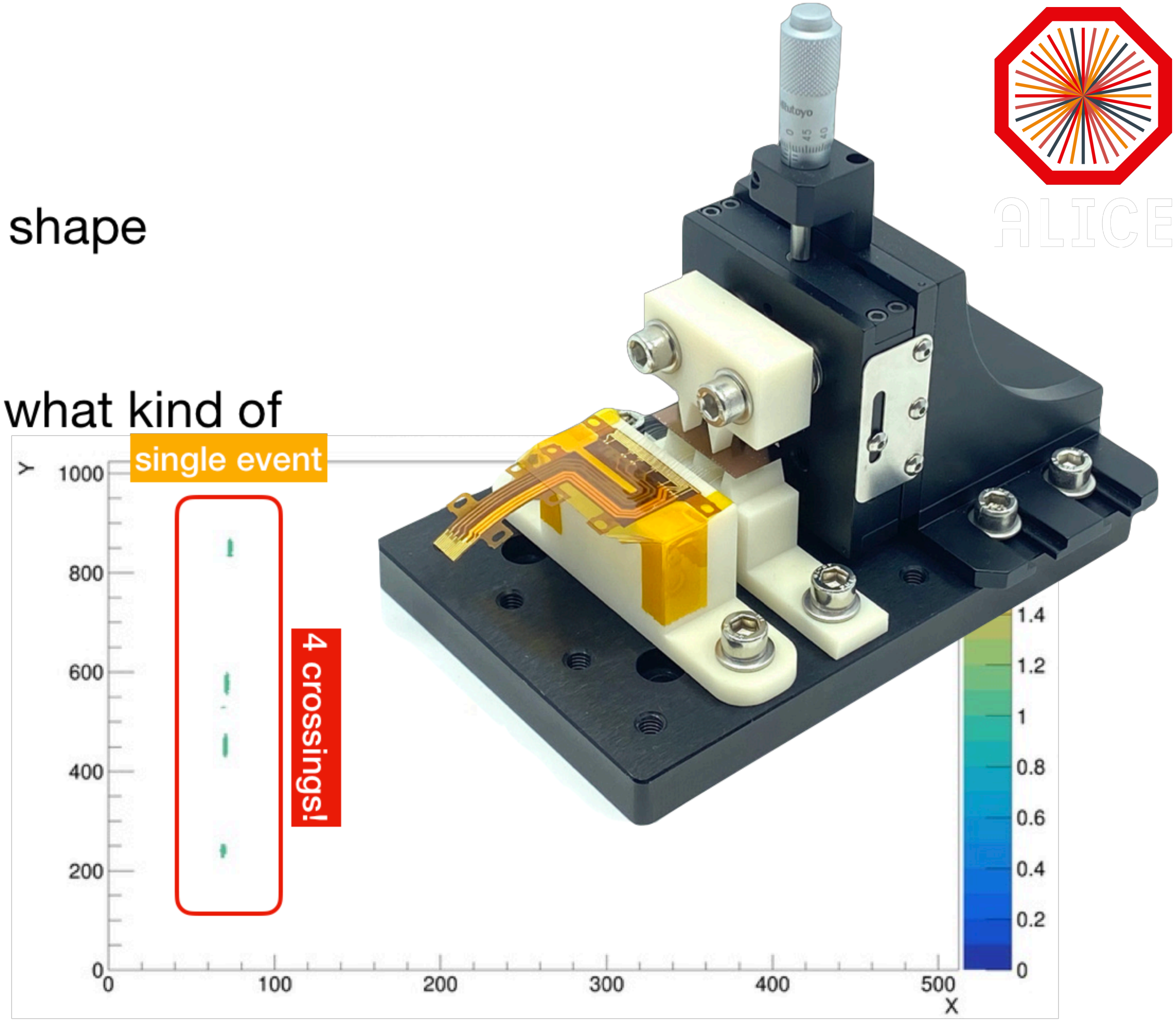
“curiosity”

- ~~W~~ (won): ALPIDE bent into a “W” shape
  - bending radii of O(2cm)

- Also “just works”, demonstrating what kind of detectors become possible now

correlation of flat and W chip





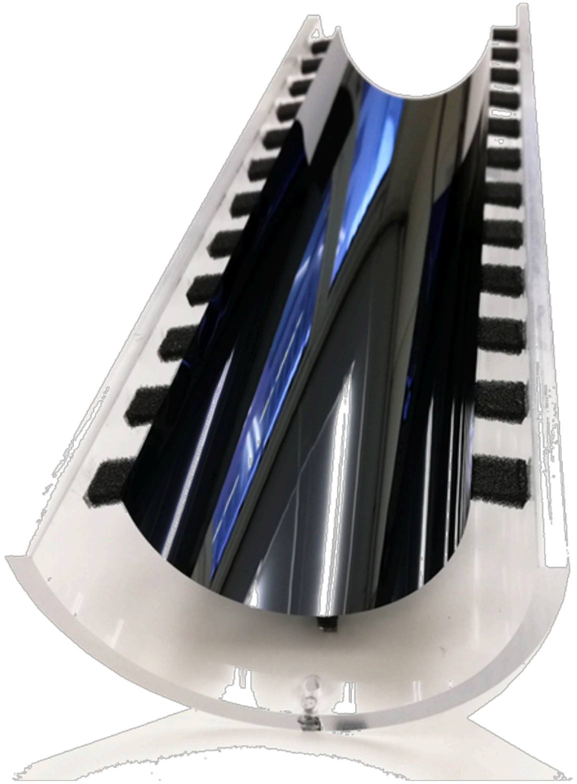
single event

4 crossings!

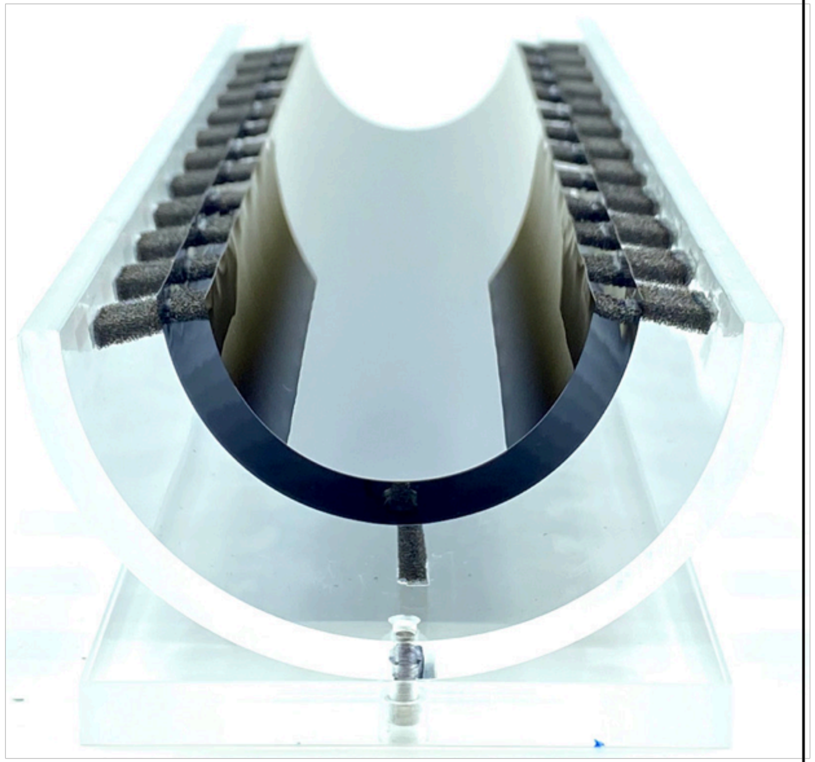
This technology has a lot more to offer – time to be creative!

Layer assembly

Layer 2



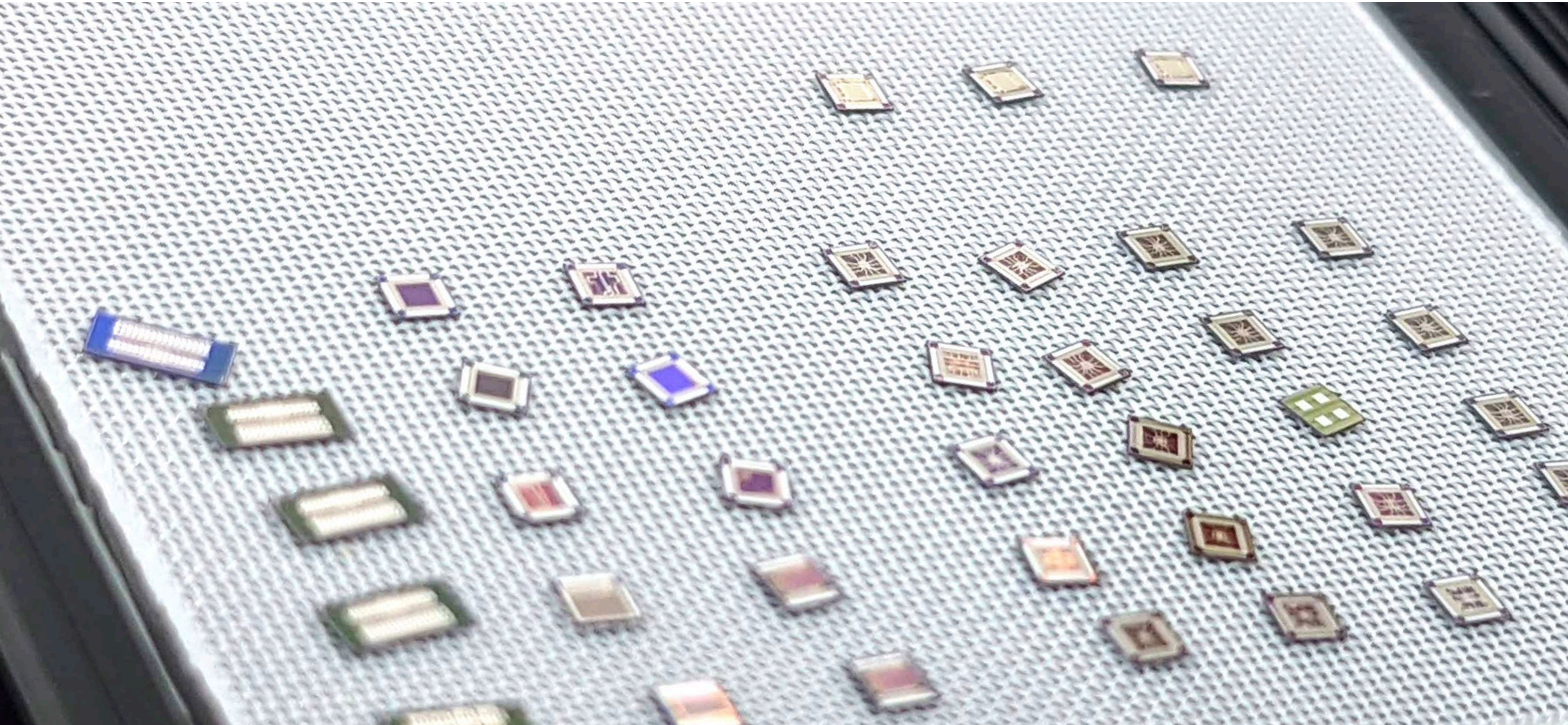
Layers 2+1



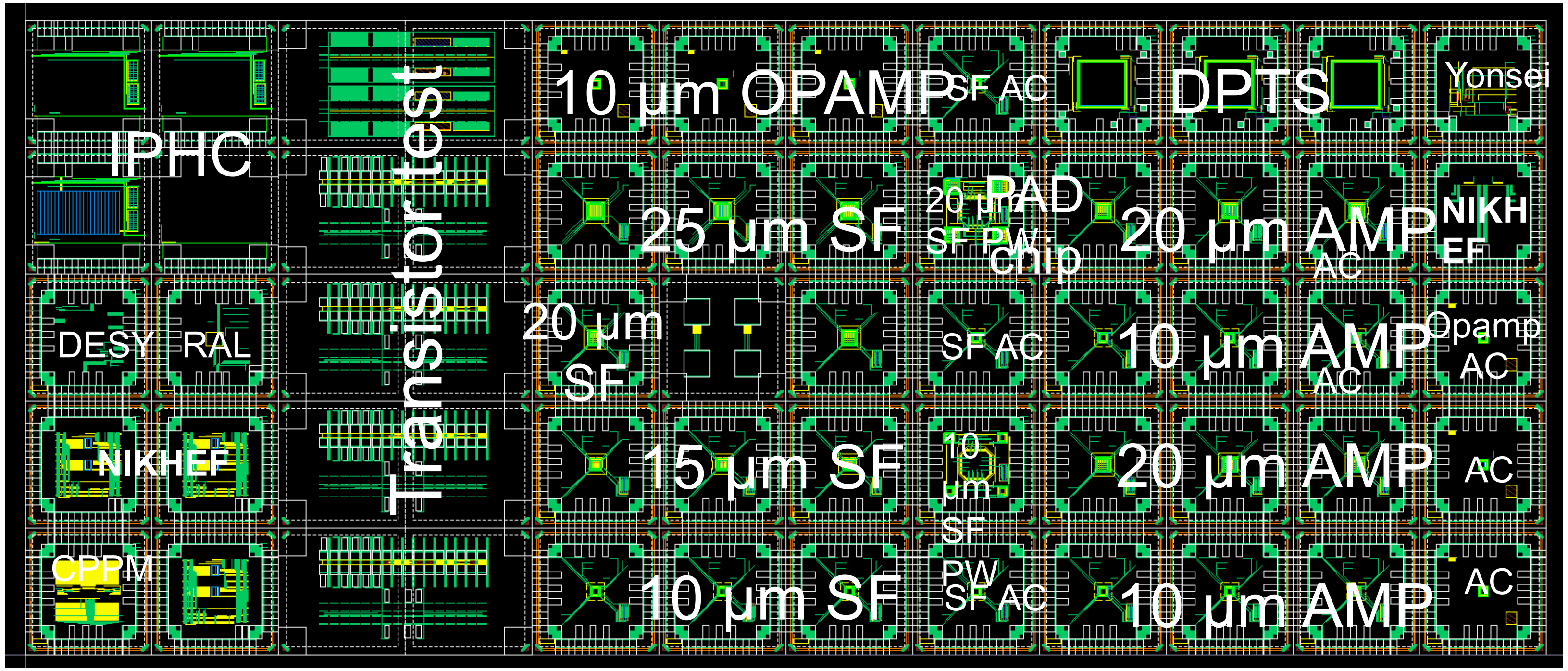
Layers 2+1+0

3-layer integration successful!

CERN EP R&D WP1.2 65 nm ISC TPSCo development

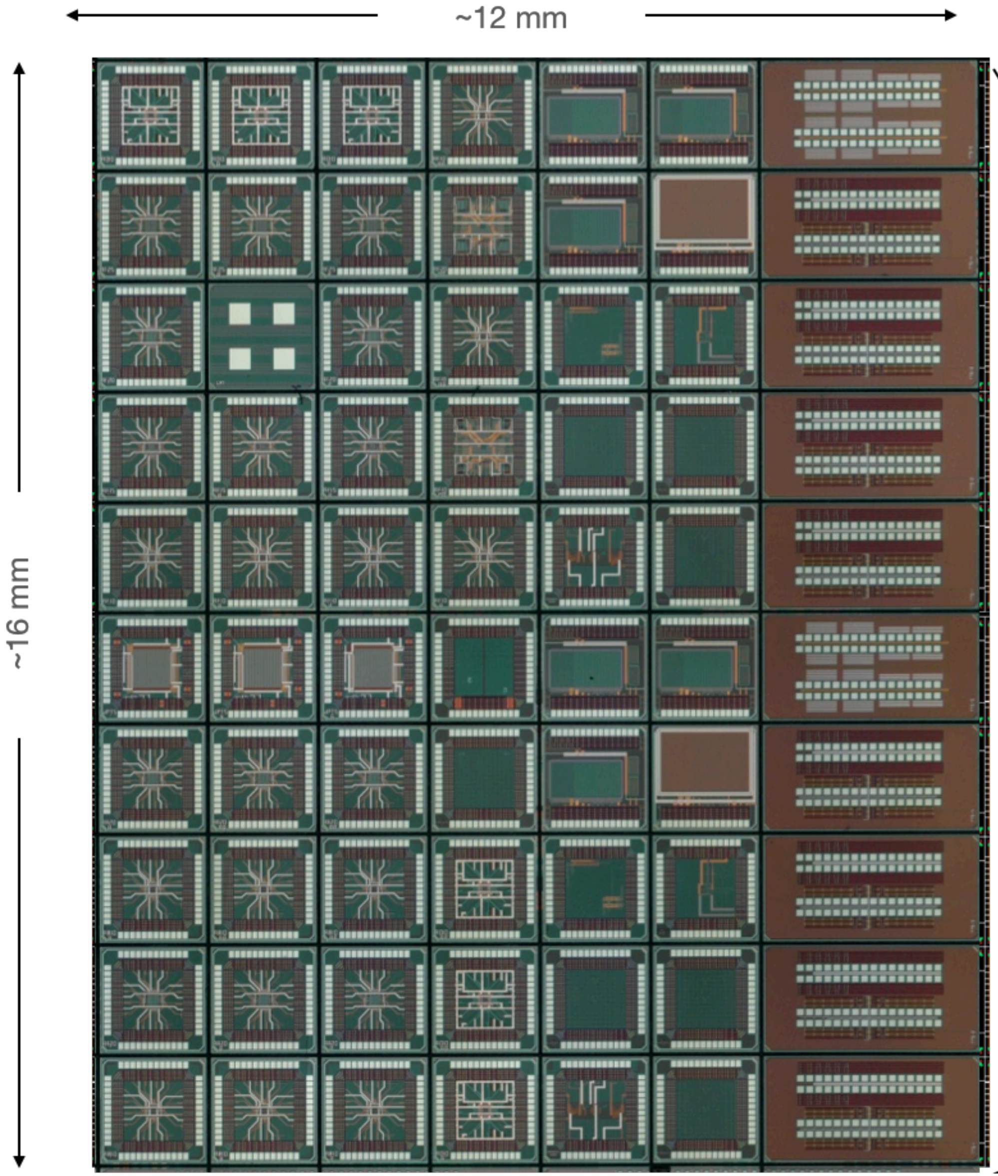


MLR1 submission, first results becoming available

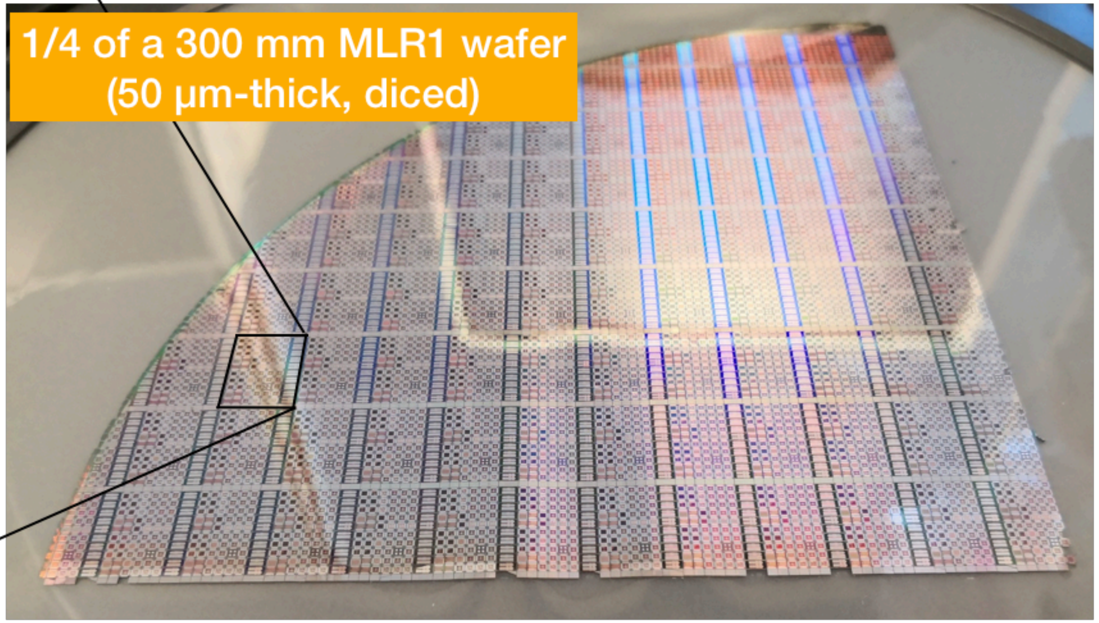


- IPHC: rolling shutter larger matrices, DESY: pixel test structure (using charge amplifier with Krummenacher feedback, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures
- Significant effort from participating institutes, also financially, and of the ALICE experiment also on test
- Transistor test structures, analog pixel (4x4 matrix) test matrices in several versions (in collaboration with IPHC with special amplifier), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.
- Converged with 4 splits of 3 wafers, back from foundry beginning of June
- Process modifications even more needed due to thinner epitaxial layer

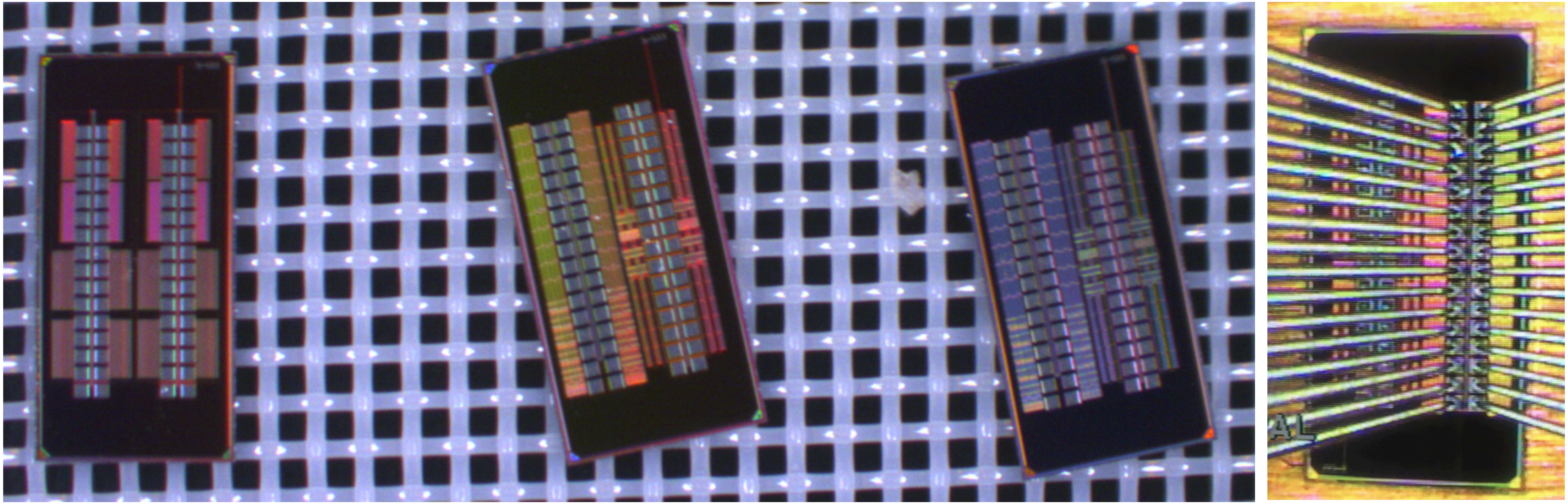
R&D 65 nm ISC TPSCo development



- Fully processed wafers are back by now
- Plenty of material ready for testing, literarily thousands of chips
- Produced with 4 different process splits
  - TCAD-guided optimisations in collaboration with foundry, comparable to TJ180nm


1/4 of a 300 mm MLR1 wafer (50 µm-thick, diced)

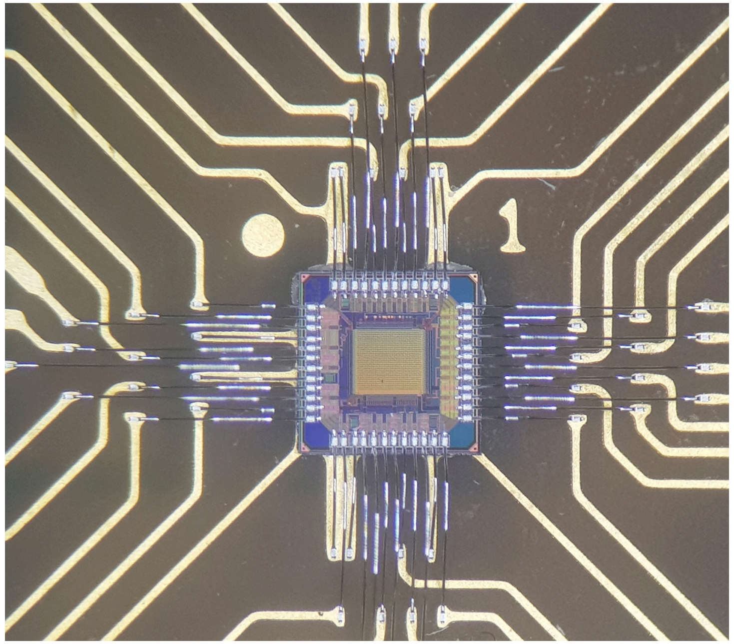
65 nm transistor prototypes

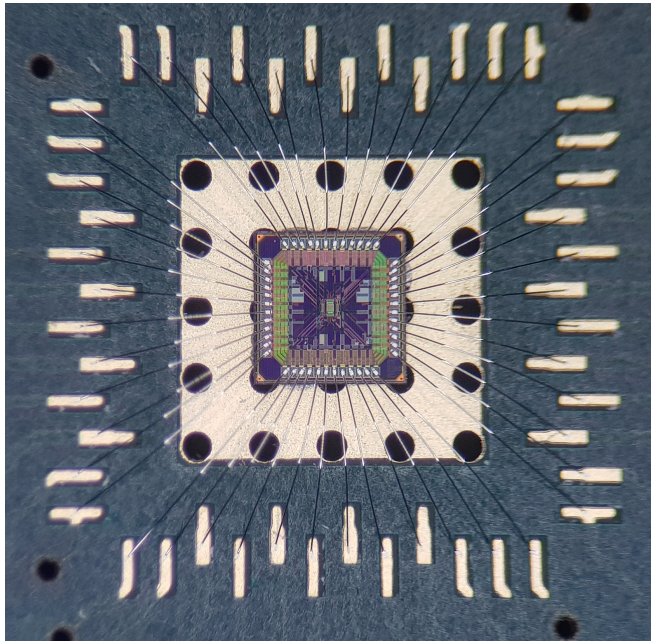


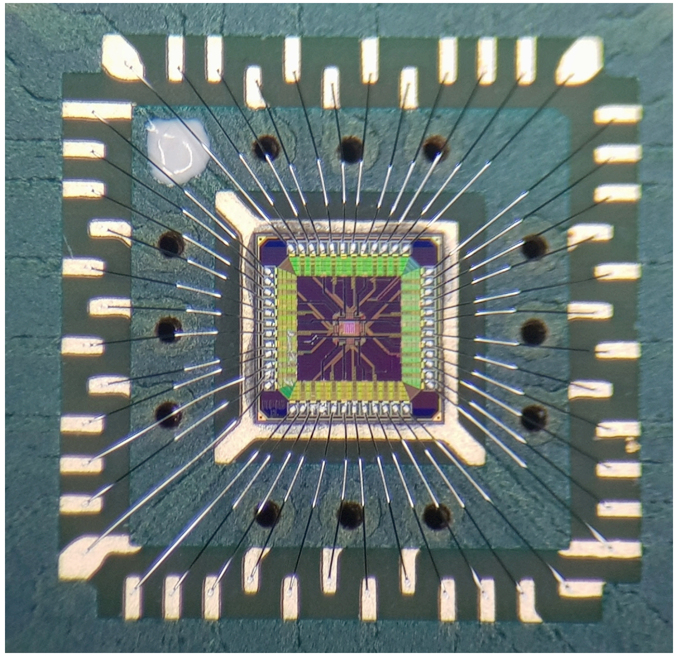
- Compatible with existing test system based on probe card.
- Tests have started
  - No apparent show stoppers so far, very encouraging results
  - Detailed analysis ongoing and in discussion with the foundry

PIXEL TEST CHIPS

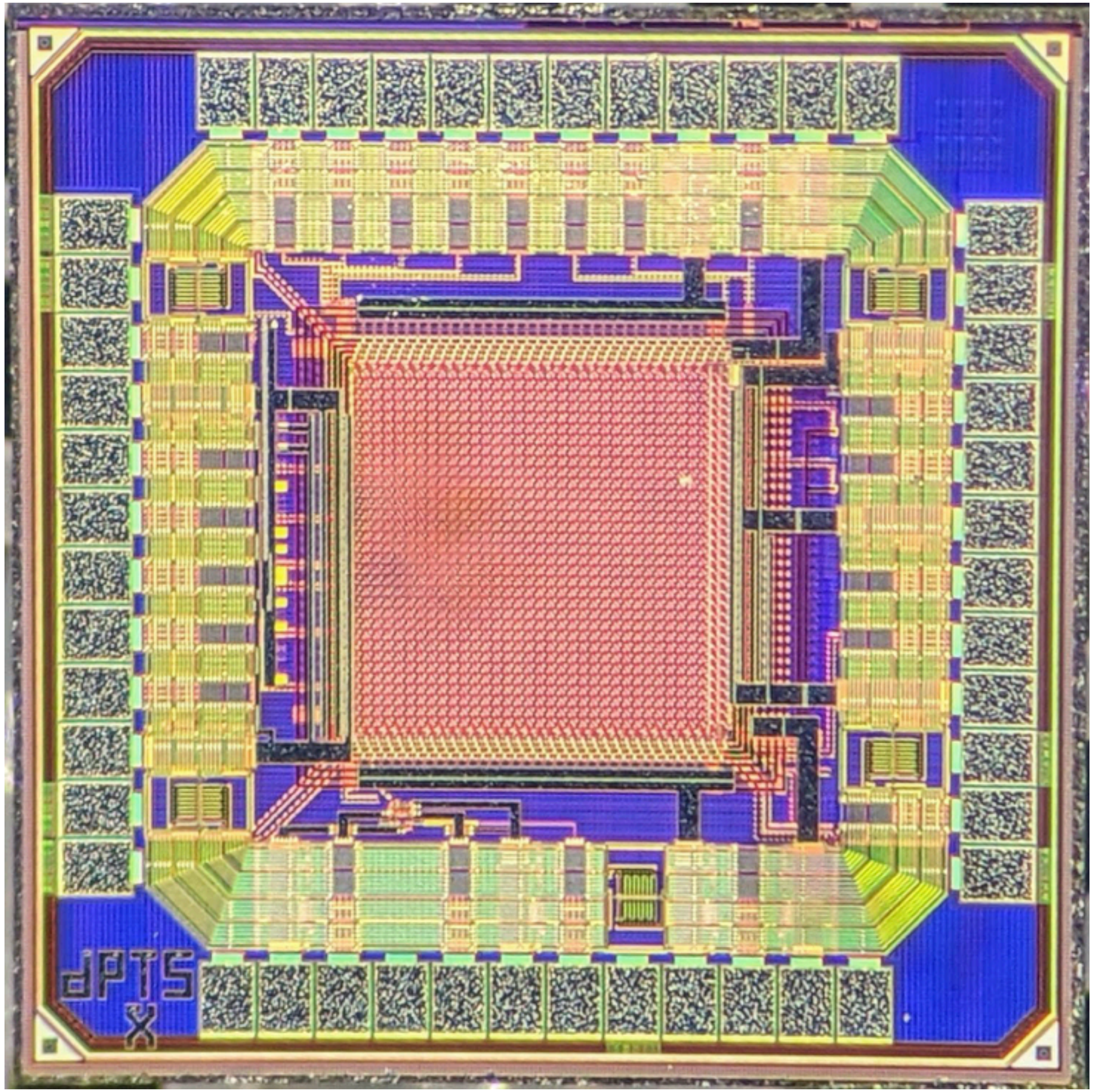
- Several flavors of analog and digital pixel test structures
- Designs were optimised with extensive device (TCAD) simulation with excellent foundry support
- Chips on carriers just became available in the lab some 4 weeks ago
- Setups are being prepared by several groups, first results are coming in





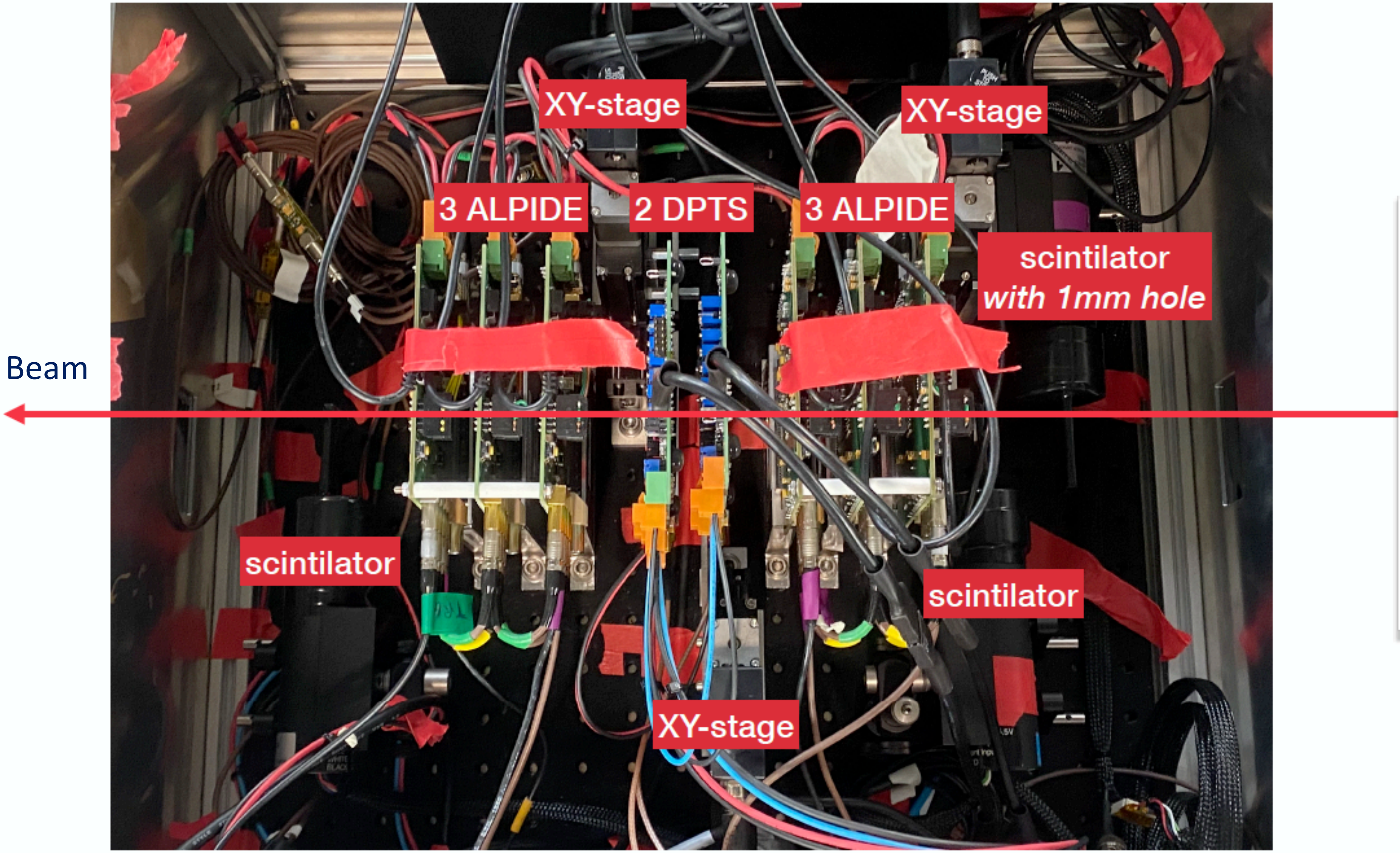


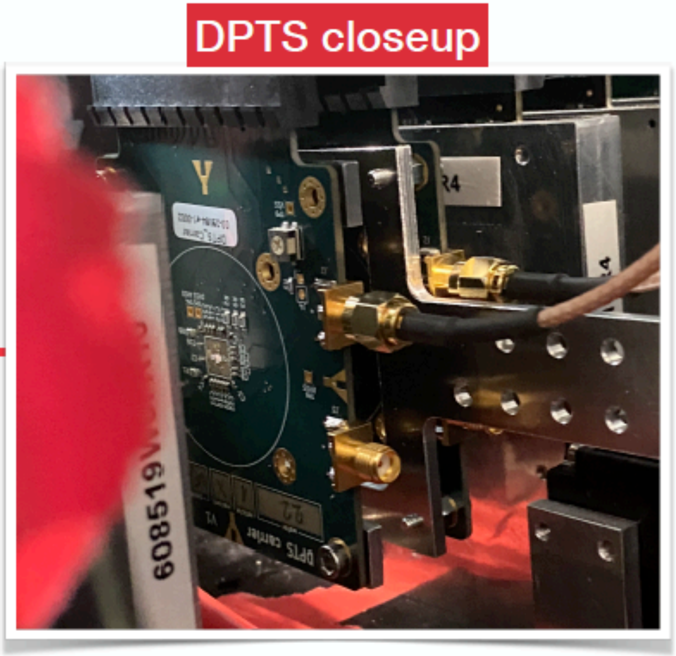
Digital Pixel Test Structure (DPTS)



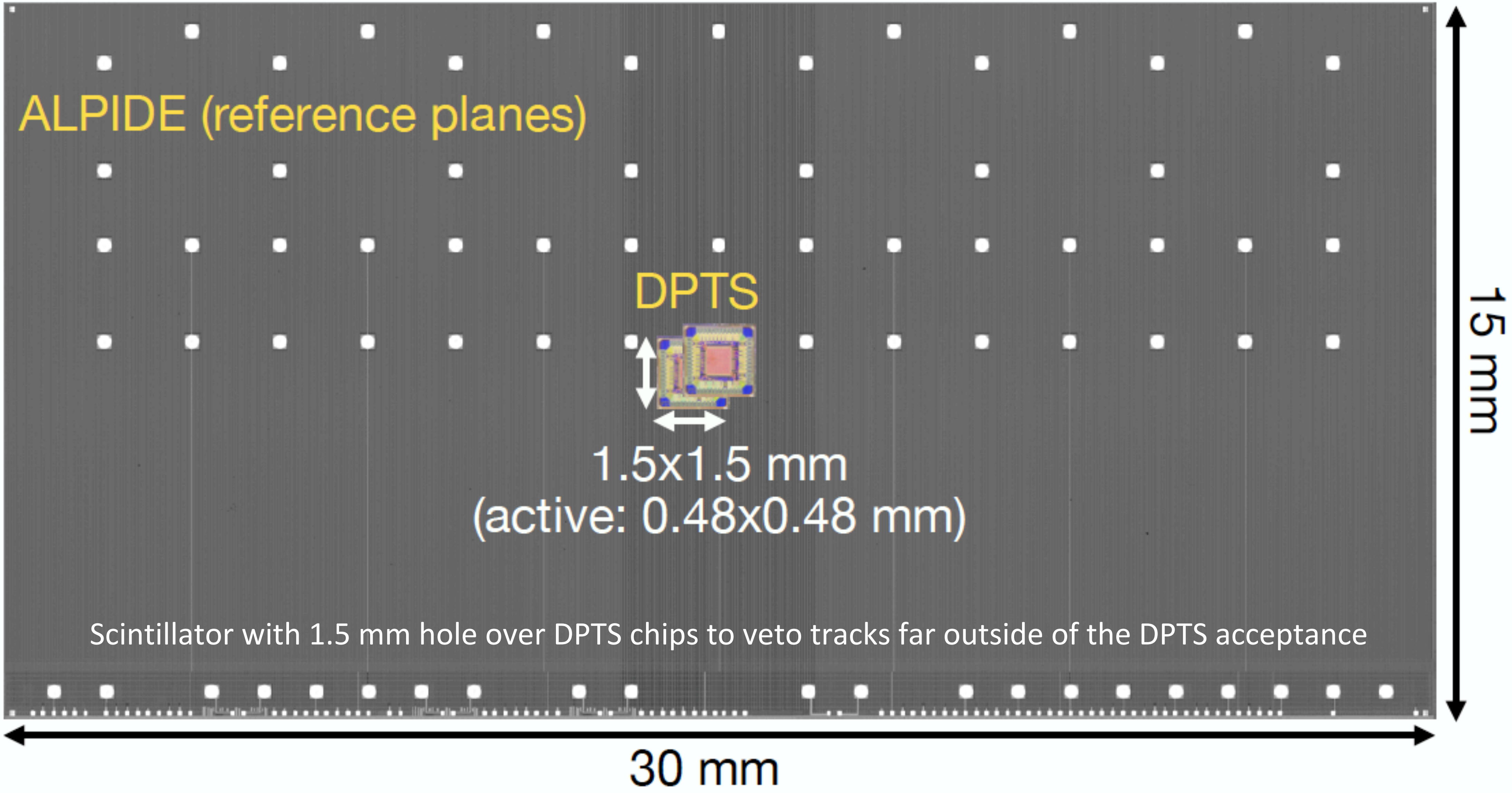
- Most “aggressive” chip in MLR1
- 1.5 mm x 1.5 mm test chip
- 32 x 32 pixels 15 µm pitch
- Asynchronous digital readout with Time-over-Threshold (TOT) information
- Allows verification of
  - Sensor *and* Front-end performance
  - Basic digital building blocks
  - SEU cross-sections of registers

First test beam setup
(electron beam of a few GeV/c)



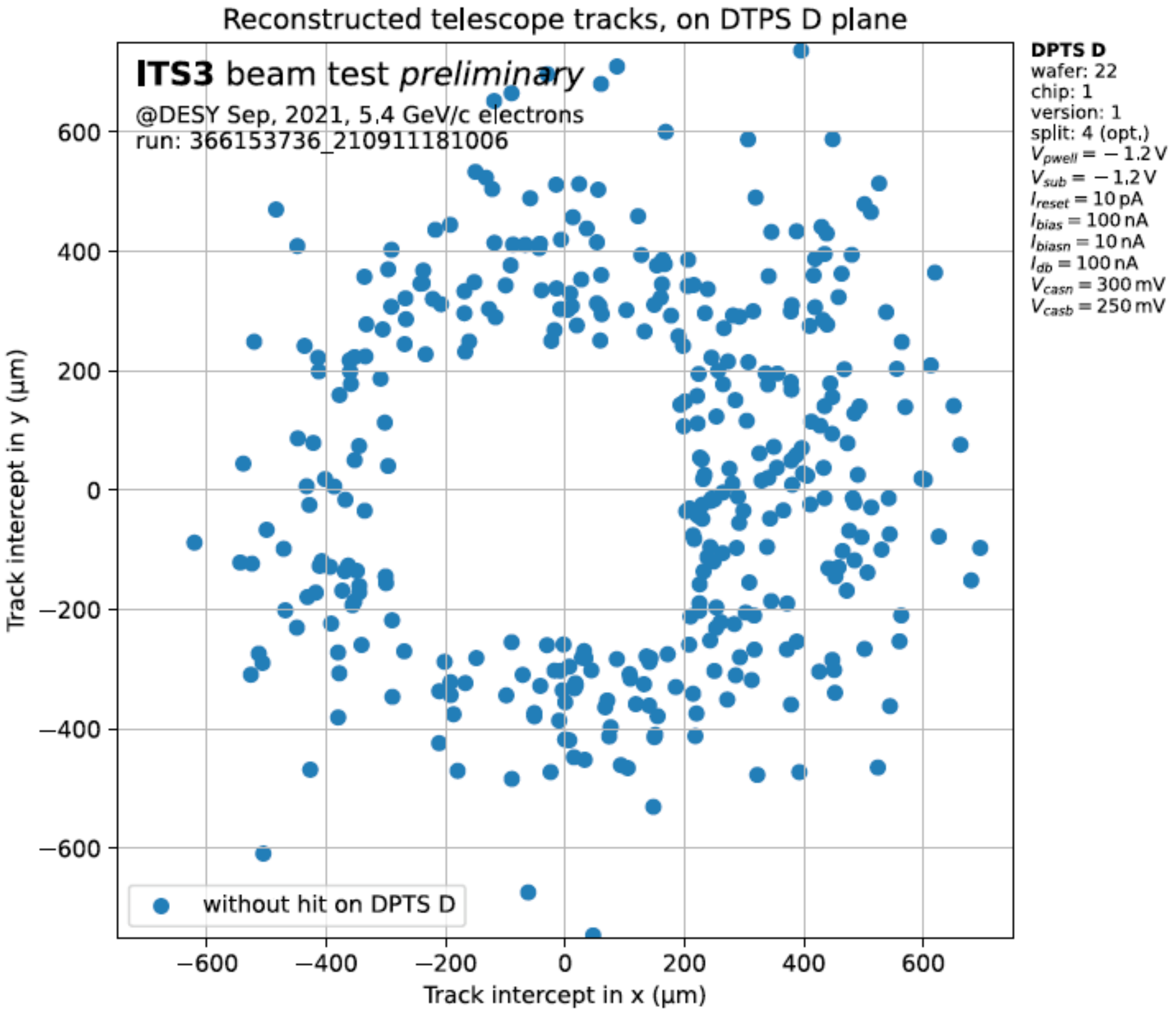


DPTS beam test results (by ALICE measurement team)



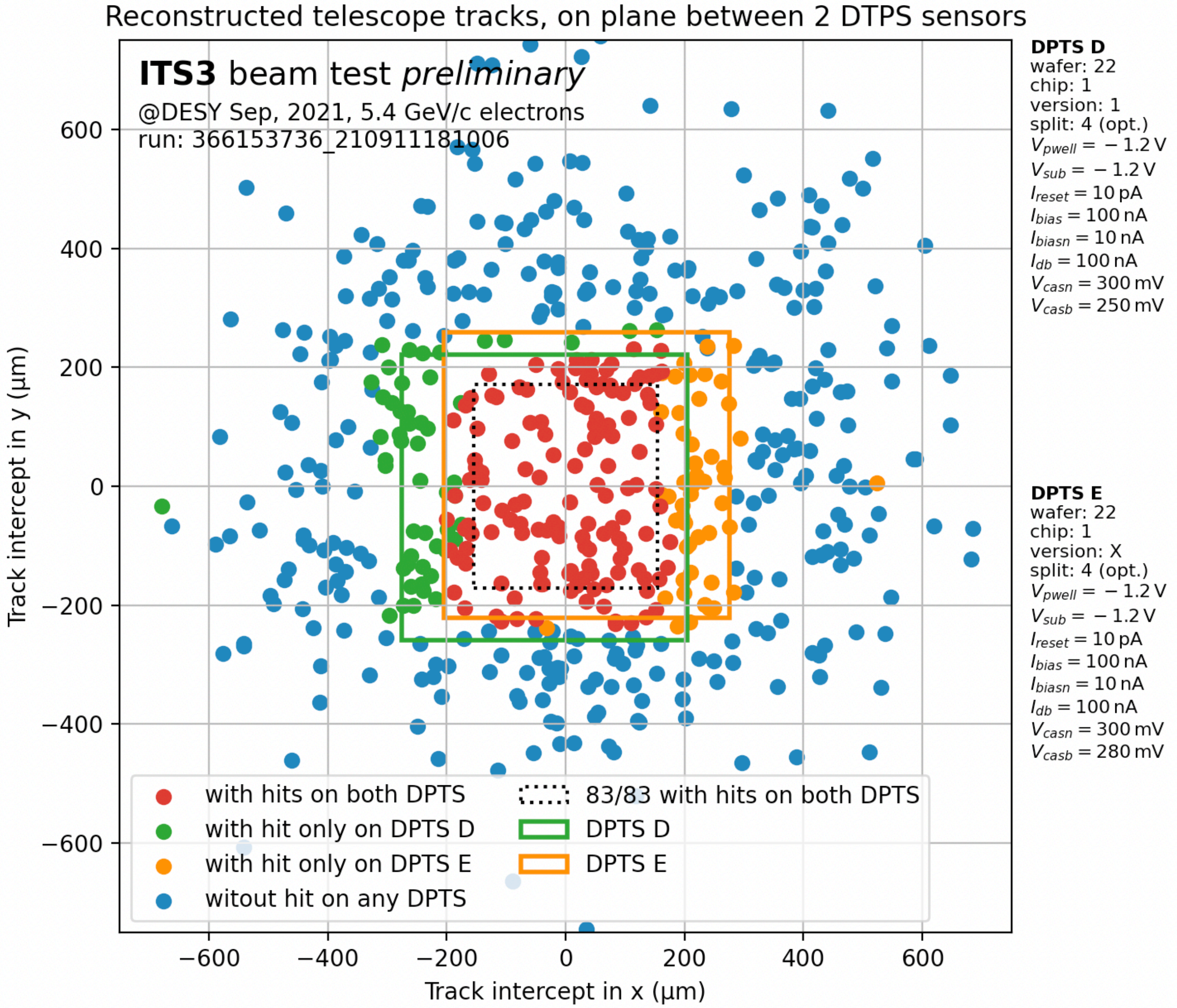
Scintillator with 1.5 mm hole over DPTS chips to veto tracks far outside of the DPTS acceptance

DPTS beam test results (by ALICE measurement team)



- Particle tracks not detected by the DPTS illustrate a clear 100 % shadow corresponding to the sensitive area of DPTS

DPTS beam test results (by ALICE measurement team)



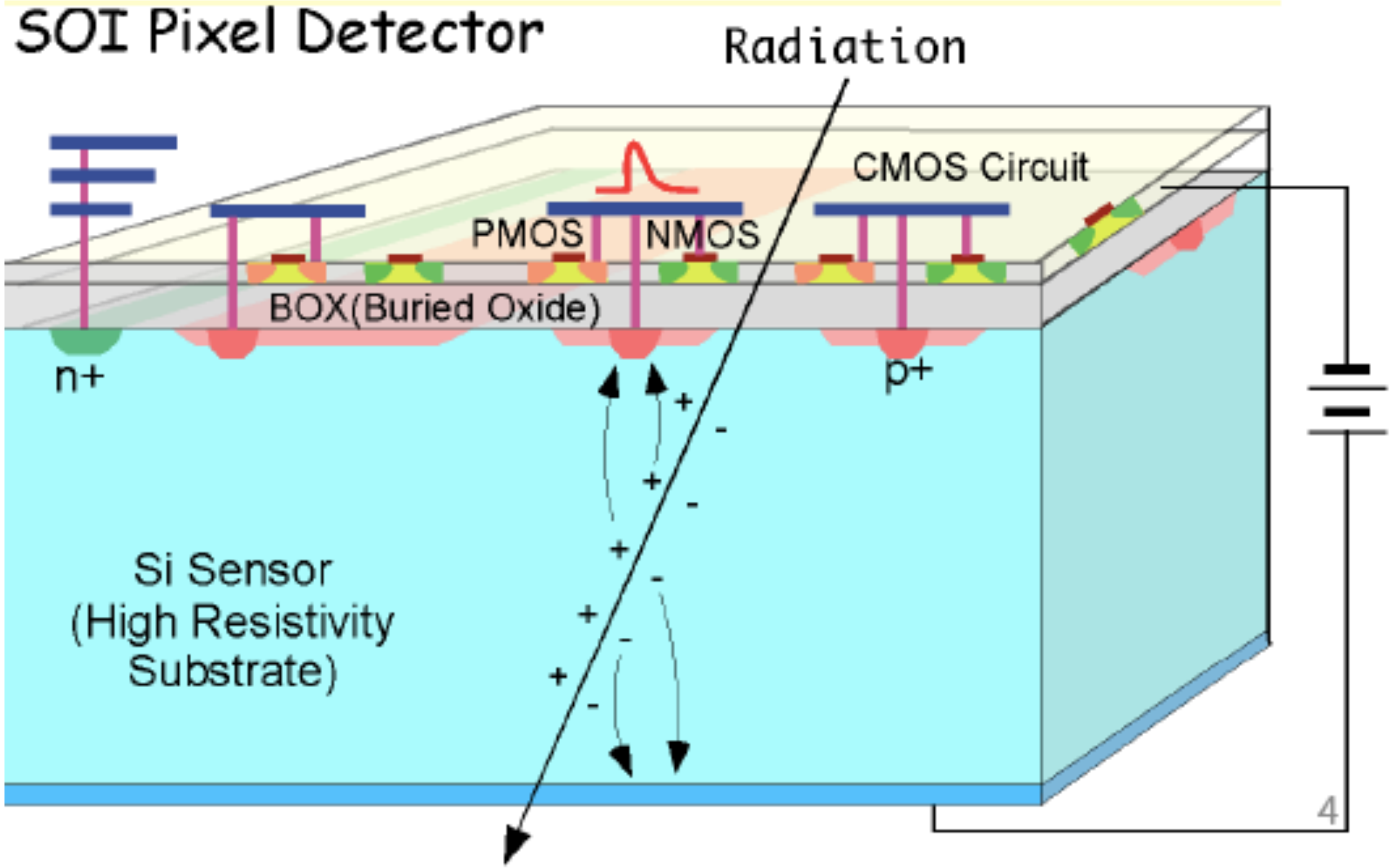
- NO blue dots within sensitive area of the two chips, they see all tracks passing through
  - 166 for the first chip (green + red dots)
  - 162 for the second chip (orange + red dots)
  - 83 tracks in common (red dots)

  (only a few % of the data analyzed)
- Efficiency with (162+166)/(162+166) tracks:

  $100\ \%^{+0\%}_{-1\%}$

  (95% confidence, Clopper-Pearson)
- Excellent sensor *and* front-end performance already from first 65 nm prototype

Some other developments: SOI sensors Y. Arai et al.

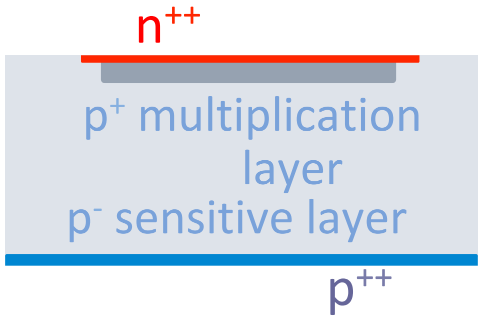


LAPIS 0.2 µm

- Impressive technology development with excellent Q/C
- Large user base and significant interest for many applications
- Some freedom on sensor material
- BOX reduces radiation tolerance, but several measures for improvement were already implemented

- https://soipix.jp

Some other developments (2)

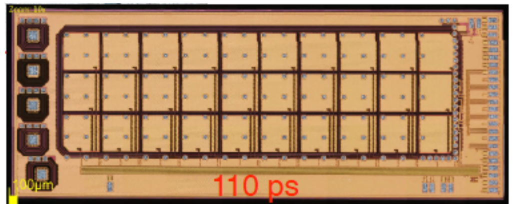


Low gain Avalanche Diodes (LGAD)

N. Cartiglia et al.

- Charge gain in Si
- ps timing for thin sensors
- Radiation damage mitigation under study

NIM A730 (2013) 226-231, NIM A831 (2016) 18-23
NIM A796 (2015) 141-148, NIM A845 (2017) 47-51
W. Riegler & G. Aglieri: 2017 JINST 12 P11017
“Time resolution of Si detectors”

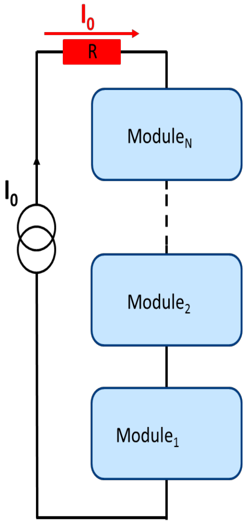


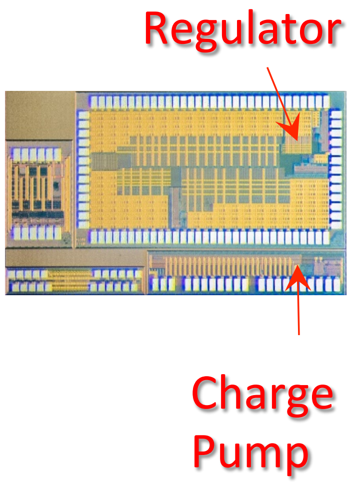
TT-PET

G. Iacobucci et al.

- SiGe readout + TDC
- Down to 50 ps
- Picosecond avalanche detector to do even better

arxiv:1908.09709
JINST 14 (2019) P02009,
JINST 14 (2019) P07013
JINST 13 (2017) P02015,
JINST 11 (2016) P03011,
arxiv:1812.00788
arxiv:1811.12381





Serial power

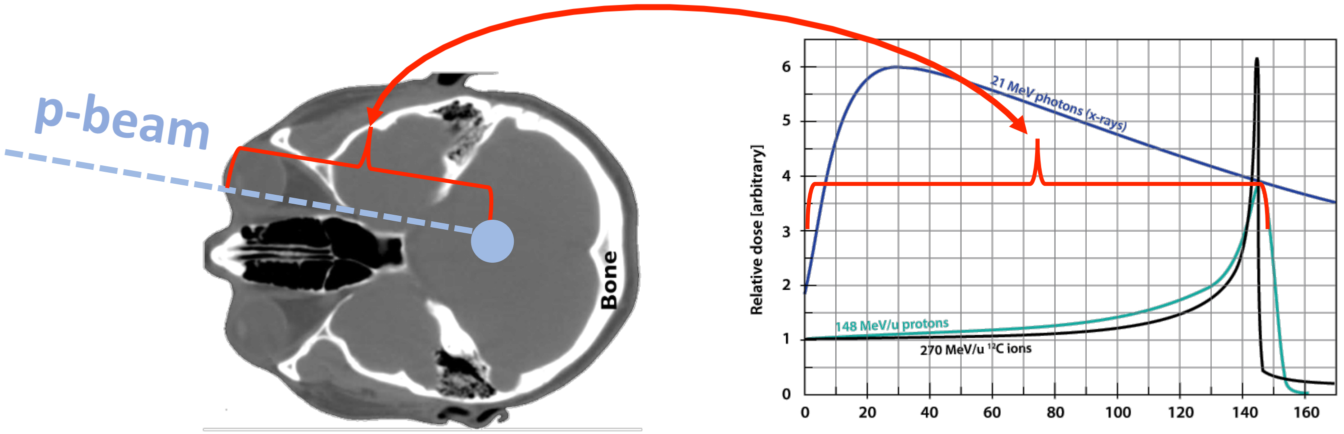
M. Karagounis et al. for hybrid sensors

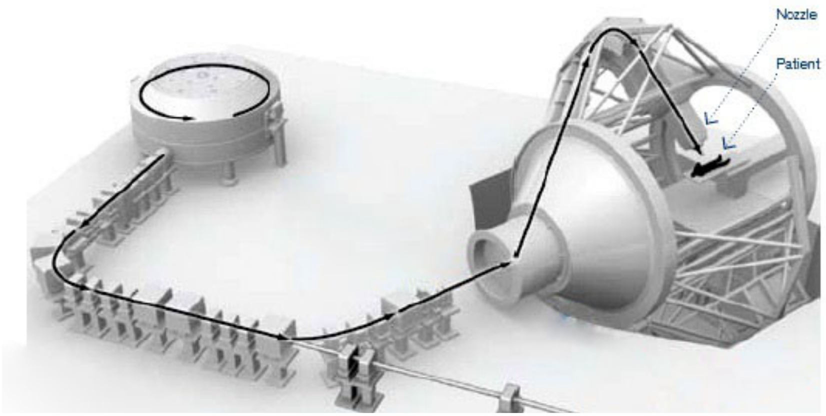
- Connecting sensors in series saves power cabling
- Requires regulation
- Charge pump for sensor bias

S. Bhat, A. Habib et al PIXEL 2018 (for CMOS sensors)

From medical imaging to medical tracking: Proton therapy and proton CT

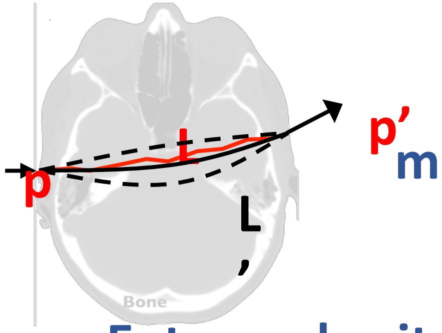
Energy tuning proton beam better than 0.5 % requires proton CT rather than X-ray CT (too poor tissue density resolution)





courtesy of P.Giubilato

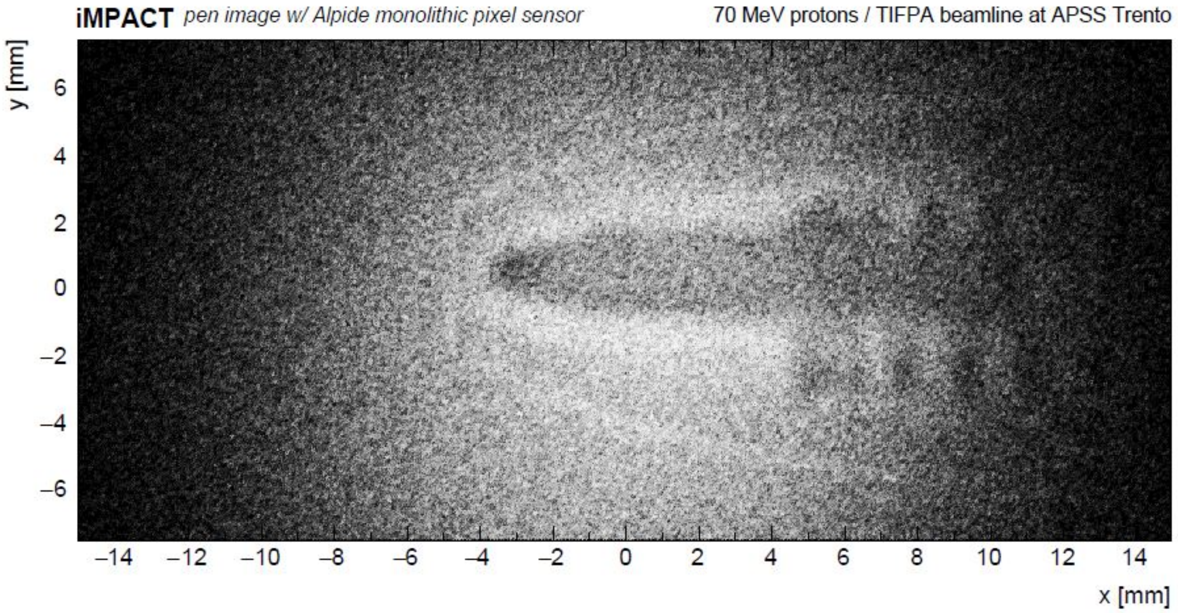
Proton true trajectory



Energy measurement

Entry and exit points + angle

Most Likely Path calculation



Demonstration with ALPIDE chip

Need at least 10^9 proton tracks (entry and exit + most likely path) and 10s of minutes with state of the art detectors.

Gaining time requires detectors which do not yet exist

walter.snoeys@cern.ch

Concluding remarks

Pixel sensors are being used in high energy physics experiments especially in the inner layers to disentangle complex events. Hybrid pixel sensors are still in the majority today.

After years of R&D monolithic sensors for HEP move to CMOS MAPS in mainstream CMOS technology, but requirements for HEP are not completely identical to those for visible light imaging, and some technology flexibility can still be beneficial.

Circuit radiation tolerance as for standard CMOS, which naturally evolved towards significant tolerance with some caveats.

Sensor radiation tolerance, precision timing and improved efficiency can be obtained from optimization for fast charge collection using techniques based on general principles applicable to different technologies. Large collection electrode sensors provide extreme radiation tolerance and more uniform sensor timing but exhibit large input capacitance.

Decreasing technology feature size or special imaging sensor features can increase the voltage excursion on a small collection electrode and ultimately reduce analog front end power to zero and allow precision timing.

Hybrid vs Monolithic distinction is becoming more vague:
2D integration combined with stitching will bring us a long way. 3D could help for the most challenging applications.

Concluding remarks

Feasibility studies on stitched devices will determine the size of the sensors we will design in the future and whether and to what extent we can profit from unbeatable wafer-scale integration. (production volume is in the outer layers, we need to be prepared for volume test/acceptance/monitoring).

Thinning and bending provides opportunities for totally new detector concepts

Pixel sensor readouts are complex circuits:

- The increasing complexity of the sensors and the chips we design require evolution towards digital-on-top design techniques with increasing verification effort.
- Need team of expert chip designers, complemented with device/TCAD/Monte Carlo experts for sensor optimization for monolithic sensors and simulation with excellent foundry support

Large area pixel sensors are enabling devices for many cutting edge research fields and practical applications like tracking in HEP, medical imaging, space-borne instruments, etc, also illustrated by this workshop and collaborations like SOIPIX

MAPS and silicon sensors are one of the few areas where production volume even within HEP would not be negligible, but where our community can have an impact not only on the quality of its own measurements, but also on society in general, and which we should try to exploit to enable access to the most advanced technologies.

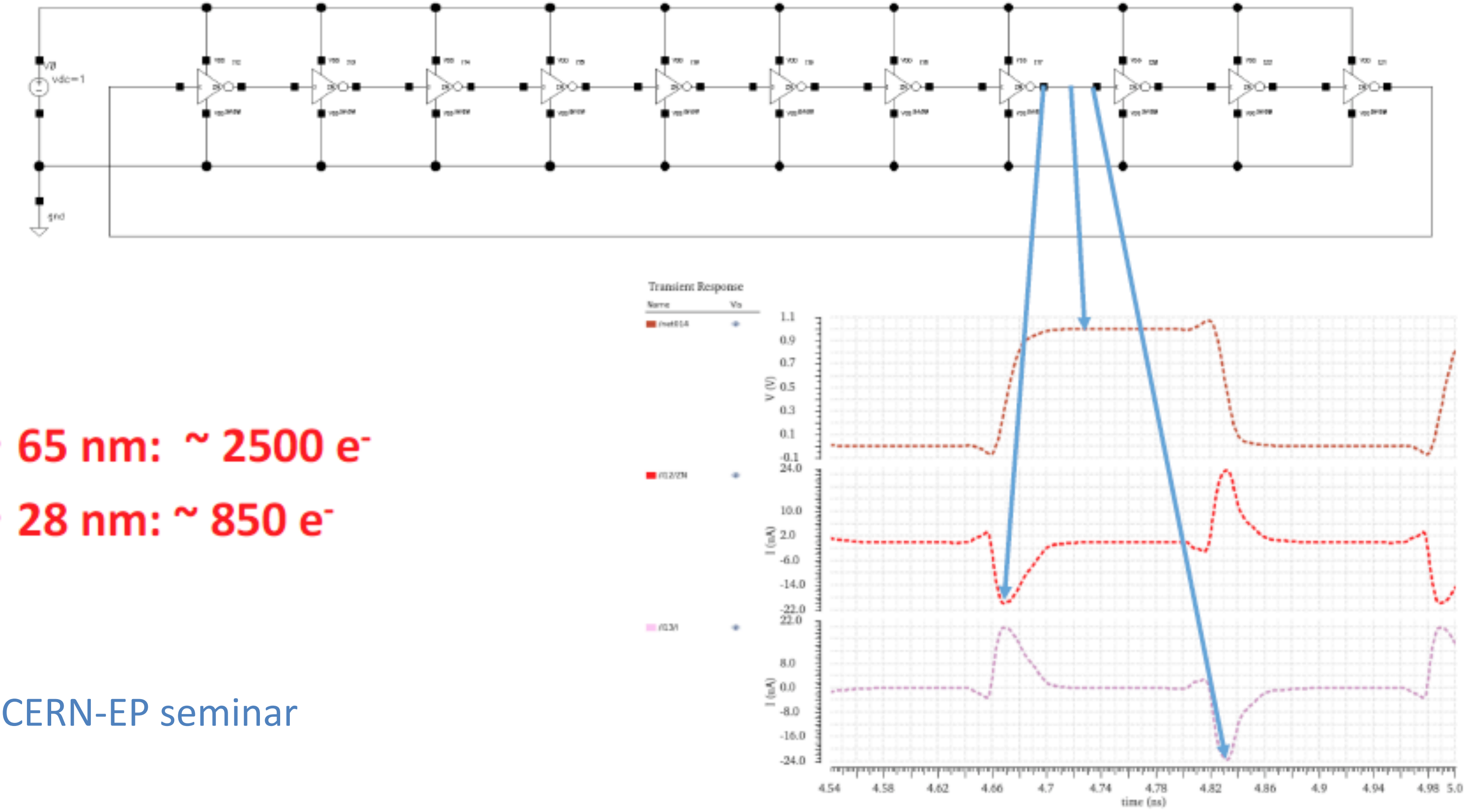
Acknowledgements

- The workshop organizers
- Colleagues from CERN and other institutes, the ALICE and ATLAS experiments, and CERN EP R&D
- Foundry support for monolithic:
  - Ikuo Mizuno from TPSCo
  - Amos Fenigstein, Assaf Lahav from TowerJazz
  - Elie Toledano and Adi Haim from Etesian Semiconductor

and their teams

THANK YOU !

How many electrons are needed to switch a logic gate ?



- **65 nm: ~ 2500 e$^-$**
- **28 nm: ~ 850 e$^-$**

A. Marchioro, 2019 CERN-EP seminar

AM Seminar CERN 2019 47