

Workshop on Advanced Radiation Detector and Instrumentation in Nuclear and Particle Physics (Online)



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Designing a front end digital pulse processing chain for FAIR CBM experiment using FPGAs

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The article is about the front end data acquisition chain developed for the MUON detectors in the CBM experiment at FAIR. As a contribution towards the development of CBM experiment, a prototype system for digital pulse processing (DPP) has been designed by me on FPGA development board. A single channel of pulse processing chain for the pulse analysis of detectors has been developed and tested successfully in our lab. The FPGA has been interfaced to the AD9228 ADC board, which is connected to a multichannel mixed signal Front End electronics (FEE) ASIC board named nXYTER. In our design, the ADC interfacing is the challenging part due to its LVDS serial data inputs at the sampling rate of 20 MHz as per the system design requirements. The concurrent and synchronous nature of FPGA architecture makes it ideal for the testing and development of pulse processing data acquisition chains. The pulses from the ASIC board coming at the rate of 20 MHz are analog inputs, which needs to be sent to FPGA by digitization with AD9228 ADC board. The acquired 12-bit parallel data from ADC board using FPGA is then processed to extract the useful information out of it, which can be then sent to the PC for visualization using various software tools like ROOT, MATLAB etc.

What is your experiment?

Designing a FPGA based nuclear pulse processing chain

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