VL+ in the HL-LHC ATLAS upgrades

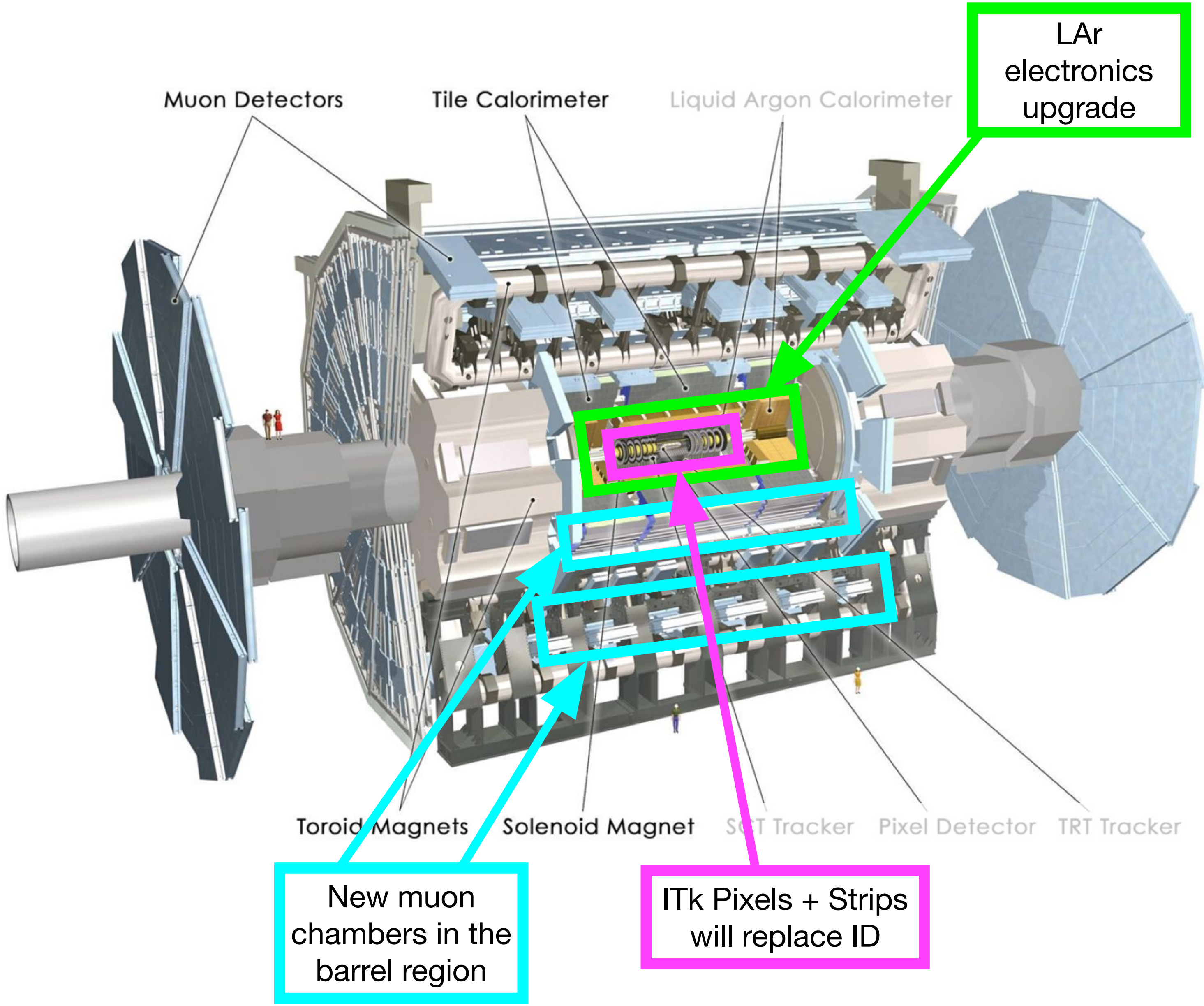
Laura Franconi, University of Bern (for ITk Pixel)

Thank you for their input to:

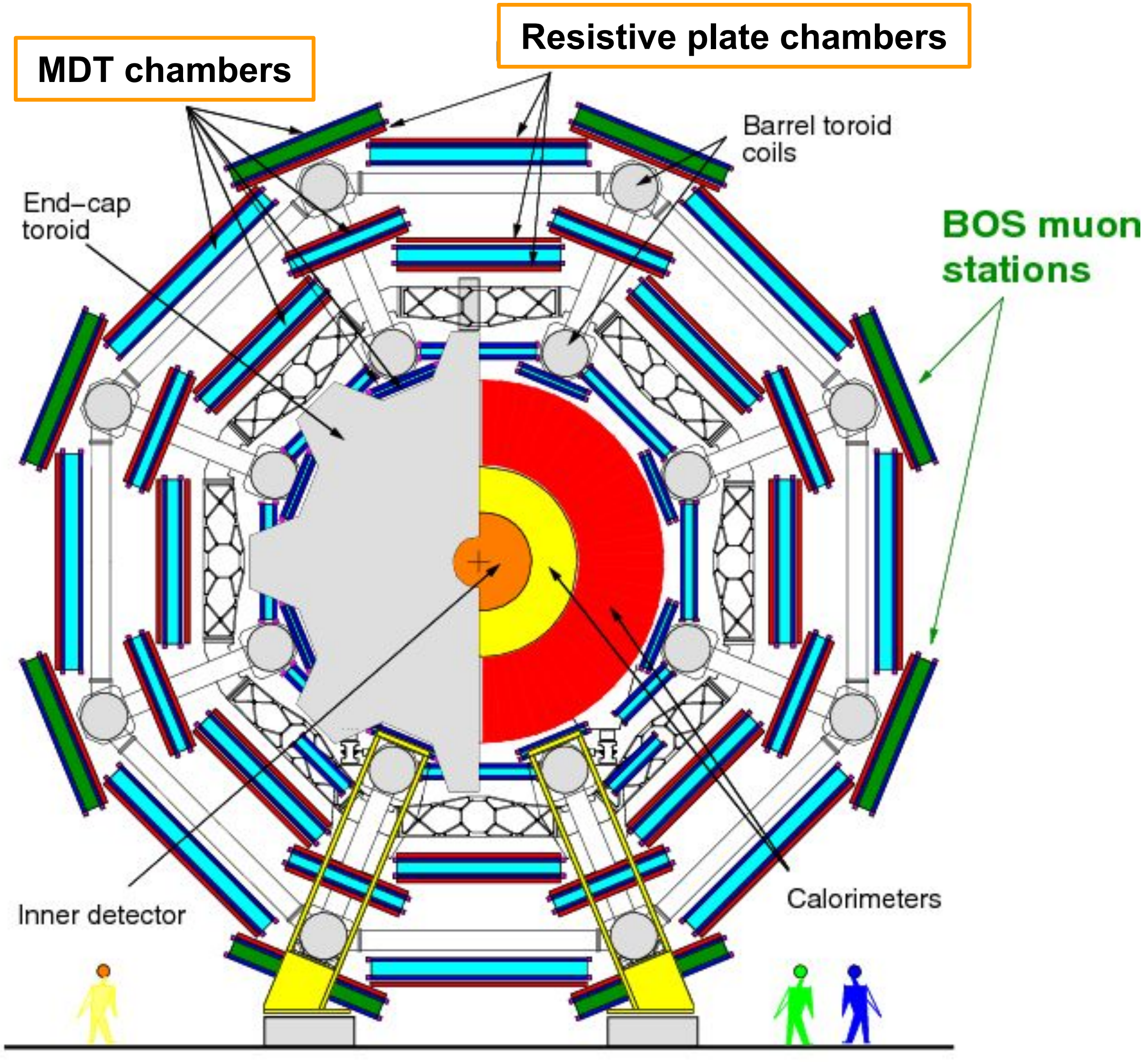
Peter Göttlicher (for ITk Strips),
Tiankuan Andy Liu (for LAr),
Xueye Hu (for Muon)

TWEPP User group meeting, 27 September 2021

ATLAS upgrades for Phase II using VL+



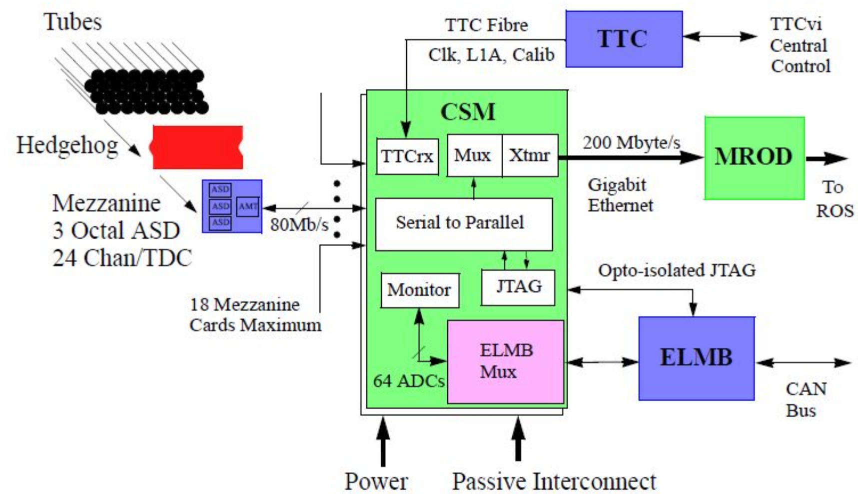
Monitored Drift Tube and Resistive-Plate Chambers



The Monitored Drift Tube Electronics system

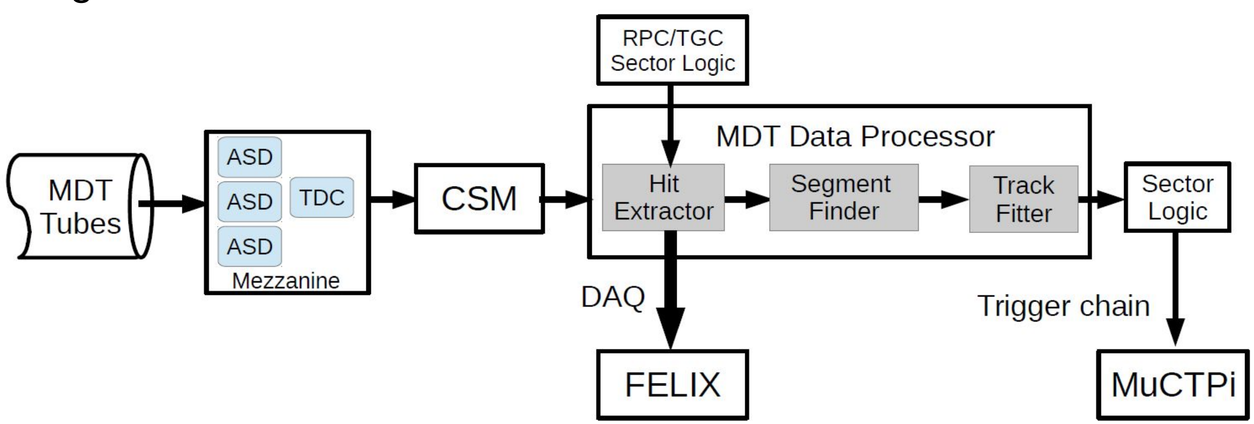
MDT Elx @ current system

- MDT & trigger chambers independently read out
  - MDT readout only on L1 trigger → lower bandwidth
  - Trigger mode used at front-end

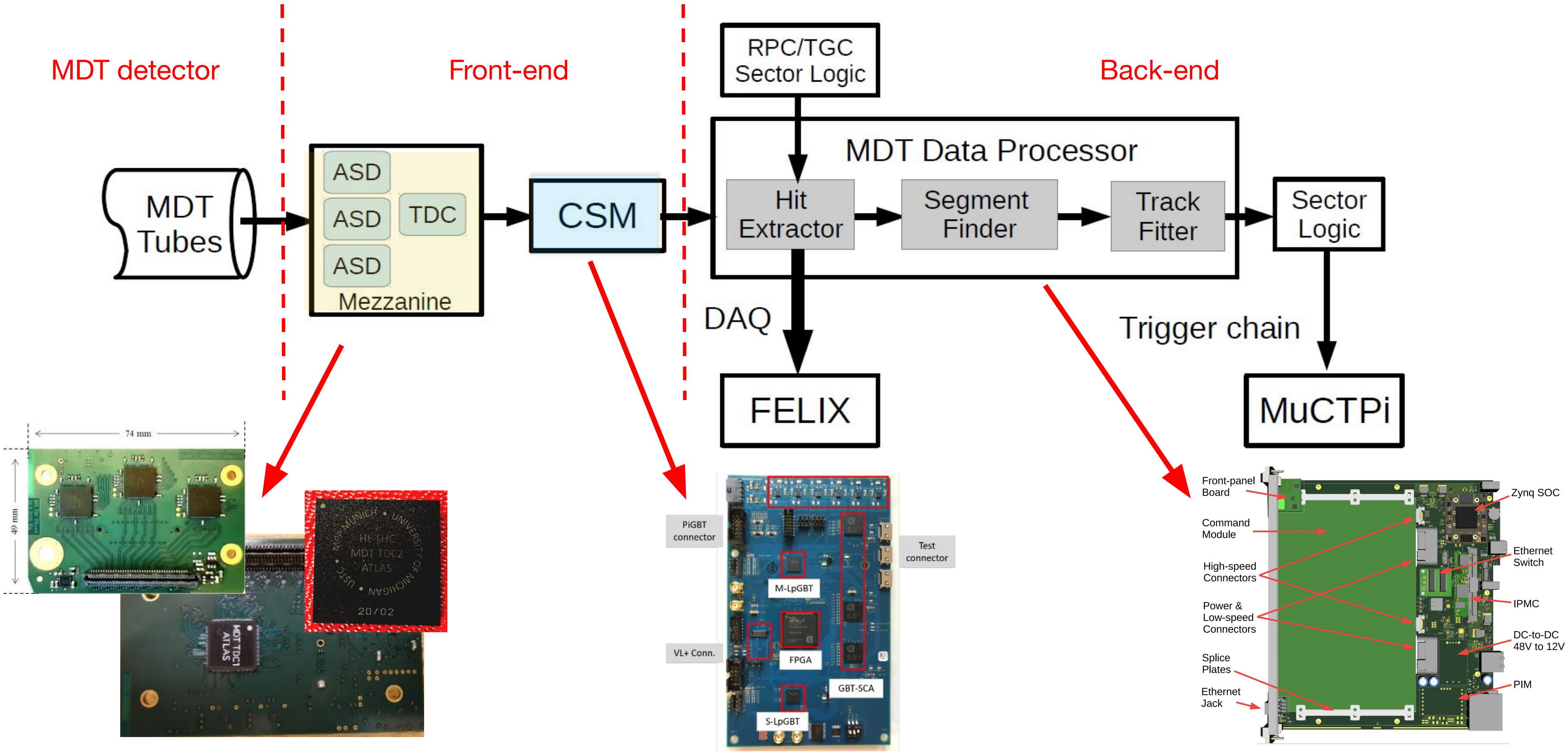


MDT Elx @ HL-LHC

- MDT data “sharpen” trigger decision
  - Find accurate pT using ROI seed from trigger chambers and confirm/reject trigger hypothesis
  - Triggerless at FE and track fitting in the counting room → higher bandwidth



The MDT Electronics system @ HL-LHC



New ASD & TDC

New CSM: lpGBT-chipset based

MDT Data Processor

- New triggerless operation
- Support higher readout bandwidth
- ~80k ASDs & ~22k TDCs

- Flexibly handle both old/new Mezz.
- Fix latency & ~20 Gb/s bandwidth
- 1188 boards

- Provide MDT trigger candidate to the global L0 trigger level
- Precision data readout
- 64 ATCA cards

ASD = Amplifier Shaper Discriminator
TDC = Time to Digital Converter

CSM = Chamber Service Module
GBT = Gigabit Transceiver

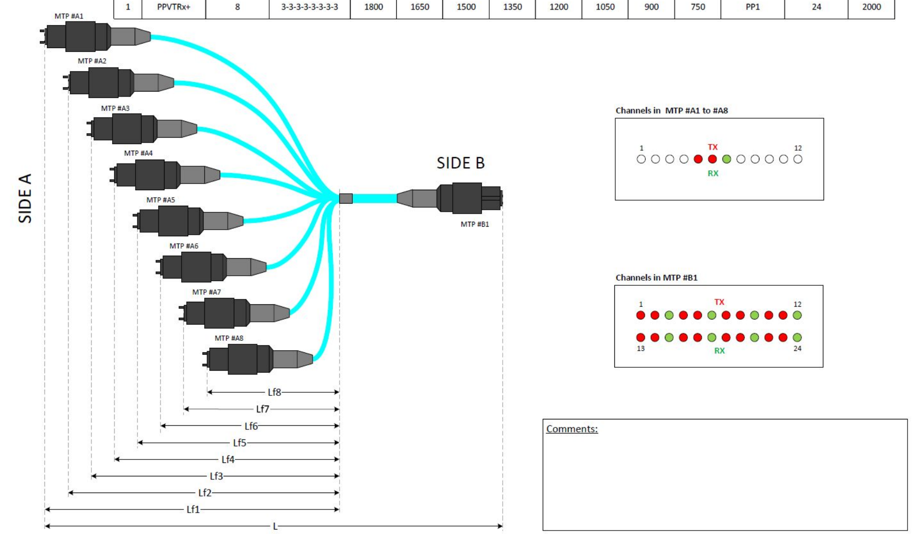
VL+ parts on the Chamber Service Module

CSM	
CSM	● Multiplexes hit timing info from up to 18 FE mezzanines ● Serves as a transfer station for Configuration, Control and Monitoring (CCM) and Timing info for MDT detector → lpGBT & VTRx+ meet both functionality and radiation requirements

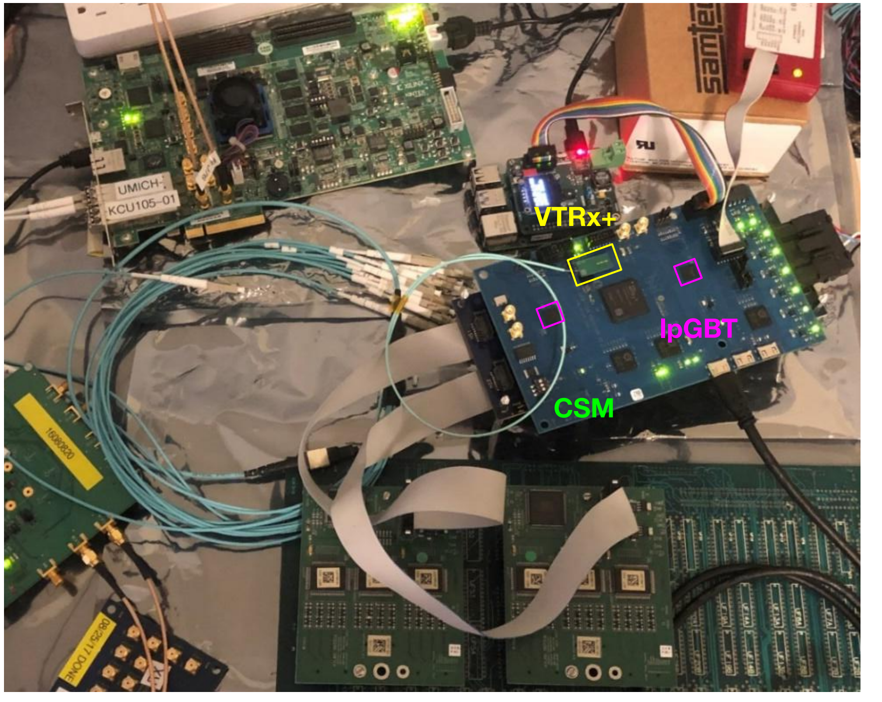
- 1 VTRx+/CSM
  - 2 Tx CHs + 1 Rx CH
- 2 lpGBTs/CSM
  - Master-Slave mode
    - Master-lpGBT: Transceiver mode, recover clock/configure through downlink
    - Slave-lpGBT: Simple Tx mode, reference clock from master-lpGBT elink clock, configure via master-lpGBT EC
  - Uplink:
    - 18x 2 CHs @320 Mb/s FE data
    - 2 fibres @10.24 Gb/s send data to L0MDT
  - Downlink: 2.56 Gb/s (16 e-links @ 80 Mb/s)
  - Monitoring: ADC 8 CHs
- Cabling plant (preliminary*):
  - Each MDT sector has one fibre box
  - Each sector has 5-8 chambers
  - Each chambers has one CSM
  - Each CSM has 3 fibres (2 uplinks, 1 downlink)
  - *not finalised on grading length, procurement by Taiwan collaborator

VL+ Prototype – Fanout_5_ATLAS_MUON

Item	SIDE A											SIDE B		L [cm]
	Connection Point	Nb of connectors	Nb of used fibres per connector	Lf1 [cm]	Lf2 [cm]	Lf3 [cm]	Lf4 [cm]	Lf5 [cm]	Lf6 [cm]	Lf7 [cm]	Lf8 [cm]	Connection Point	Nb of used fibres	
1	PPVTRx+	8	3-3-3-3-3-3-3-3	1800	1650	1500	1350	1200	1050	900	750	PP1	24	2000



VL+ parts on the CSM prototype



lpGBT on CSM prototype

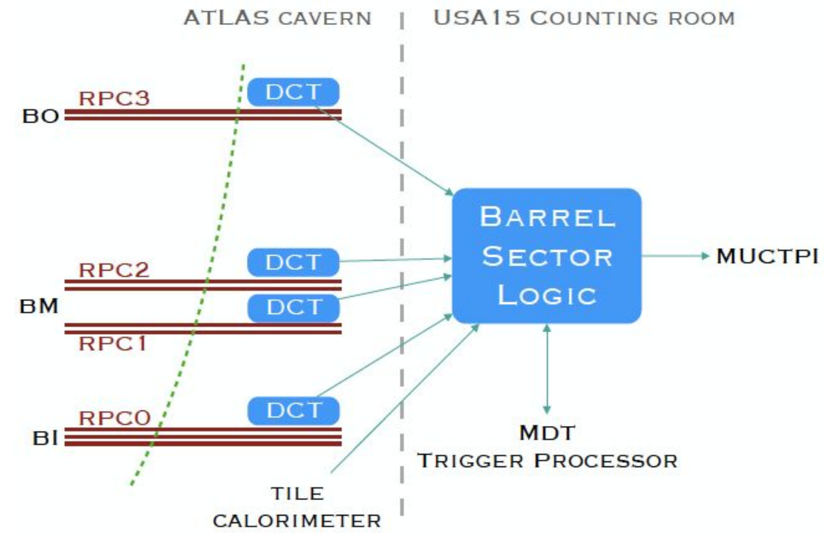
- 20 pcs assembled on 10 CSM boards
- Functionality: all working as expected
- Issues: configuration can be lost when moving piGBT connector from master to slave lpGBT or when have statics

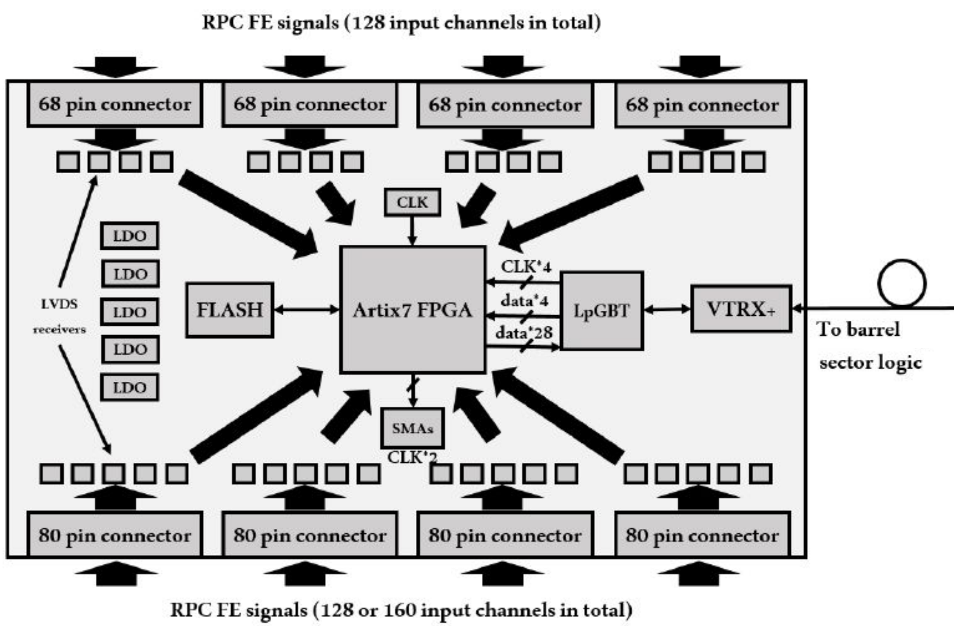
VTRx+ on CSM prototype

- 3 VTRx+ v0 modules at Umich
- Functionality: all working as expected
- Issues:
  - MT connector and bare fibres are vulnerable, so we need to add MT-MPO adapter on board (CSM board has strict size limitation)
  - It seems v1 has different mechanical drawings and different I2C register mapping but the information has not been released clearly
    - causes some confusion for L0MDT group

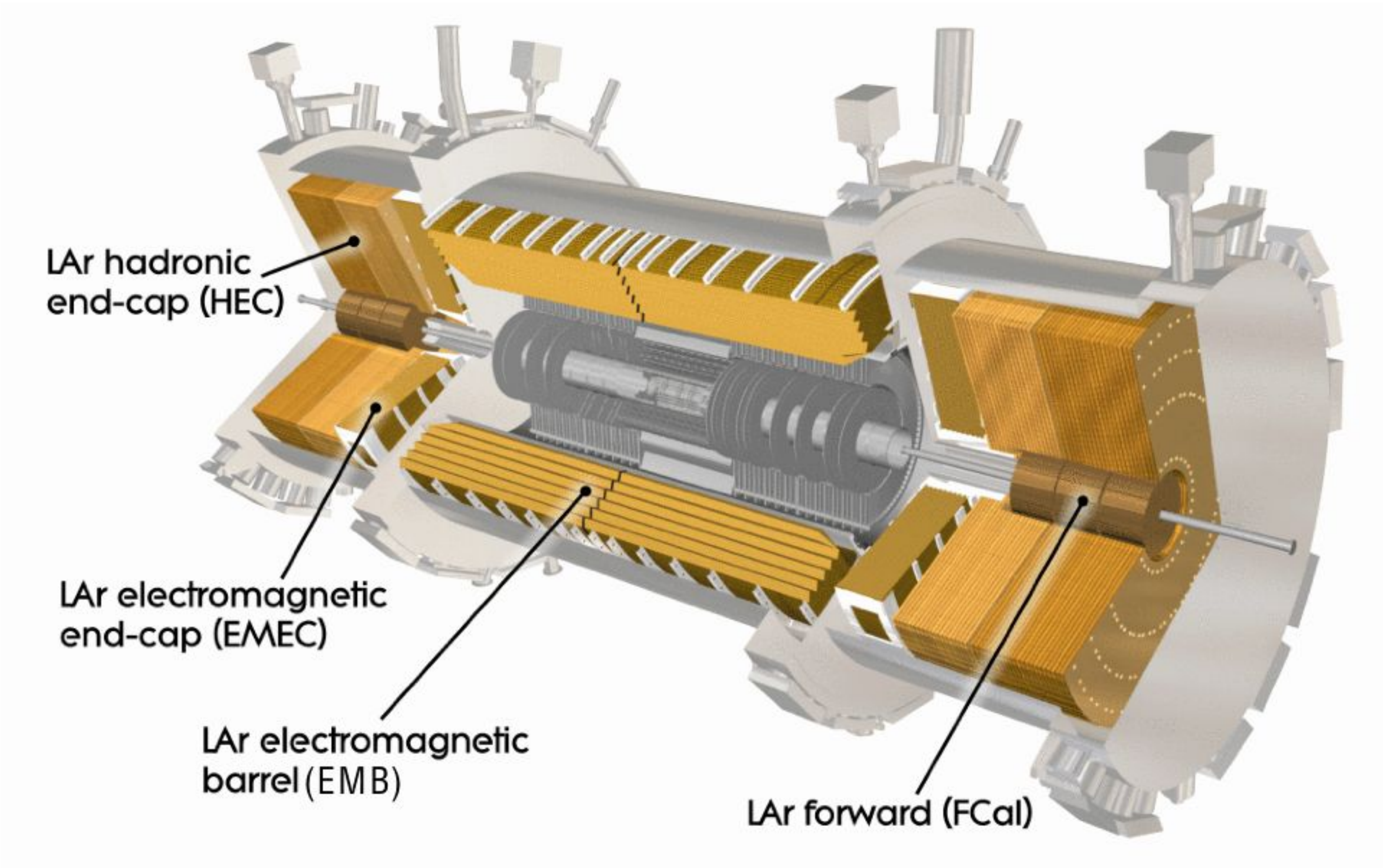
RPC Data Collector and Transmitter (DCT)

- Upgrade of RPC readout and Barrel Muon trigger
- All RPC hits are collected by DCTs and sent off-detector to Barrel Sector Logic board via optical fibre
- 1570 DCTs, up to 288 channels each, two flavours:
  - for legacy RPCs (BM, BO)
    - DCT includes a TDC functionality
  - for new BI RPCs
    - DCT reads already digitised data from RPC FE boards
- DCT components:
  - Artix-7 FPGA
  - lpGBT
  - VTRx+ → replaced by a commercial SFP+ optical transceiver? (decision in Oct)
  - LVDS receivers
  - LDOs
- First prototype (BM-BO type) just received
- Passive fibre plant to be designed

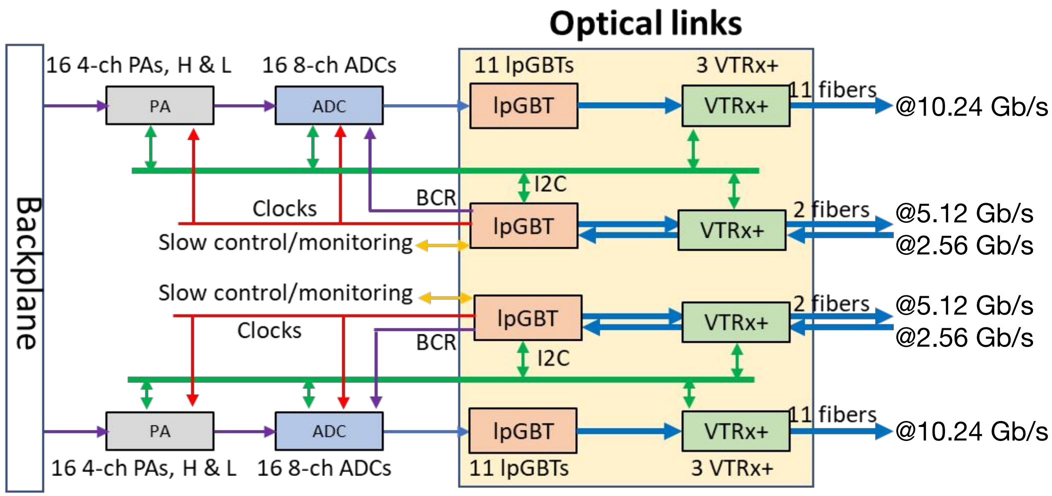




Liquid Argon Calorimeter



Optical links in ATLAS LAr calorimeter Phase II



- Data links to transmit all digitised data off detector
  - 128 analog channels per Front-End Board (FEB2),
  - 1524 boards
  - Data rate/FEB2 > 200 Gb/s
  - Total LAr data rate > 300 Tb/s

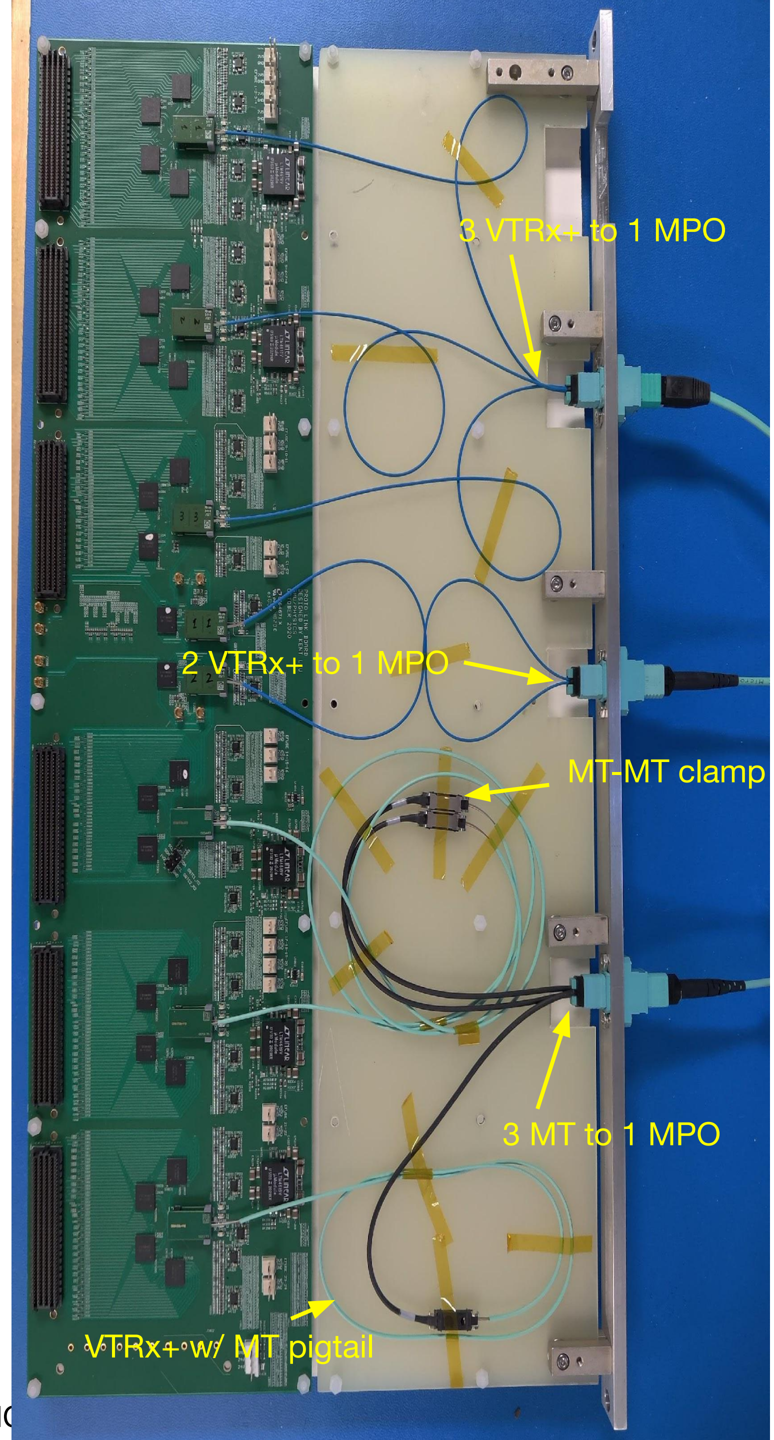
- Control links for clocks, bunch crossing reset signals, I2C configuration, and other slow control/ monitoring (reset, temperature, etc.)

- Each FEB2 has 24 lpGBTs and 8 VTRx+ modules
  - The whole LAr calorimeter uses 40k lpGBTs and 13k VTRx+ modules

- Radiation level (ASICs):
  - TID: 2.25 kGy
  - NIEL: $4.9 \times 10^{13}\ n_{eq}/cm^2$
  - SEE: $7.7 \times 10^{12}\ h/cm^2$

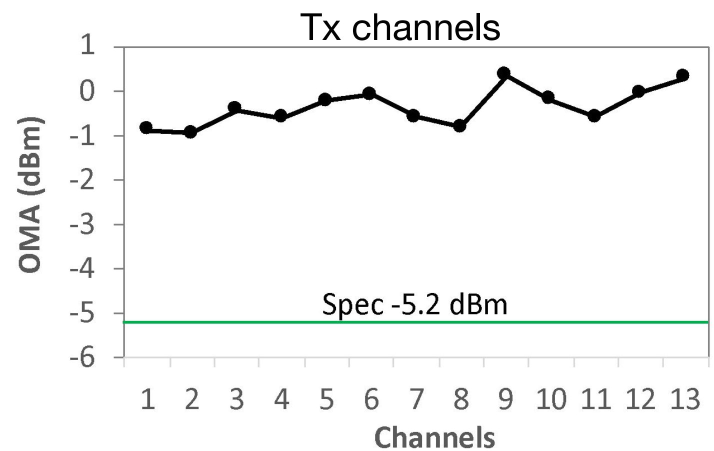
Fibre routing on FEB2

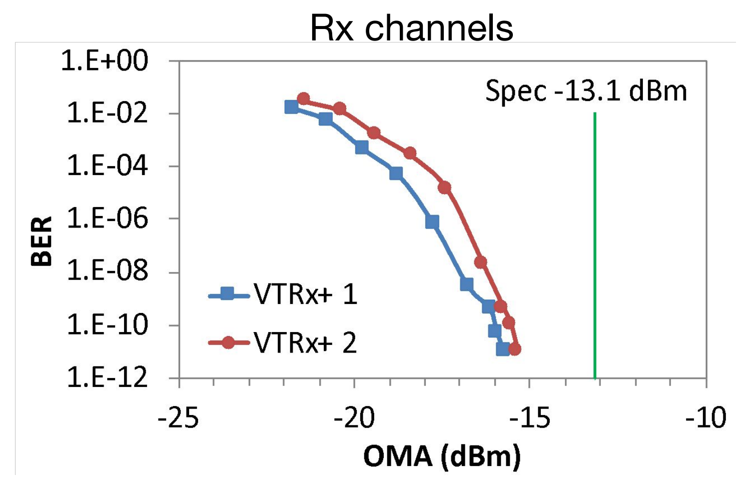
- Connecting all modules with front panel with extra fibre, insertion loss, board area, and assembly efforts
- Exploring the possibility to re-connect 2 or 3 VTRx+ modules directly to an MPO adapter
- The current prototypes (3 MT to 1 MPO and 2 MT to 1 MPO, shown on the top of the photo) have fibres longer than needed for possible modifications of the plant



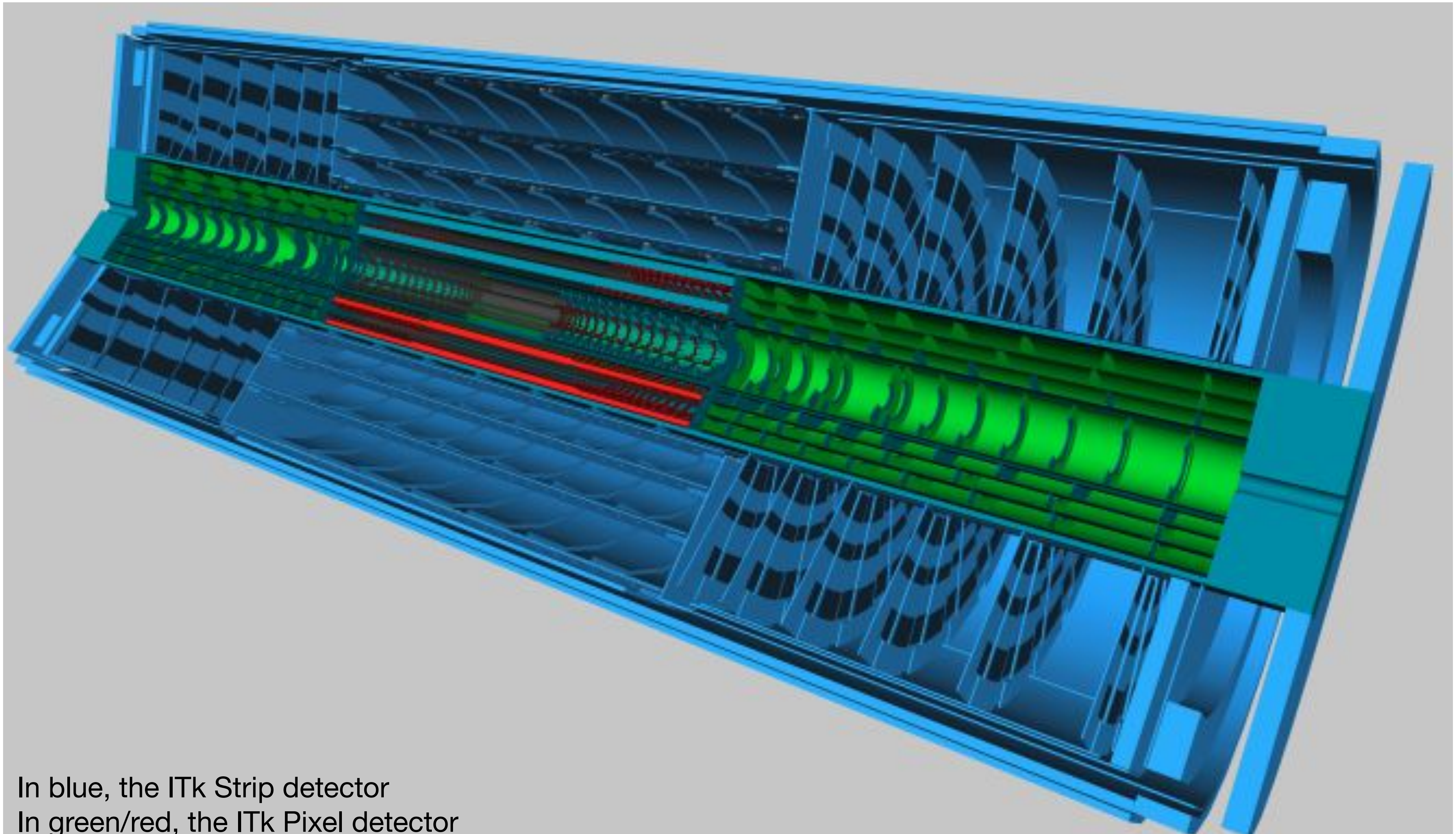
VTRx+ reconnection status

- We asked two assembly houses to prototype a few samples
- 5 modules are re-connected, shipped back, and passed the proposed QC test. Another 5 modules are on the way to ship back
- No pre-assembly test. Post-assembly test results are shown on the right
- We assume that reconnection affects only optical power, so we will not need to perform a full QC test



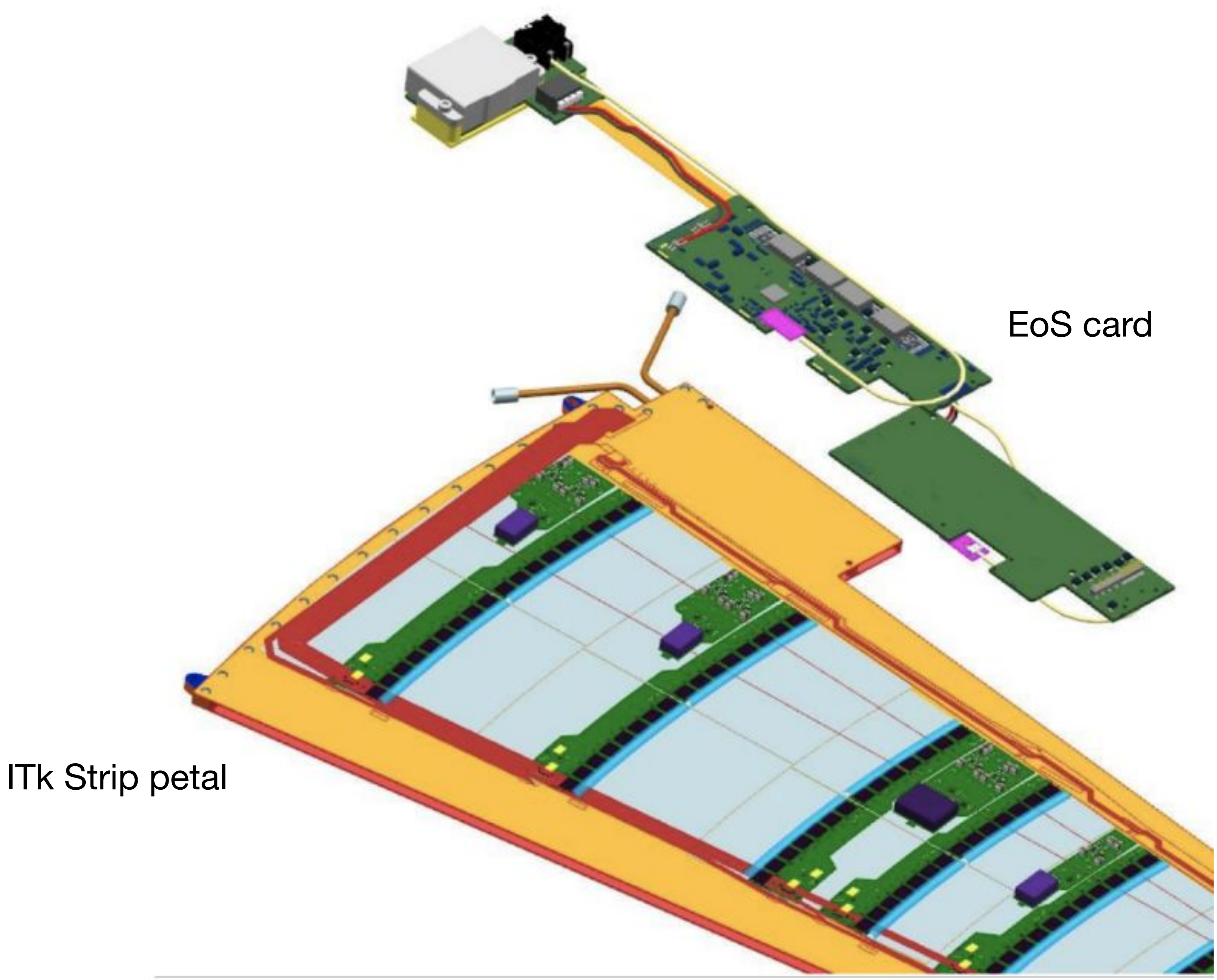


ITk Strip



In blue, the ITk Strip detector
In green/red, the ITk Pixel detector

End of Structure card



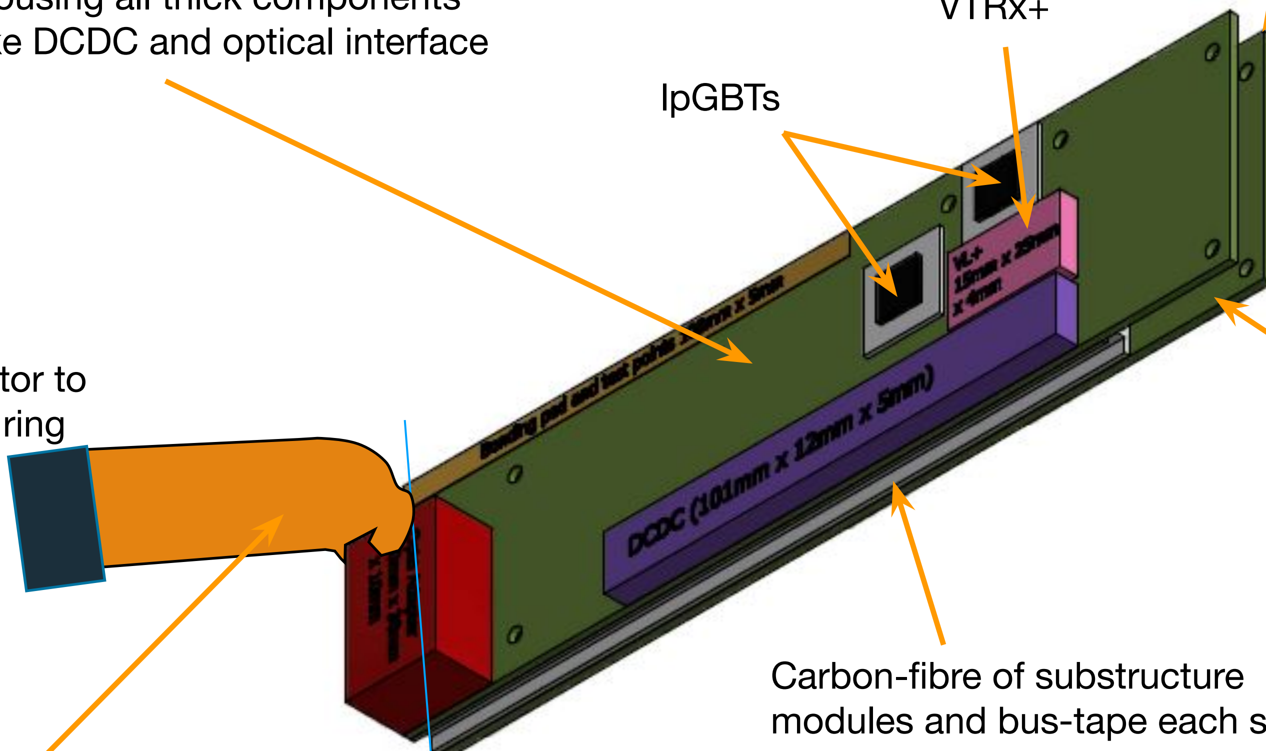
General concept of the EoS

Slave EoS:
Only thin components

Master EoS:
Housing all thick components
like DCDC and optical interface

VTRx+

lpGBTs



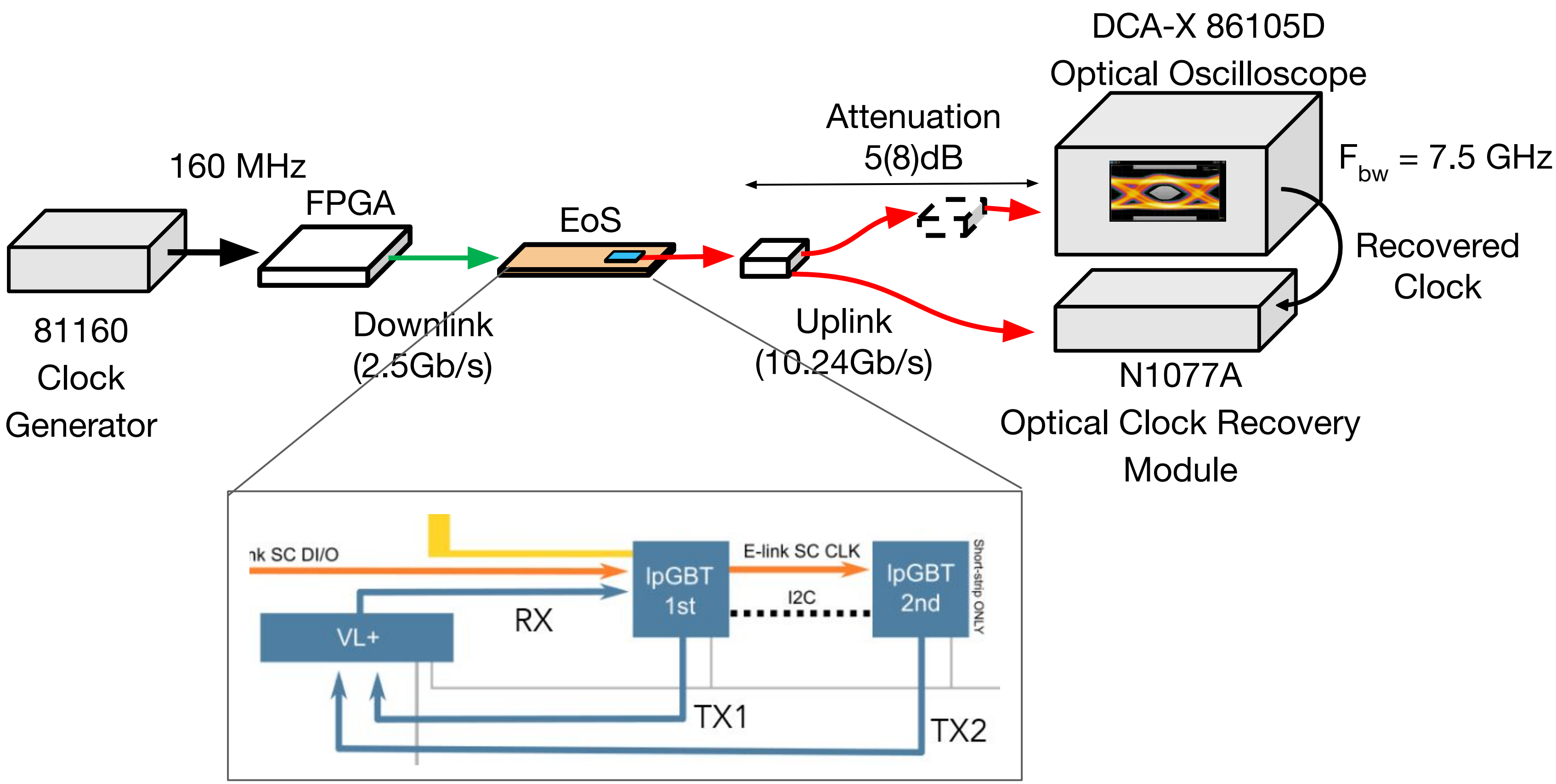
Connector for
master-slave
interconnect

Connector to
Service ring

Carbon-fibre of substructure
modules and bus-tape each side
→ Each EoS region gets 2 boards:
a "Master" and "Slave"

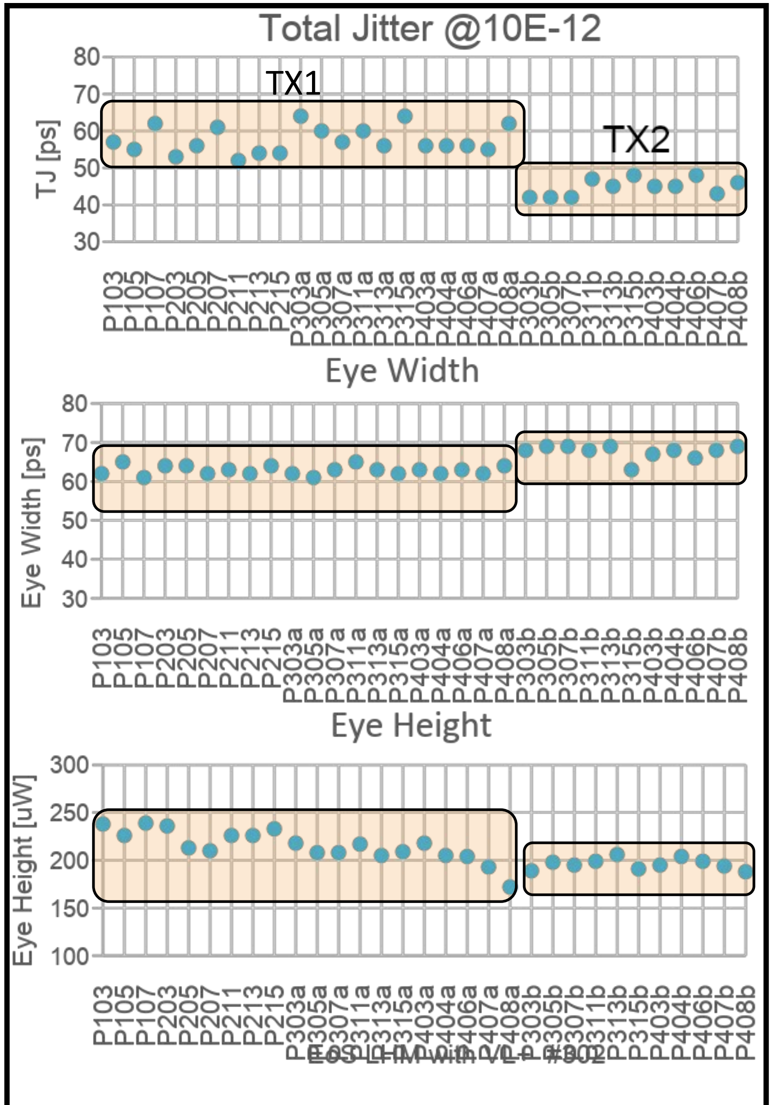
Flexible connection
to Service ring with
connector to PP0
either on master or slave

Setup for QA (optical eye diagrams)



- The setup has a minimum attenuation of ~5 dB on the Tx line
- At the moment we use a set of not optimised parameters for the lpGBT/VL+
- Some combinations of EoS and VL+ do not comply with the eye mask standard in the VTRx+ specs document (EDMS document No.1719329)

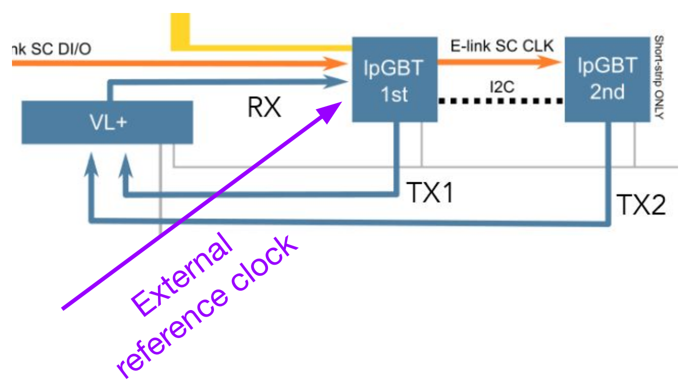
Different behaviour Tx1 vs Tx2



Comparing 20 EoS cards using the same VL+

Studies on Tx performance

- Different behaviour of Tx1 and Tx2 measured during tests on ~10 cards with the same VTRx+ module
  - Different EoS designs
  - Different individual PCBs, lpGBTs and VTRx+
- Difference disappears with use of external clock
- More studies enforced by the reviewers
  - Not critical issue, to be checked with new chips when available



Clock recovery modes

Tx1 jitter is worse when using the Rx to recover the clock w.r.t. using the external reference clock

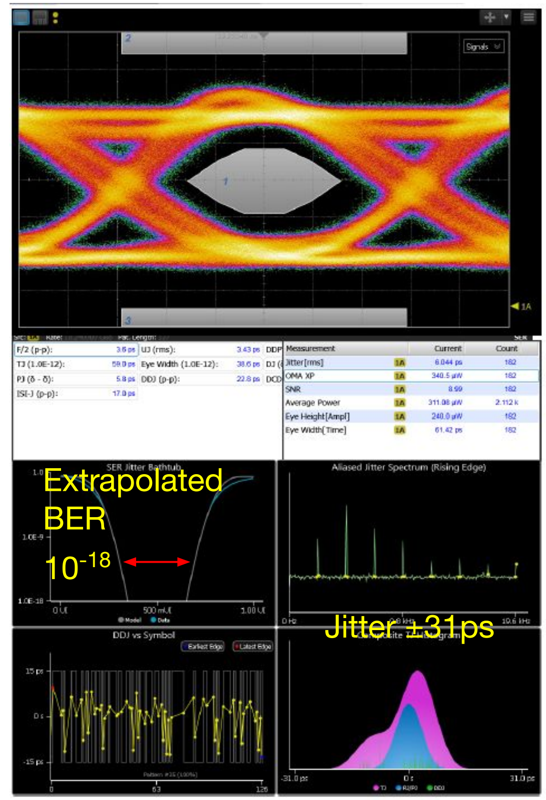
The reason is not understood, under investigation

- Cross talk from Rx to Tx?
- More heat load in lpGBT1?
- Can optimisation of parameters help?
  - How to optimise simultaneously multiple parameters?

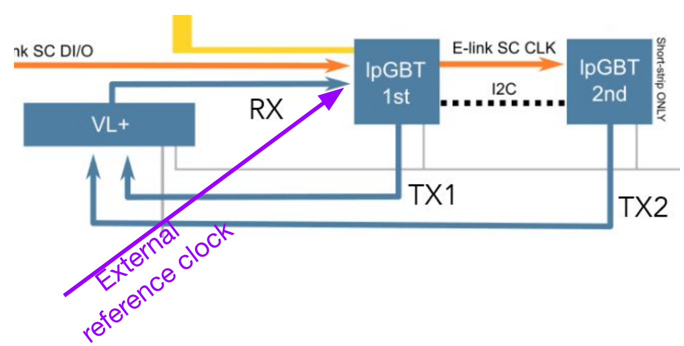
BER within specs (regardless of clock scheme): BER is far better than 10^{-12}

In detector, clock must be recovered from Rx

Tx1 with Rx-recovered clock



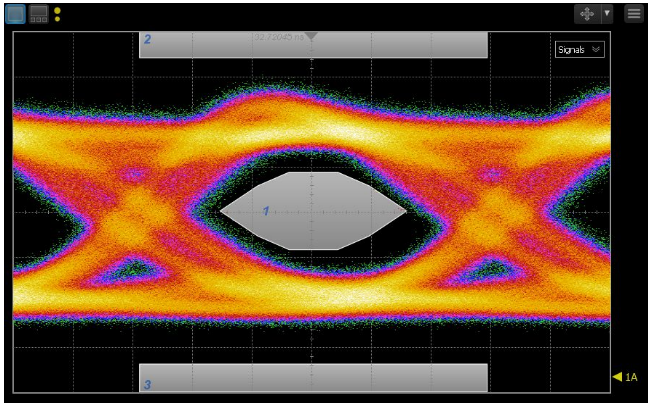
Tx1 with external ref. clock



Effect of the temperature on the uplinks

Tx1 "Rx-recovered clock"

-30 ^{0}C

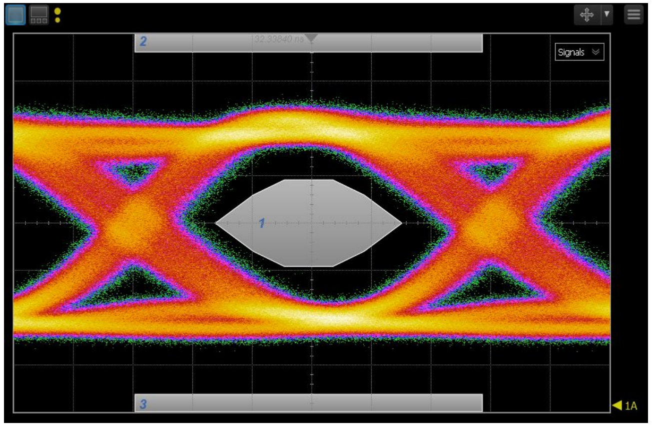


QA - Optical eye-diagrams for 10Gb/s fibres

Measure with ~5dB additional attenuation

For all cold temperatures the BER was < 10^{-12}
Slightly better jitter for warm temperature

+10 ^{0}C



More info in back-up slides

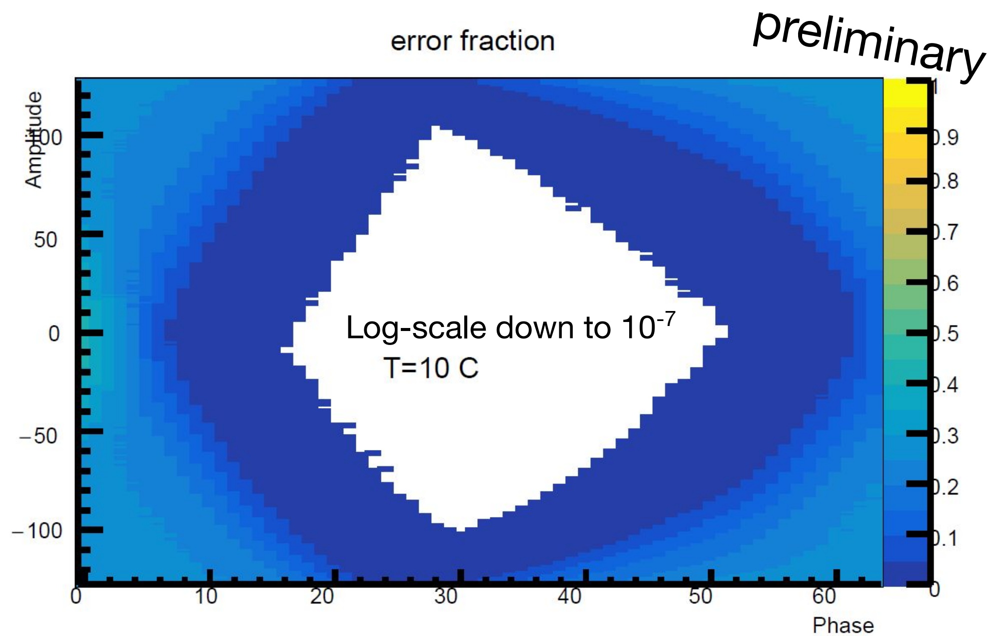
Eye diagrams for QC

QC: Eye diagrams with KINTEX-7

FPGA code for usual operation of the lpGBT (no specific bit-stream protocol from XILINX)

During QC, it is useful to get a qualitative measurement for every EoS.
ToDo: identify an easy parameter to tag bad candidates.

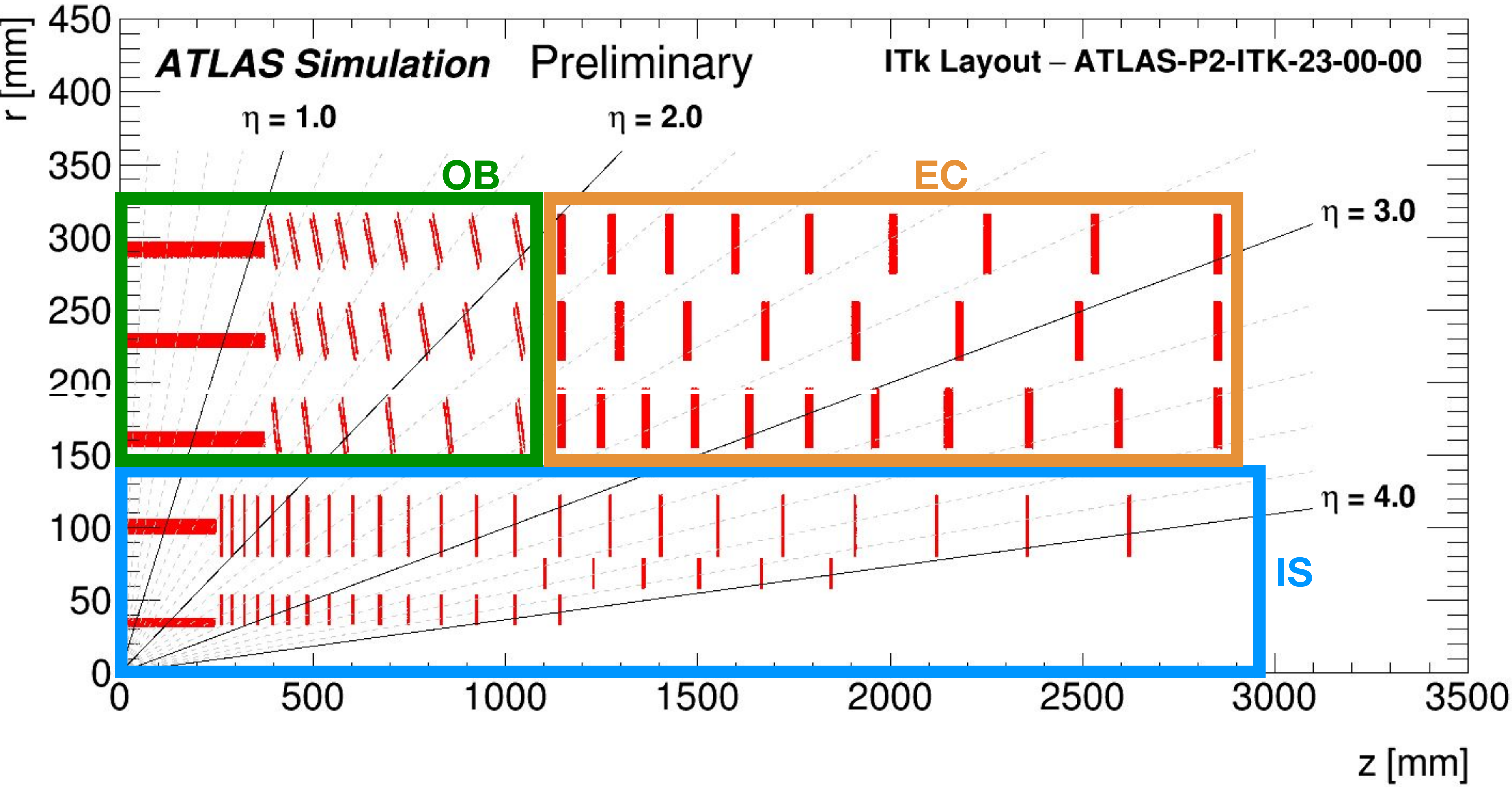
For QA we do the measurement on a few cards with an optical instrument looking to the fibre



Summary ITk Strips EoS

- Pre-production of EoS master and slave cards with available lpGBT-v0
  - Critical issues because of connector shortage and limited experience in the integration
- Final design will be completed in the next weeks
  - Order PCB (delivery ~ 85 working days)
  - Assembly with lpGBT-v1
- QA/QC progress, here highlighted the Tx-eye diagrams and development to get it in QC with less accuracy, but for every PCB

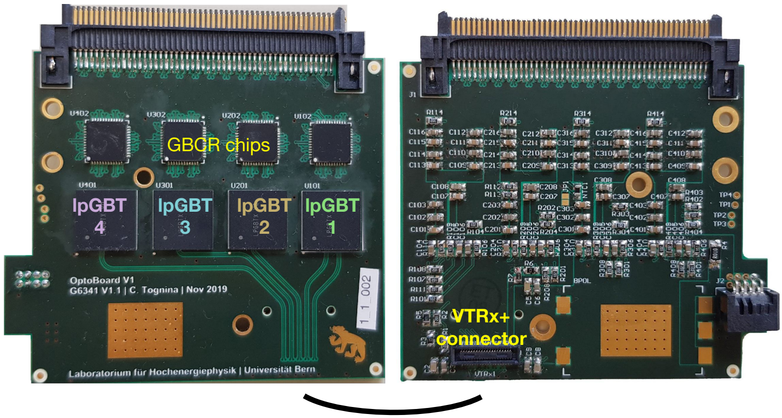
ITk Pixel


ATLAS Simulation Preliminary
ITk Layout – ATLAS-P2-ITK-23-00-00
η = 1.0
η = 2.0
η = 3.0
η = 4.0
OB
EC
IS
r [mm]
z [mm]
450
400
350
300
250
200
150
100
50
0
500
1000
1500
2000
2500
3000
3500

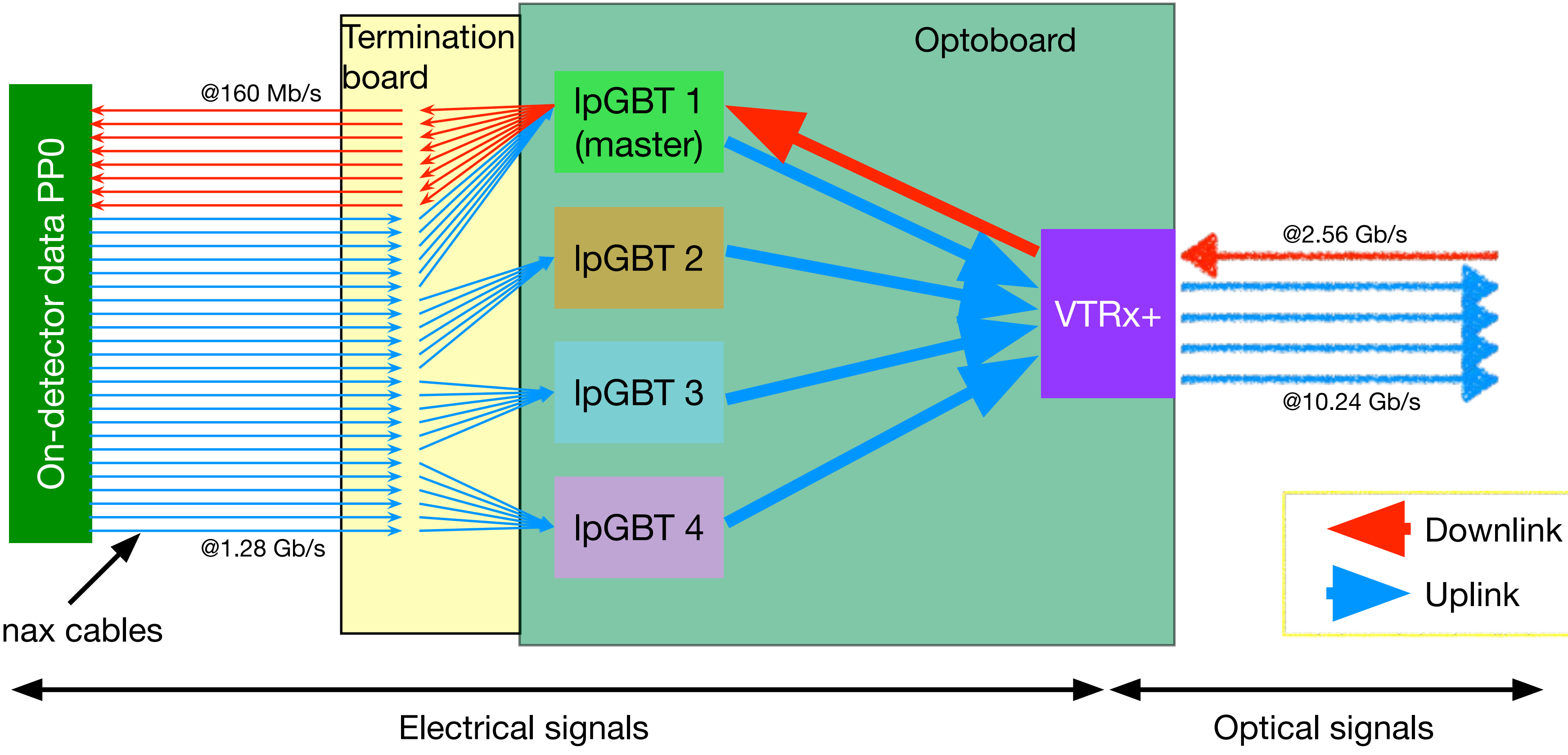
The Optoboard

Aggregates and performs electrical-optical conversion of the data signals and trigger and commands

NOTE: not all twinax cables are always connected, not all lpGBTs are always active!

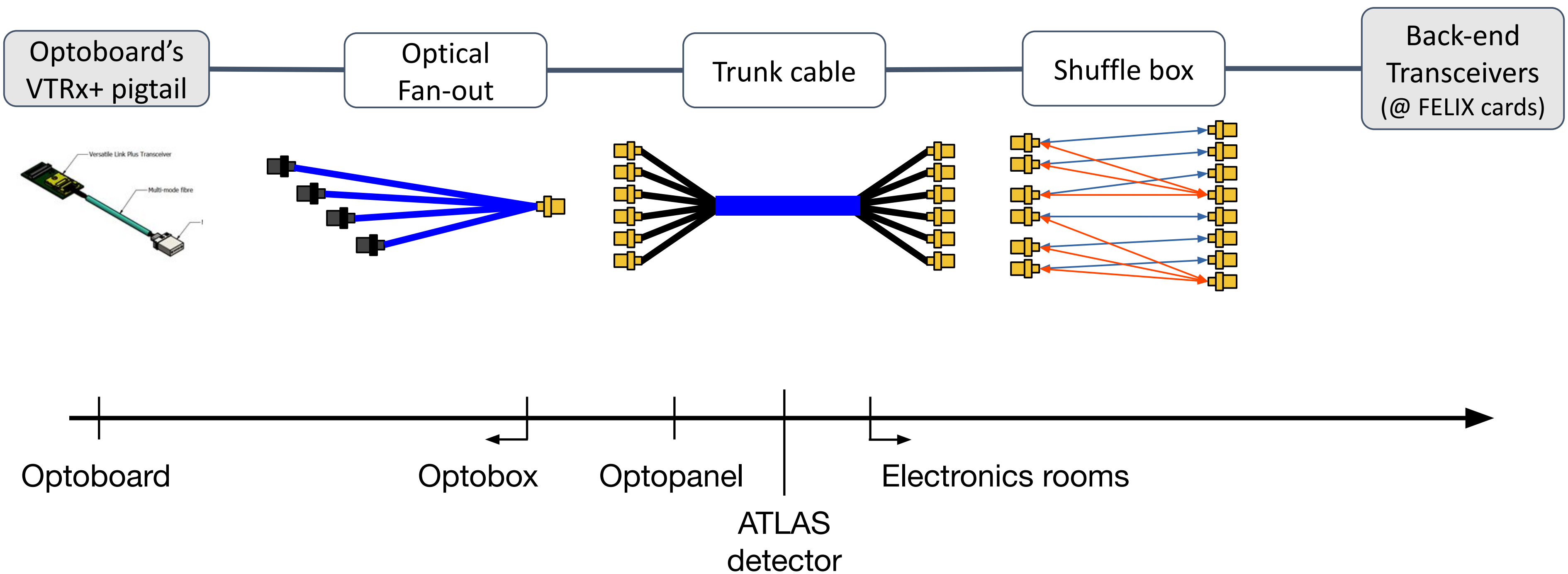


Optoboard

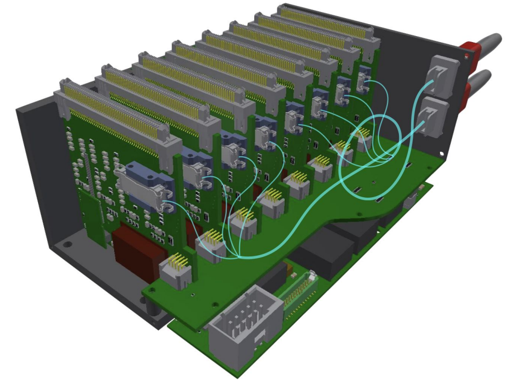


ITk Pixel DT chain - optical

Propagates the optical signal from the Optosystem to the electronics room



Complexity in the Optosystem



- 1564 Optoboards, 220 Optoboxes (normal + mirrored)

13 different Optoboard flavours (combination electrical uplinks/downlinks)

Each Optoboard's VTRx+ has 1 to 4 active optical uplinks

Optoboxes have different number of Optoboards (constraints given by powering) and can host Optoboards with different optical configurations

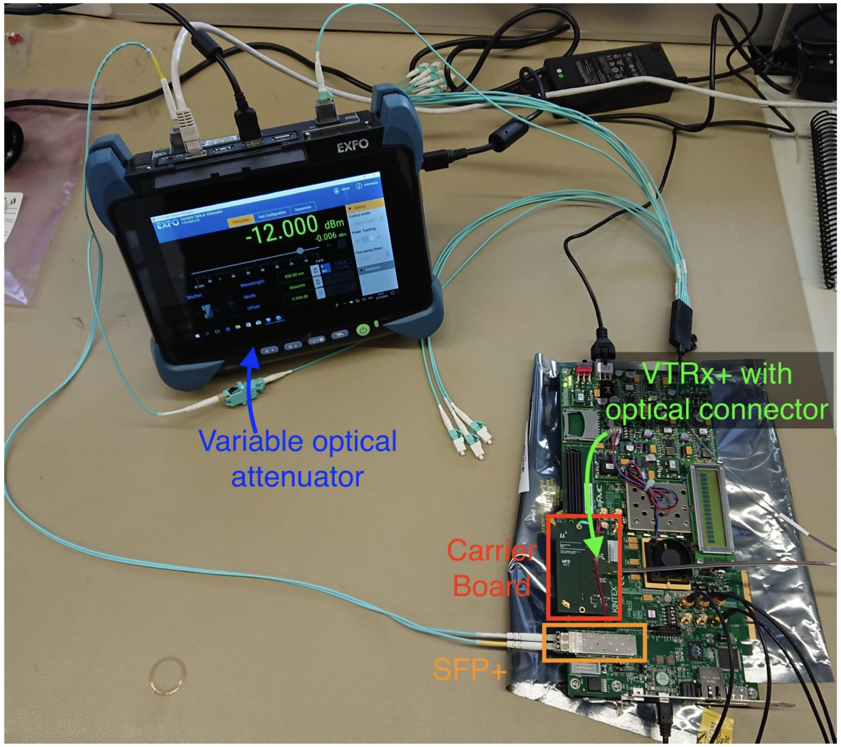
Layer types in the ITk Pixels

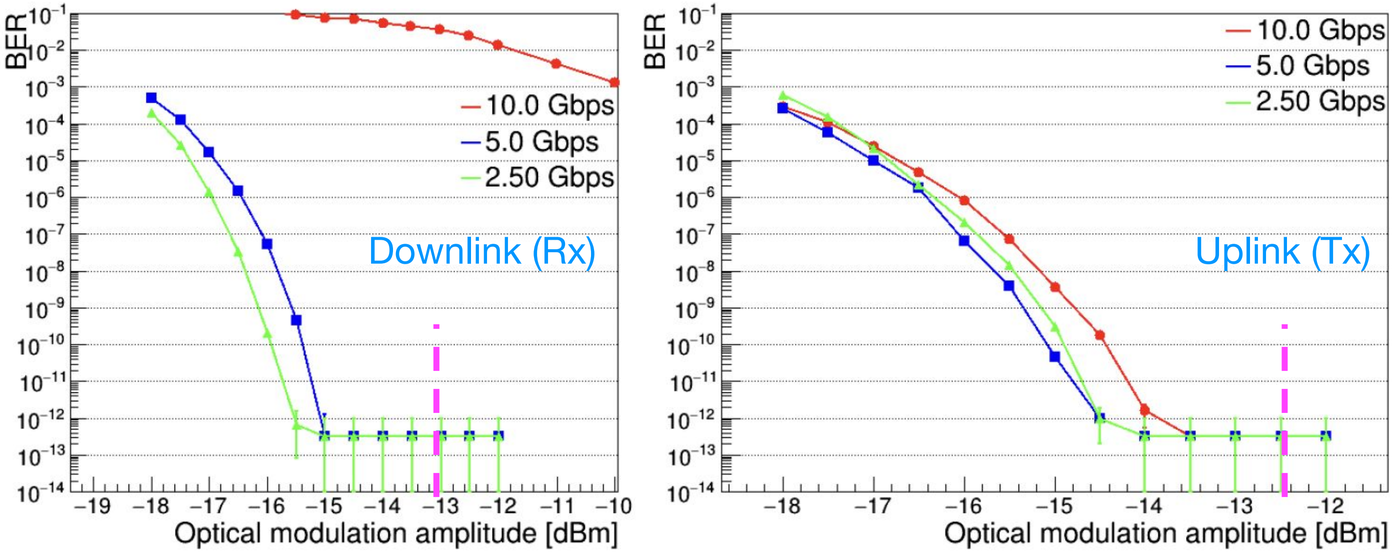
	electrical u/d	# active optical uplinks	#Optoboxes	#Optoboards in Optoboxes
IS 1L0+L1 (IS Barrel)	24/2	4	16	4, 7
	12/6	2		
IS L0+2L1 (IS Barrel)	24/2	4		
	12/6	2		
IS Coupled Ring	18/2	4	30	8
	9/1	4		
	20/5	4		
IS Intermediate Ring	18/3	4	6	8
	12/2	4		
IS Quad Ring	20/5	4	8	8
OB Flat Layer 2	12/6	2	16	6
OB Flat Layer 3	6/6	1	20	6, 7, 8
OB Flat Layer 4	6/6	1	24	6, 7, 8
OB Inclined Layer 2	16/8	4	24	6, 8
OB Inclined Layer 3	6/6	1		
	5/5	1		
OB Inclined Layer 4	8/8	2	20	4, 8
	6/6	1		
EC Layer 2 "1 MHz" (rings 6-11)	16/4	4	12	8
EC Layer 2 "4 MHz" (rings 1-5)	16/8	4	8	5
EC Layer 3	12/6	4	16	8
	10/5	4		
EC Layer 4 "flavour 1" (rings 1-7)	8/8	2	16	4, 8
	5/5	1		
EC Layer 4 "flavour 2" (rings 8-9)	16/8	4	4	8
	10/5	4		

Optimisation of the cable plant requires multiple flavours of fan-outs and shuffle boxes

VTRx+ tests

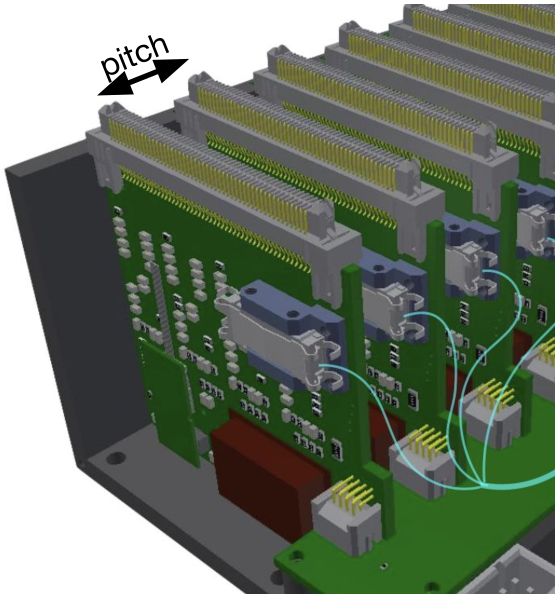
- V5 prototypes to test the data transmission performance
- Bit Error Ratio rate as a function of the signal strength
  - Both uplink and downlink reach required BER (10^{-12}) within the specs (dashed line in the plots)
- Smooth use of VTRx+ in our test setups, mounted on each Optoboard

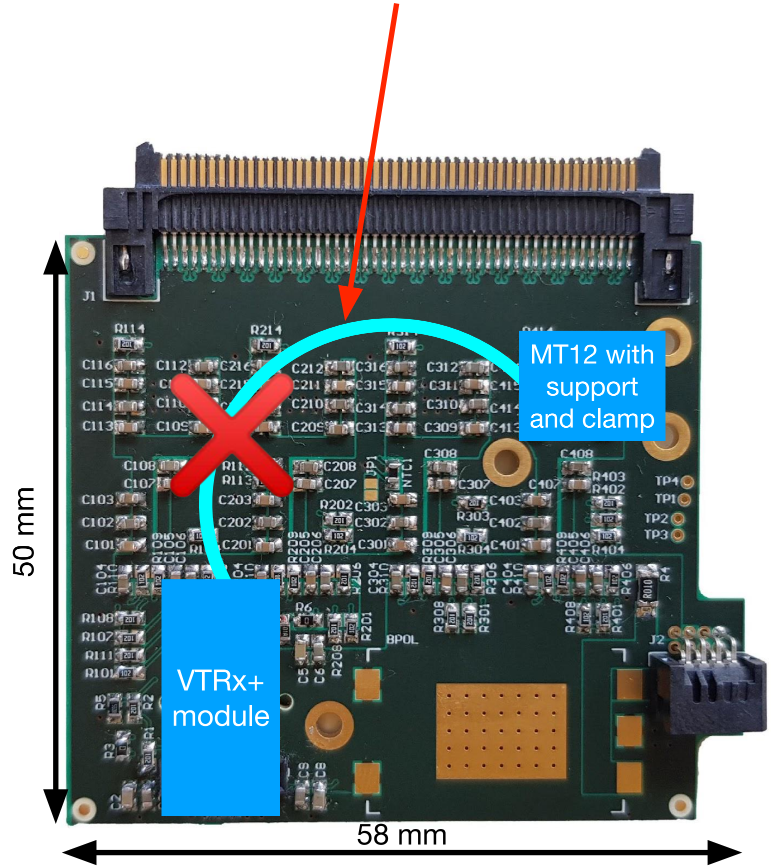


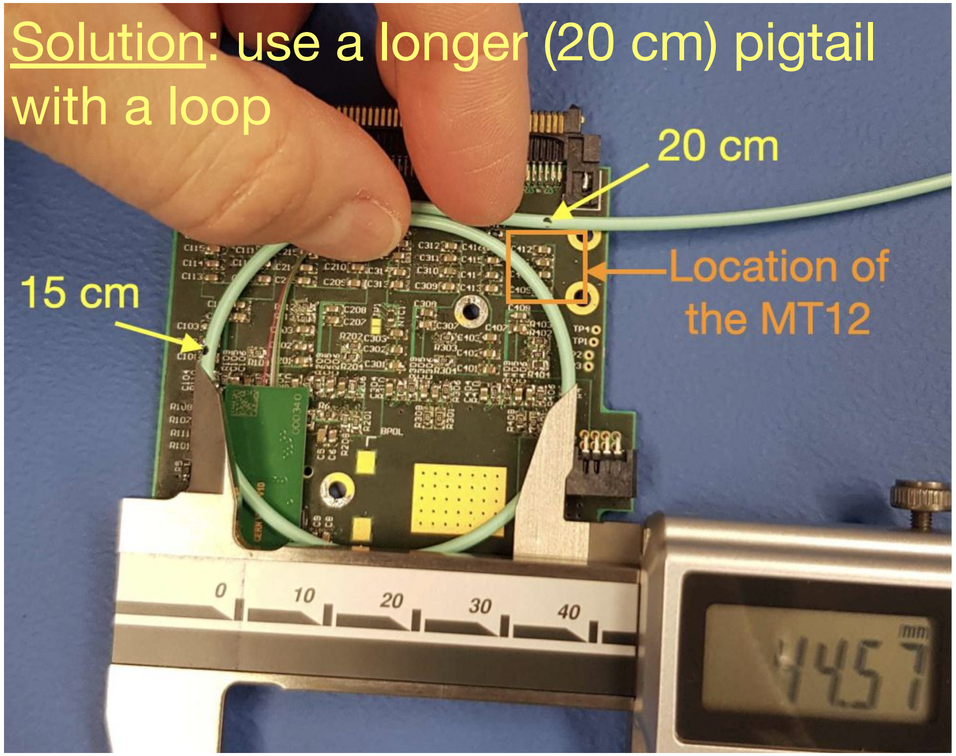


VTRx+ pigtail length

- Very limited space between the Optoboards to fit the VTRx+ pigtail
  - The Optoboard is 58x50 mm^2 and the VTRx+ module is 20-mm tall
  - The pitch between two Optoboards is 15 mm (excluding the Optoboard cooling profile — in the back of the board)
- Minimum bending radius and minimum length of the VTRx+ pigtail do not allow for single bend

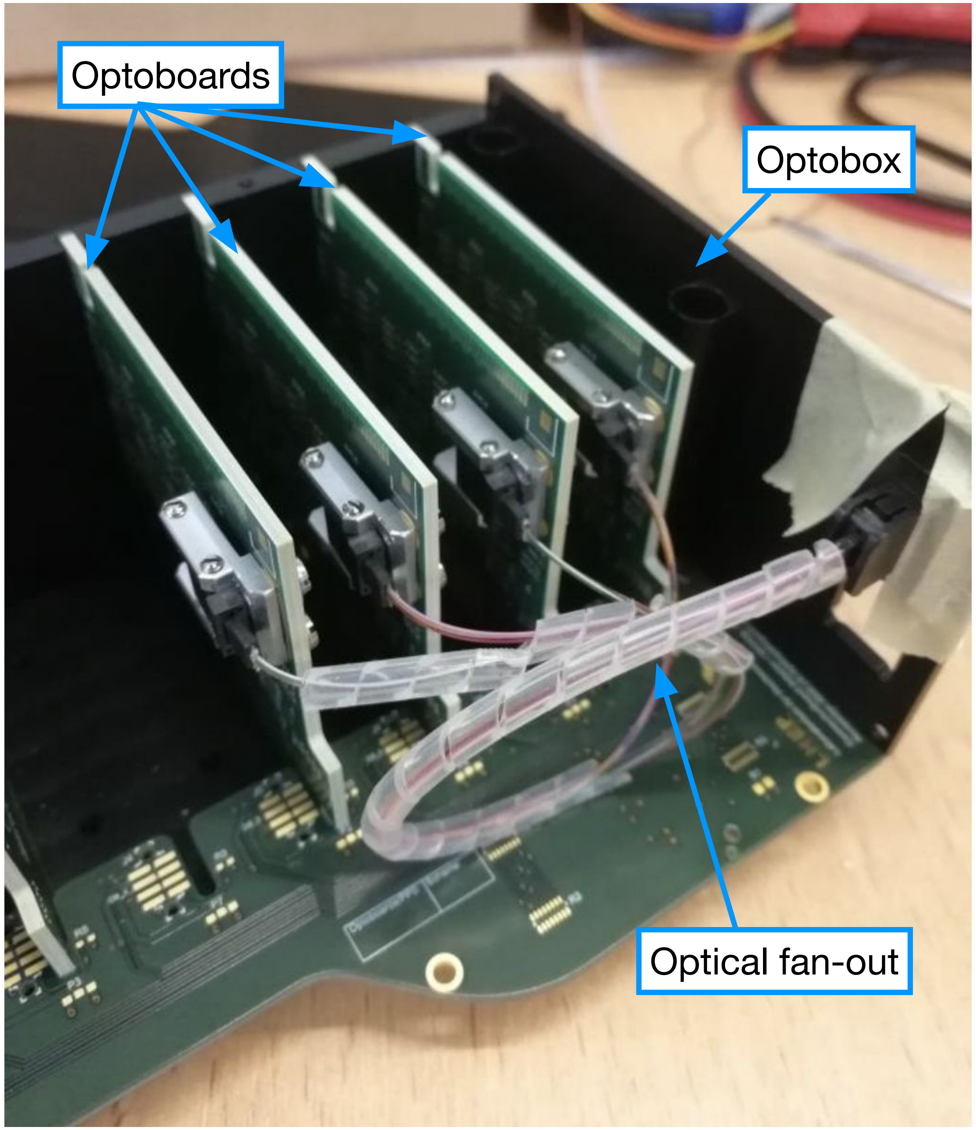


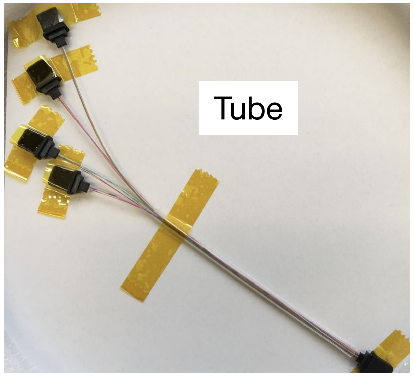


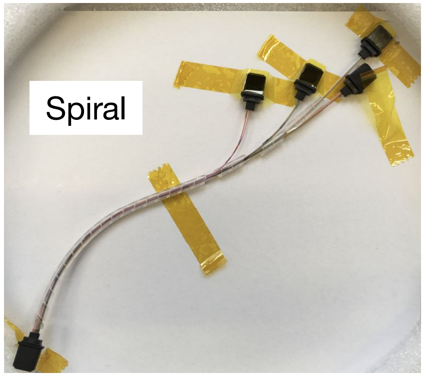


First prototype of optical fan-out

- Inside the Optobox
  - Mechanical tests to check if it fits
- Spiral shield is more convenient for our application
  - More flexible
  - Inside the Optobox, the fibres do not need special protection
- Currently at CERN in ATLAS ITk Pixel System test lab
  - First communication established between 7 Optoboards and FELIX card, through optical fan-out, 80-m trunk cable and (COTS) shuffle box

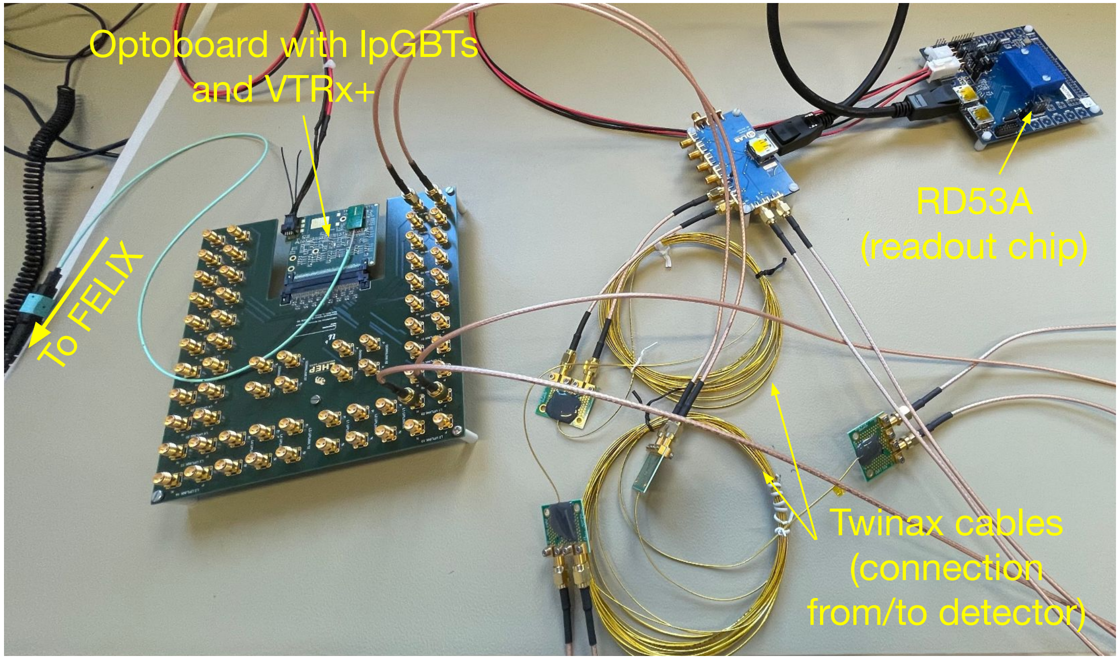




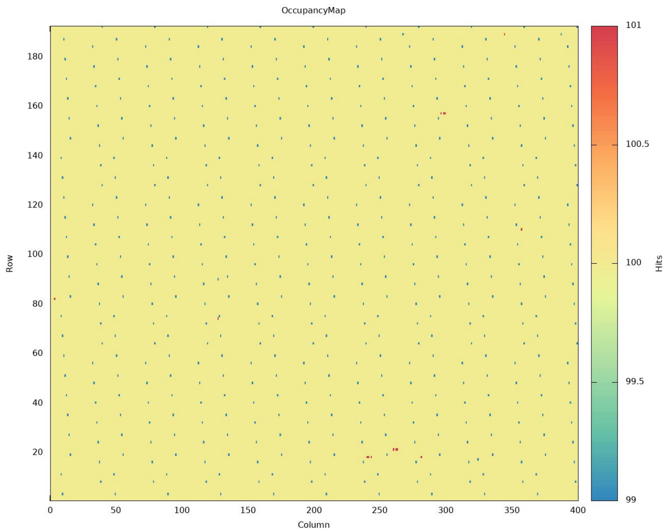


IpGBT & VTRx+ in the ITk data transm. chain

Entire ITk Pixel data transmission tested (from front-end chip to FELIX)



Successful digital scan!



Back-up slides

PCB count

Currently only lpGBT-v0 available

Needs for pre-production:

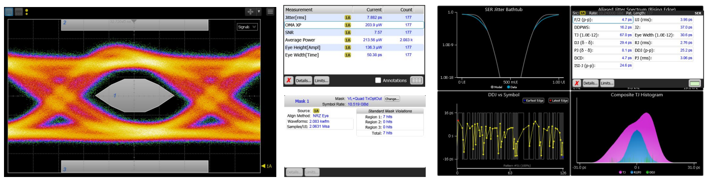
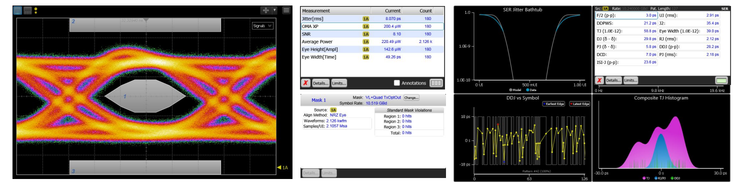
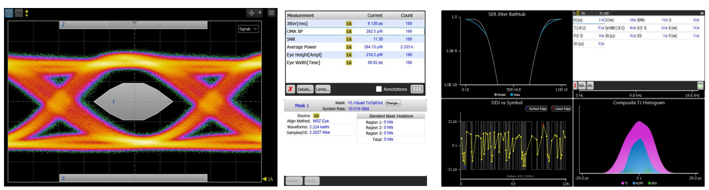
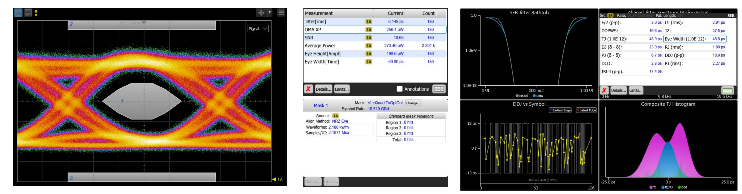
Needed pairs of EOS	vo			v1		
	SS	LS	Petals	SS	LS	Petals
PPA	2	2	4			
PPB	3	1	4	5	7	12
Total	5	3	8	5	7	12

Flavour		In hand		In population	Sum
		“Old”	“New”		
Stave master A-side	SS	12			12
	LS	9			9
Stave slave A-side	SS	4	2	2	8
	LS	8	2		10
Petal master		6	2	4	12
Petal slave		7	3	4	14

Summing depends on: “old” versions will be used → Enough for pre-production with lpGBT-v0
Population of remaining PCBs started after having passed the FDR-follow-up for petal
Spare stave_master PCB in case we get early the lpGBT-v1

Mounting Glenair-connector and e-fusing done on demand

Effect of the temperature on the uplinks

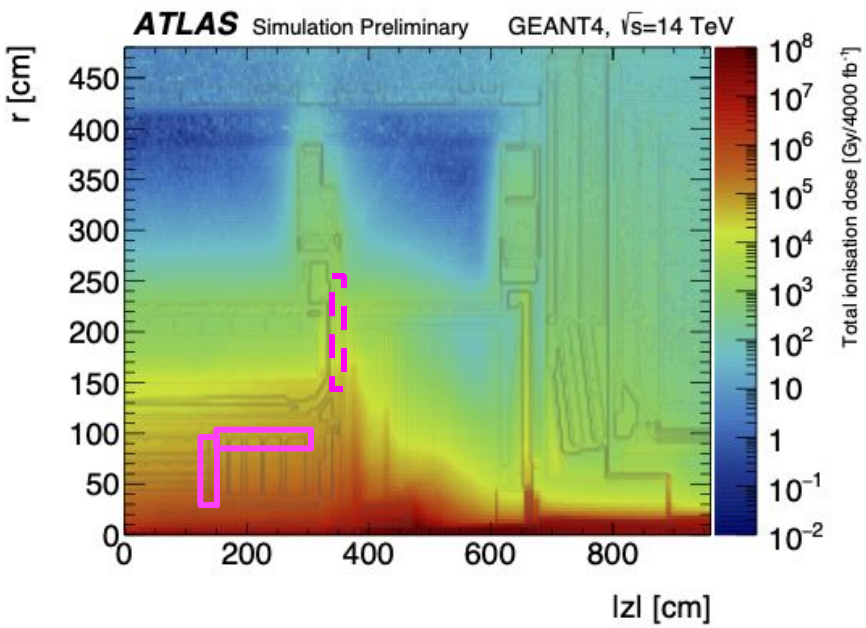
Environmental temperature	Tx1 "Rx-recovered clock"	Tx2 "Ref-clock"
-30 ^{0}C		
+10 ^{0}C		

QA - Optical eye-diagrams for 10Gb/s fibres

Measure with ~5dB additional attenuation

For all cold temperatures the BER was < 10^{-12}
Slightly better jitter for warm temperature

Radiation environment for the VL+ fibres in HL-LHC ATLAS



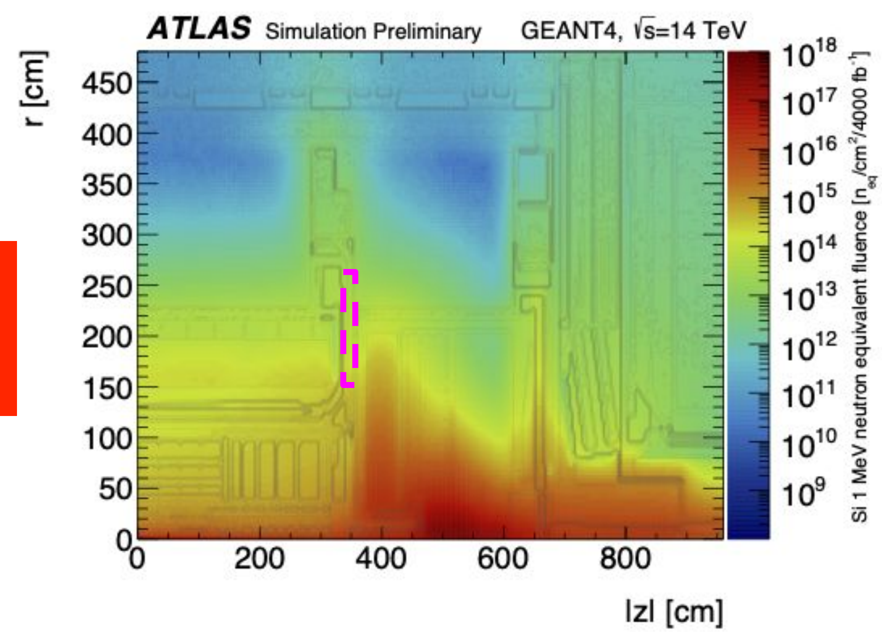
ITk Pixel VTRx+

ITk Strip XXX

LAr XXX

Muon XXX

Add here the position of the starting point of the fibres for the other detectors



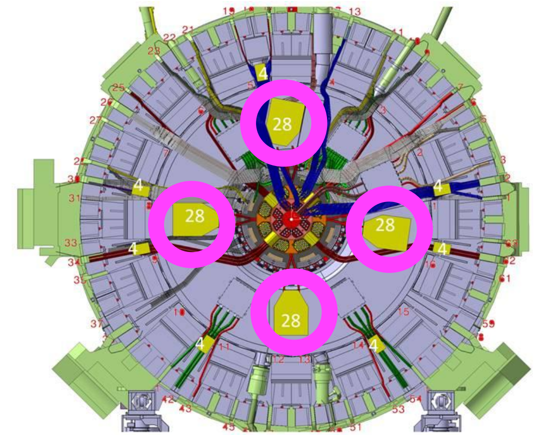
Types of Optoboards in ITk Pixel

	SP Chain types	Optoboard flavours			
		OB1		OB2	
		Upl.	Downl	Upl.	Downl
IS 1L0+L1 (IS Barrel)	L0-T	24	2	24	2
	L1-Q	12	6		
IS L0+2L1 (IS Barrel)	L0-T	24	2	24	2
	L1-Q	12	6		
	L1-Q	12	6		
IS Coupled Ring	EC0-T	18	2	9	1
	EC1-Q	20	5	20	5
IS Intermediate Ring	EC0-T	18	3	12	2
IS Quad Ring	EC1-Q	20	5	20	5
OB Flat Layer 2	short chain	12	6		
	long chain	12	6	12	6
OB Flat Layer 3	short chain	6	6		
	long chain	6	6	6	6
OB Flat Layer 4	short chain	6	6		
	long chain	6	6	6	6
OB Inclined Layer 2	half ring US	16	8		
	half ring USA	16	8		
OB Inclined Layer 3	half ring US	6	6	5	5
	half ring USA	6	6	5	5
OB Inclined Layer 4	half ring US	8	8	6	6
	half ring USA	8	8	6	6
EC Layer 2 "1 MHz" (rings 6-11)	half ring	16	4	16	4
EC Layer 2 "4 MHz" (rings 1-5)	half ring	16	8		
EC Layer 3	half ring	12	6	10	5
EC Layer 4 "flavour 1" (rings 1-7	half ring	8	8	5	5
EC Layer 4 "flavour 2" (rings 8-9	half ring	16	8	10	5

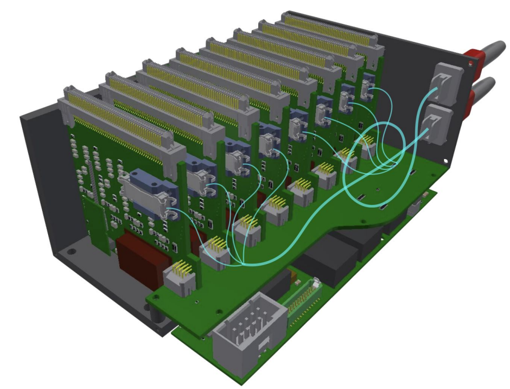
- Each line colour represents a part of the ITk Pixel detector that has independent mechanical structure
- Optoboard flavours = number of electrical uplinks and downlinks that are connected to an Optoboard
- For the same ITk Pixel part, different Optoboards may be needed

As shown later, this variety has implications on the optical section of the data transmission chain for ITk Pixel

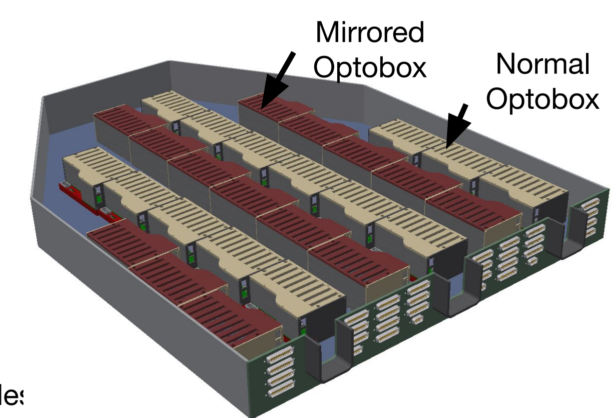
The Optosystem mechanics



- Located at z ~ ±3500 mm R~1500 mm
  - Radiation level ~ 15 Mrad (incl. safety factor ≥ 2)
  - *Rad-hard VTRx+, non-rad trunk cable*
- Organised in 4 Optopanels on each side



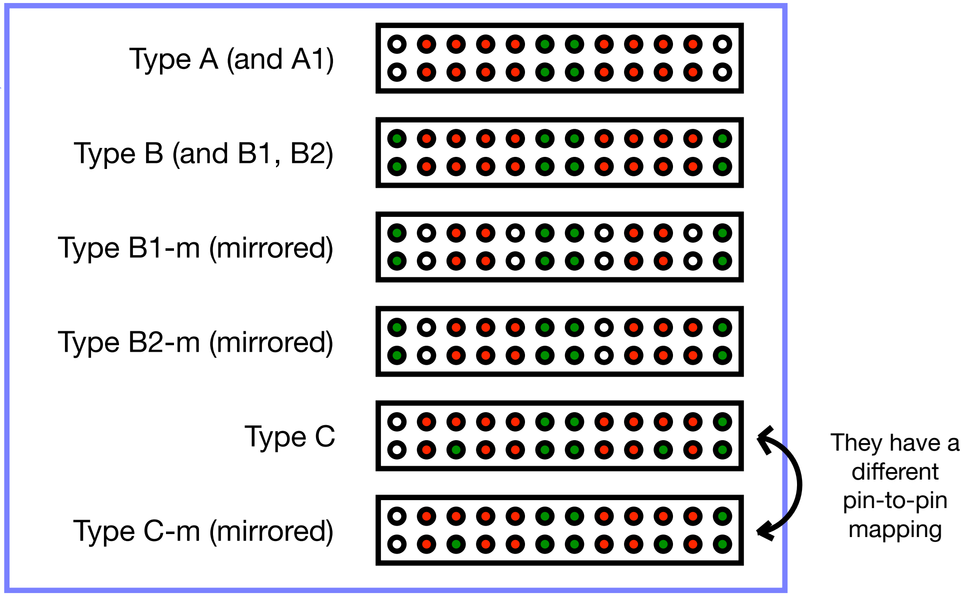
- Each Optobox has up to 8 Optoboards reading the same part of the ITk Pixel detector
- Each Optobox contains 1 or 2 optical uplinks
  - *Quantity depends on the number of active uplinks inside the entire Optobox and on the fan-out flavour*



- Each Optopanel hosts “normal" and “mirrored” Optobox versions to create twinax-only channels and fibres&power&monitor-cable channels
  - *Impact on the flavours of optical-fan-outs*

Flavours of optical components

- The variety of the electrical/mechanical part of the data transmission chain calls for an optimisation of the optical section
  - Goal: minimise the number of FELIX readout cards
    - minimise the number of active uplinks (reduced by optimisation of the electrical mapping between the detector and each Optoboard)
    - minimise the number of dark fibres (i.e. fibres that do not transport any signals)
  - Solution: have more flavours of the optical components. The current baseline is:
    - 6 optical fan-outs
    - 5 shuffle boxes



Shuffle box	#input connectors	#output connectors	Quantity (no spares included)
A	6	8	36
A1	3	3	8
B1	6	4	8
B2	5	5	8
C	6	7	4

Special case: fan-out type C

- The C-type fan-out connects
  - 2 Optoboards with 4 uplink fibres +
  - 6 Optoboards with a single uplink fibre
- The currently defined C-type fan-out has uplinks/downlink of the same VTRx+ in contiguous pin positions
- New idea
  - uplink/downlink of the same VTRx+ may be distant (see pink boxes)
  - would reduce number of shuffle boxes to 4 (-1 flavour)

fan-out C:	
1	
2	u
3	u
4	u
5	u
6	d
7	d
8	u
9	u
10	u
11	u
12	
13	d
14	u
15	d
16	u
17	u
18	d
19	d
20	u
21	u
22	d
23	u
24	d

new option?	
1	d
2	u
3	u
4	u
5	u
6	d
7	d
8	u
9	u
10	u
11	u
12	d
13	d
14	u
15	u
16	u
17	u
18	d
19	d
20	u
21	
22	
23	u
24	d

same VTRx+

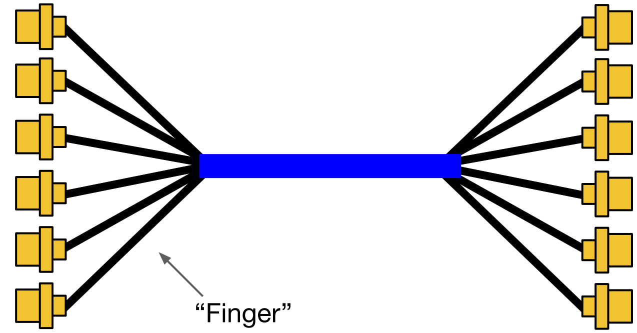
same VTRx+

Fan-out C								
B	A1	A2	A3	A4	A5	A6	A7	A8
1								
2	3							
3	4							
4	5							
5	6							
6	7							
7		7						
8		6						
9		5						
10		4						
11		3						
12								
13			7					
14			4					
15				7				
16				4				
17					4			
18					7			
19						7		
20						4		
21							4	
22							7	
23								4
24								7

new option?								
B	A1	A2	A3	A4	A5	A6	A7	A8
1					7			
2	3							
3	4							
4	5							
5	6							
6	7							
7		7						
8		6						
9		5						
10		4						
11		3						
12				7				
13			7					
14			4					
15					4			
16				4				
17						4		
18						7		
19							7	
20							4	
21								
22								
23								4
24								7

same colour (in each pinout) = same VTRx+

Trunk cable



- Link the fan-out at the Optobox walls to the shuffle box input
  - ~80-100 m in length
- 144 fibres, 6 MPO24 connectors per side
  - Each "finger" is 2.5-m long
  - 1 or 2 connectors per Optobox (depending on fan-out)
- 56 trunk cables used for the ITk Pixel detector
- Whenever possible, a trunk cable connects Optoboxes with the same type of fan-out
  - This helps the arrangement of the different shuffle box flavours in the electronics room

Example: A-side, Same colour in each Optopanel represents Optoboxes that are connected to the same trunk cable