lpGBT Project Status

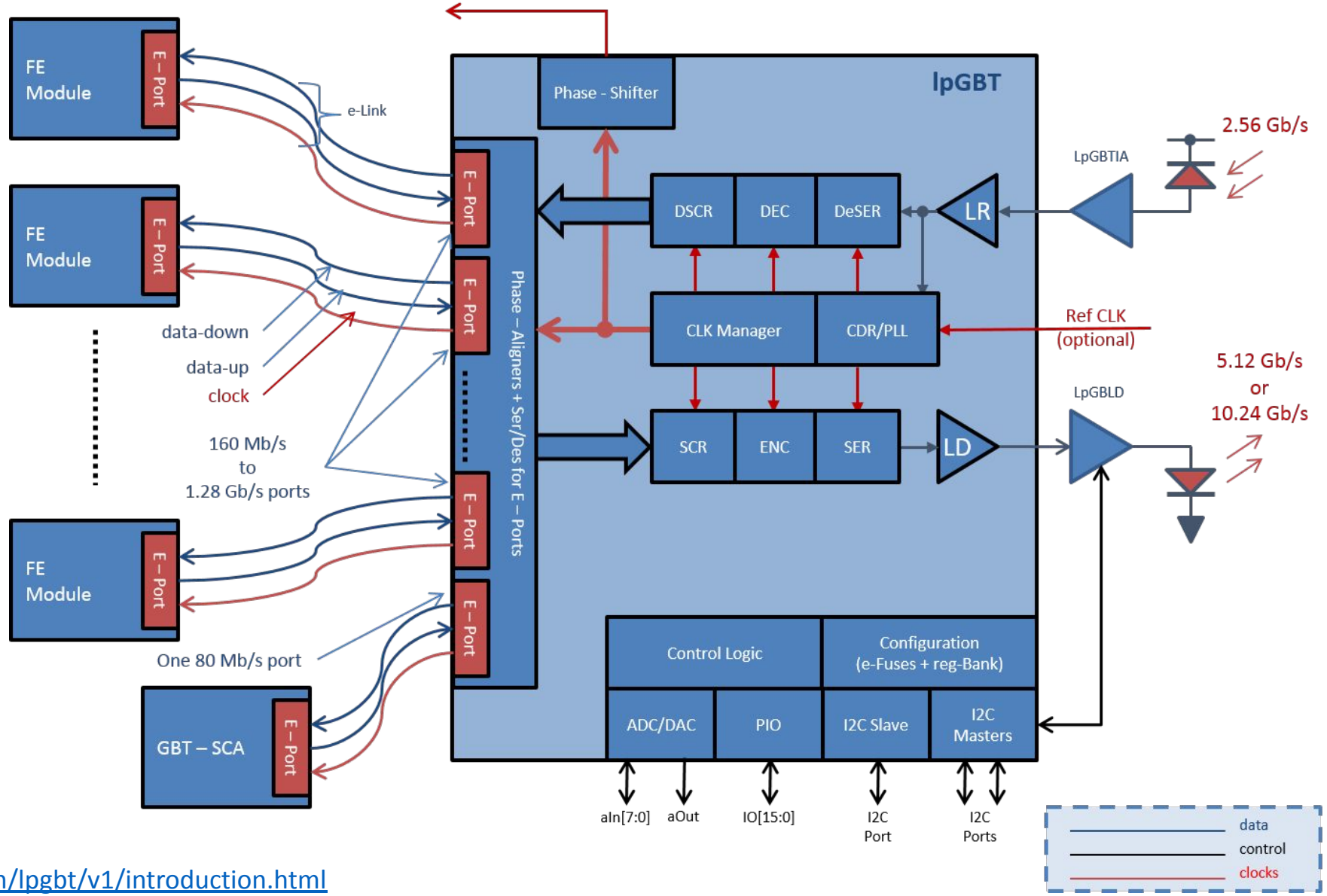
Szymon Kulis, on behalf of the lpGBT team

27 September 2021

TWEPP2021 Optoelectronics User Group Meeting

Contact: https://lpgbt-support.web.cern.ch/ or lpgbt-support@cern.ch

lpGBT architecture



https://lpgbt.web.cern.ch/lpgbt/v1/introduction.html

lpGBT team and contributors

lpGBT Design team

CERN, Geneva: Sophie Baron, Stefan Biereigel, Jose Fonseca, Rui Francisco, Iraklis Kremastiotis, Thanushan Kugathasan, Szymon Kulis, Pedro Leitao, Paulo Moreira, David Porret, Adithya Pulli, Ken Wyllie

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lpGBT Test team

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Macrocell contributors

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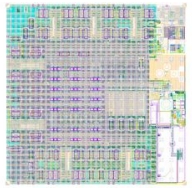
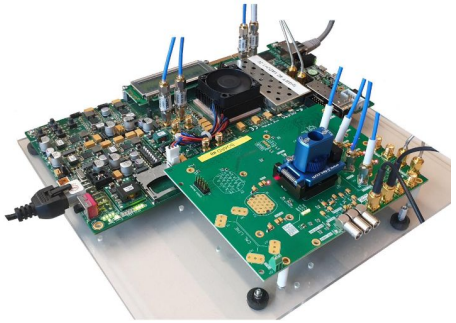
CERN, Geneva: Alessandro Caratelli, Iraklis Kremastiotis, Stefano Michelis

Timeline

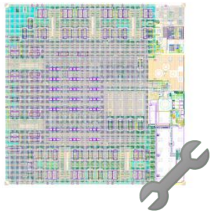
07/2018
lpGBTv0 submission



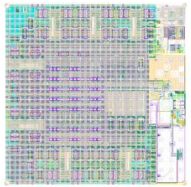


Q4 2018 - Q3 2019
Extensive testing:
- Functional
- Characterization
- SEE/TID

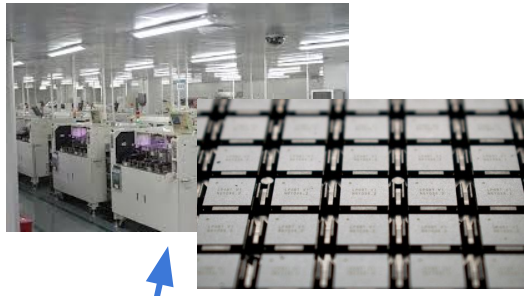
07/2019
lpGBTv1 redesign started



03/2021
lpGBTv1 submission

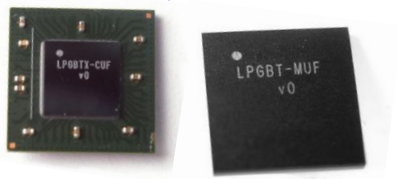


12/2021
lpGBTv1 production ramp-up



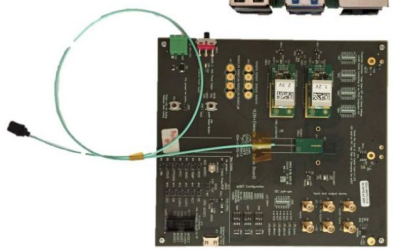
Today: 27/09/2021

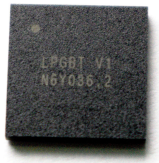
TIMELINE



11/2018 lpGBTv0
Prototypes @ CERN

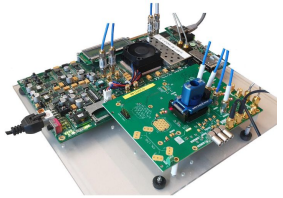
Q1 2019
Started the development of tools:
VLDB+ and piGBT





09/2021 lpGBTv1
Prototypes @ CERN

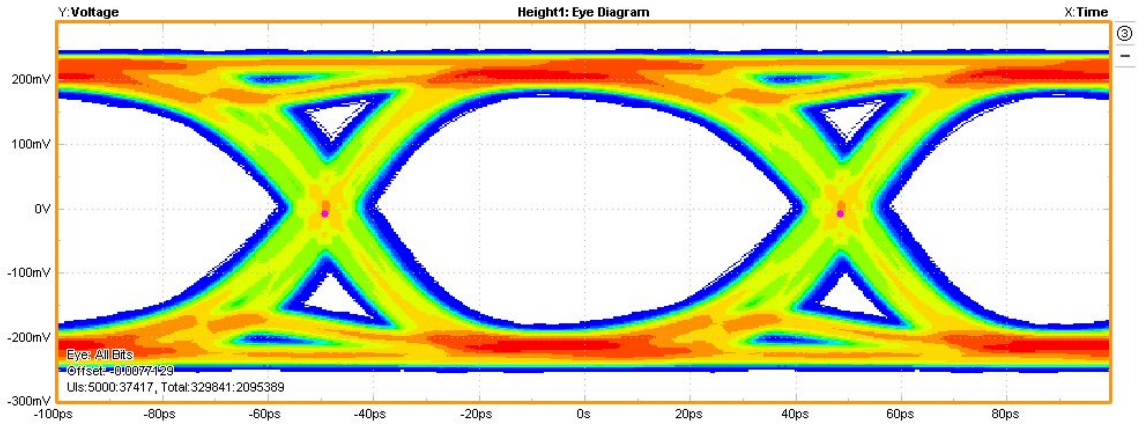
09/2021
lpGBTv1 functional validation and characterization



11/2021
lpGBTv1
TID and SEE characterization

lpGBTv0 prototype summary

- During the lpGBTv0 testing phase most of the design resources were put into testing:
  - The prototype was extensively tested during 2019
  - Analog and digital functionalities were successfully validated
  - Single-Event-Effect (SEE) tests and Total Ionizing Dose (TID) tests were performed
- Despite being fully functional, there were known shortcomings before submission (e.g. electromigration)
- Other issues were only identified during the TID and SEE radiation tests and this was the driver to respin the design



lpGBTv0 10.24 Gbps transmitter eye diagram; <20 ps jitter pk-pk

From lpGBTv0 to lpGBTv1

Function		lpGBTv0				lpGBTv1				
		Functionality	Performance	TID	SEU	Changes	Functionality	Performance	TID	SEU
ASIC Control	I2C Slave	✓	✓	✓	❗	🔨	✓	👍		
	IC channel	✓	✓	✓	N/A	🔨	✓	⏳		
	EC port	✓	✓	✓	N/A	🔨	✓	⏳		
	Brown-out detector	✓	❌	❌	N/A	🔨	✓	👍		
	Configuration memory	✓	✓	✓	❌	🔨	✓	⏳		
	eFuses	✓	✓	❌	N/A	🔨	✓	⏳		
	Startup & WatchDog	✓	✓	✓	✓	🔨	✓	👍		
	PowerOn Reset	✓	✓	✓	✓	N/A	✓	⏳		

Legend:

- ✓ Functionality/Performance good!
- ❗ Functionality/performance satisfactory but some aspects of it need improvement!
- ❌ Functionality/performance unsatisfactory and must be reviewed!
- N/A Does Not Apply or wasn't specifically tested.
- 🔨 Addressed issue in the lpGBTv1
- ⏳ Work in progress
- 👍 Work in progress (preliminary testing shows that the problems observed in lpGBTv0 were mitigated)

More complete list with issues description available on TWEPP2019 "The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC" by Paulo Moreira https://indico.cern.ch/event/799025/contributions/3486153

From lpGBTv0 to lpGBTv1

Function		lpGBTv0				lpGBTv1				
		Functionality	Performance	TID	SEU	Changes	Functionality	Performance	TID	SEU
ASIC Control	I2C Slave	✓	✓	✓	❗	🔨	✓	👍		
	IC channel	✓	✓	✓	N/A	🔨	✓	⏳		
	EC port	✓	✓	✓	N/A	🔨	✓	⏳		
	Brown-out detector	✓	❌	❌	N/A	🔨	✓	👍		
	Configuration memory	✓	✓	✓	❌	🔨	✓	⏳		
	eFuses	✓	✓	❌	N/A	🔨	✓	⏳		
	Startup & WatchDog	✓	✓	✓	✓	🔨	✓	👍		
	PowerOn Reset	✓	✓	✓	✓	N/A	✓	⏳		

🔨 **I2C Slave:** A mistake prevented the I2C slave to be accessed once one of the triplicated A/B/C clocks were disabled. The I2C slave has been redesigned.

🔨 **IC channel / EC port:** SerialControl frame structure updated. Updated EC port to introduce multi-drop configuration and tri-state operation (1).

🔨 **Brown-out detector:** Circuitry was improved to reduce the comparator offset dispersion between the 3 BOD circuits.

🔨 **Configuration memory:** Changed the asynchronous set/reset load signals, which are susceptible to SET, to synchronous load signals.

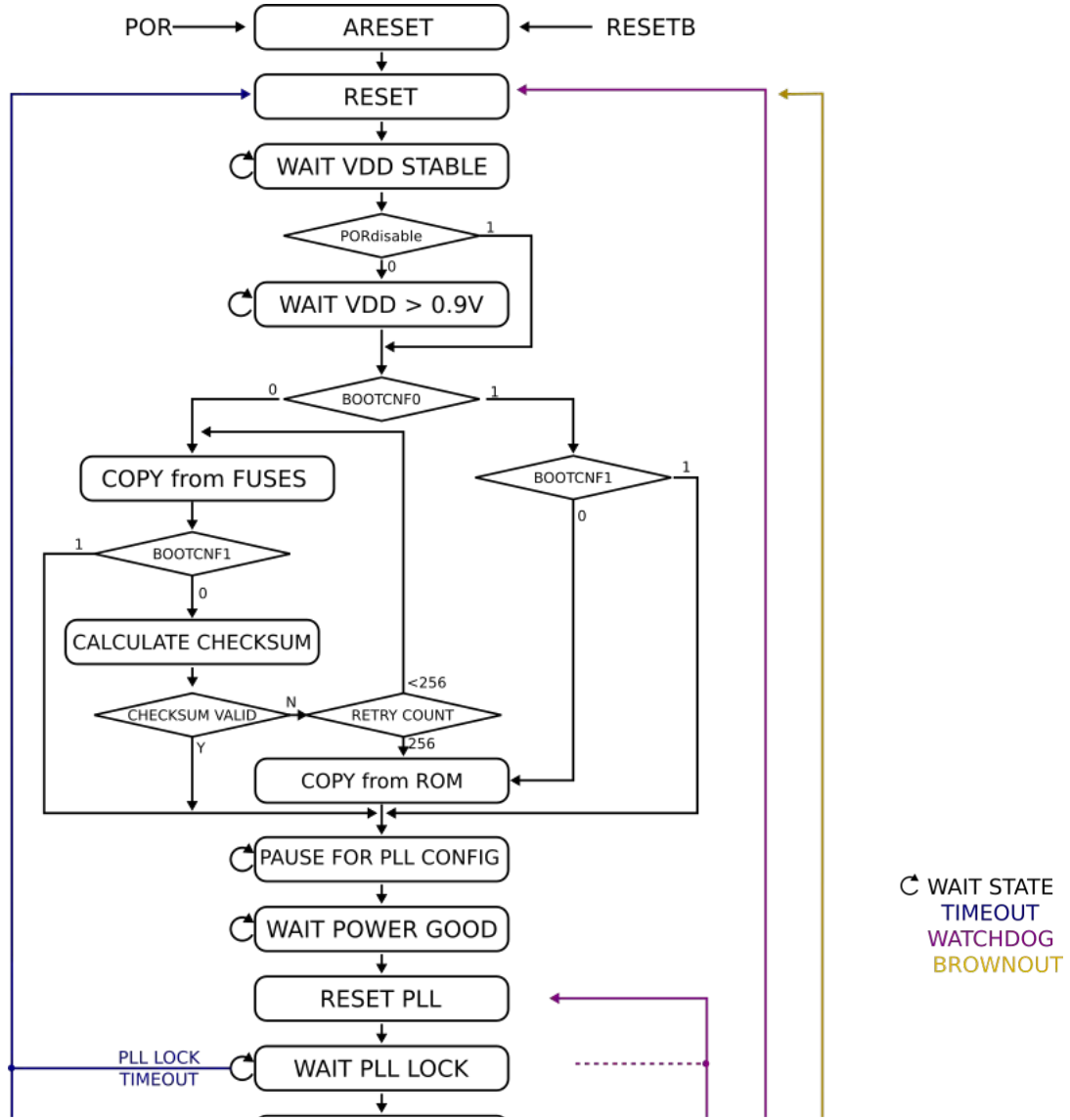
🔨 **eFuses:** Instead of redesigning the eFuse block we have redesigned the power-up state machine to include a predefined Read-Only-Memory (ROM) and Cyclic-Redundancy-Check (CRC) (more on the next slide)

🔨 **Startup & WatchDog:** Updated the power-up state machine to include the ROM and CRC

(1) https://lpgbt.web.cern.ch/lpgbt/v1/configuration.html#ec-channel-multi-drop-bus

ROM and CRC on the power-up state machine

- **BOOTCONF[1:0]** pins (replacing **VCObypass** and **SC_I2C**) control the chip is initialization.
  - **ROM start-up**: the basic functions are initialized to default values letting the chip ready for detailed configuration via the IC-channel, the EC-port or I2C-port.
  - **Fuse start-up**: a CRC checksum is used to verify if the fuses have been correctly read. In case of 256 consecutive failures, the chip switches to ROM start-up.



From lpGBTv0 to lpGBTv1

Function		lpGBTv0				lpGBTv1				
		Functionality	Performance	TID	SEU	Changes	Functionality	Performance	TID	SEU
HS Transmitter	TX datapath @ 5.12 Gbps	✓	✓	✓	✓	N/A	✓	✓		
	TX datapath @ 10.24 Gbps	✓	✓	✓	✓	N/A	✓	✓		
	PRBS Generators	✓	✓	✓	N/A	N/A	✓	✓		
	HS data loopback	✓	✓	N/A	N/A	N/A	⏳	⏳		
HS Receiver	Equalizer	✓	✓	✓	✓	N/A	✓	⏳		
	Frame Aligner	✓	❗	✓	✓	🔨	✓	⏳		
	Rx datapath @ 2.56 Gbps	✓	✓	✓	✓	N/A	✓	⏳		
	Eye Opening Monitor	✓	✓	N/A	N/A	N/A	✓	✓		
	PRBS Checkers	✓	✓	N/A	N/A	N/A	✓	✓		

🔨 **Frame Aligner:** The 2.56 Gbps frame-aligner state-machine was redesigned to be more robust against unlock situations with a faster locking time.

From lpGBTv0 to lpGBTv1

Function		lpGBTv0				lpGBTv1				
		Functionality	Performance	TID	SEU	Changes	Functionality	Performance	TID	SEU
ePortRx	Deserializer	✓	✓	❗	❗	🔨	✓	✓		
	Phase-Aligner	✓	✓	✓	✓	🔨	✓	✓		
	PRBS Checkers	✓	✓	N/A	N/A	N/A	✓	✓		
	eRx	✓	✓	✓	✓	N/A	✓	✓		
	eRx+equalization	✓	✓	✓	✓	N/A	✓	⏳		
ePortTx	Serializer	✓	✓	✓	✓	N/A	✓	✓		
	PRBS Generators	✓	✓	N/A	N/A	N/A	✓	✓		
	Mirror function	✓	✓	✓	✓	N/A	✓	✓		
	eTx	✓	✓	✓	✓	🔨	✓	👍		
	eTx+pre-emphasis	✓	✓	✓	✓	🔨	✓	👍		

🔨 **ePortRx's deserializer and phase-Aligner:** The circuit's performance showed to be marginal within the TID specification by having non-reliable data transmission at higher TID for 1.28 Gbps. The circuitry was improved by increasing the timing slack to accommodate TID induced degradation.

🔨 **eTx:** The circuit's performance has been improved as part of the overall effort to decrease the deterministic jitter

From lpGBTv0 to lpGBTv1

Function		lpGBTv0				lpGBTv1				
		Functionality	Performance	TID	SEU	Changes	Functionality	Performance	TID	SEU
Experimental control and monitoring	I2C master (x3)	❗	❗	❗	N/A	🔨	✓	👍		
	GPIO	✓	✓	✓	✓	N/A	✓	✓		
	ResetOut	✓	✓	✓	✓	N/A	✓	✓		
	Reference voltage	✓	✓	❗	N/A	🔨	✓	👍		
	Temperature sensor	✓	✓	✓	N/A	N/A	✓	⌛		
	8[12]-bit Voltage DAC	✓	✓	✓	N/A	N/A	✓	⌛		
	8-bit Current DAC	✓	✓	✓	N/A	N/A	✓	⌛		
	10-bit ADC	✓	✓	✓	N/A	🔨	✓	👍		

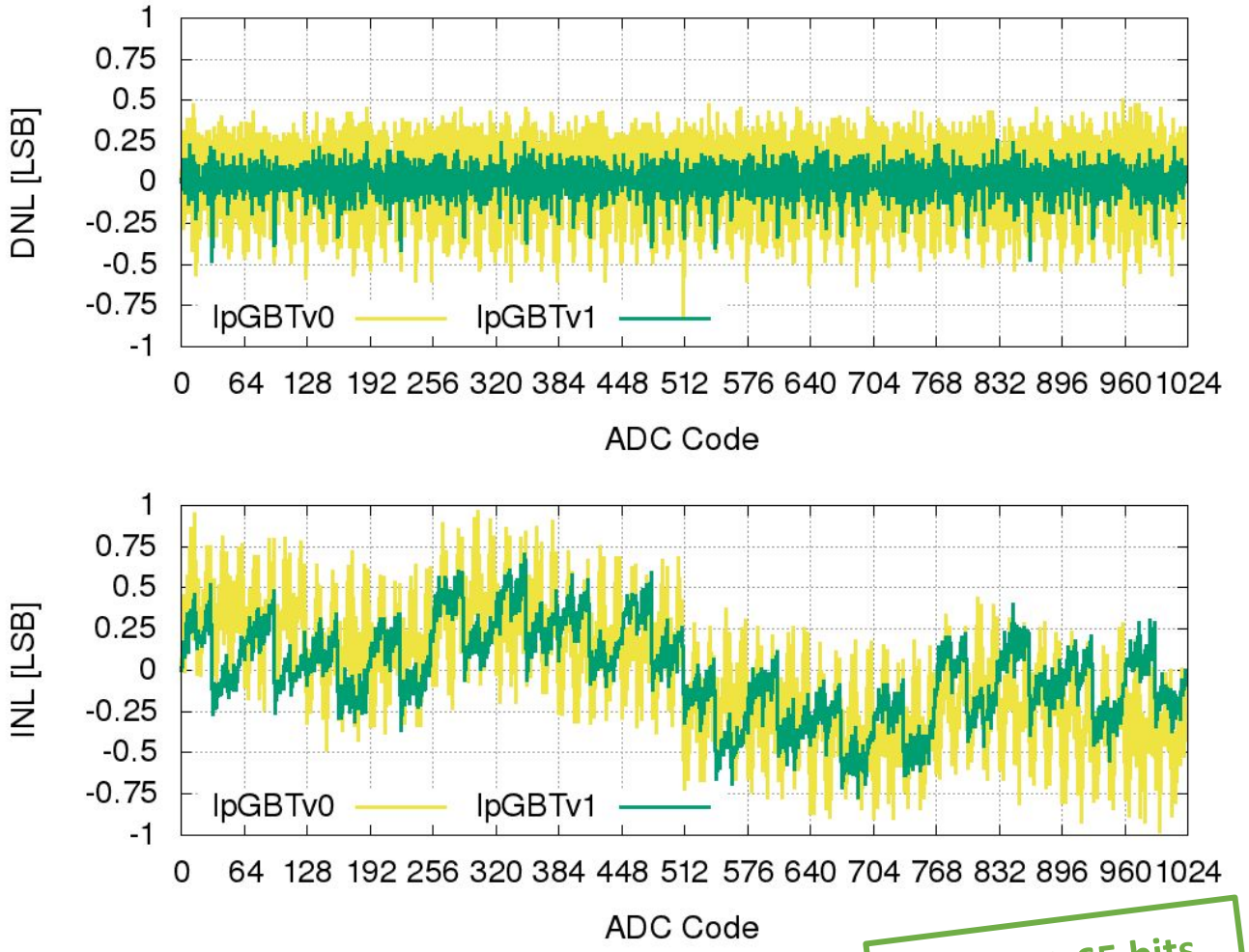
🔨 **I2C masters:** The I2C masters typical yield for lpGBTv0 was of 43%. This was due to a timing constraint which is now corrected.

🔨 **Reference voltage:** The circuit's tuning range was optimized.

🔨 **ADC:** The circuit's performance was optimized to improve the linearity and increase ENOB.

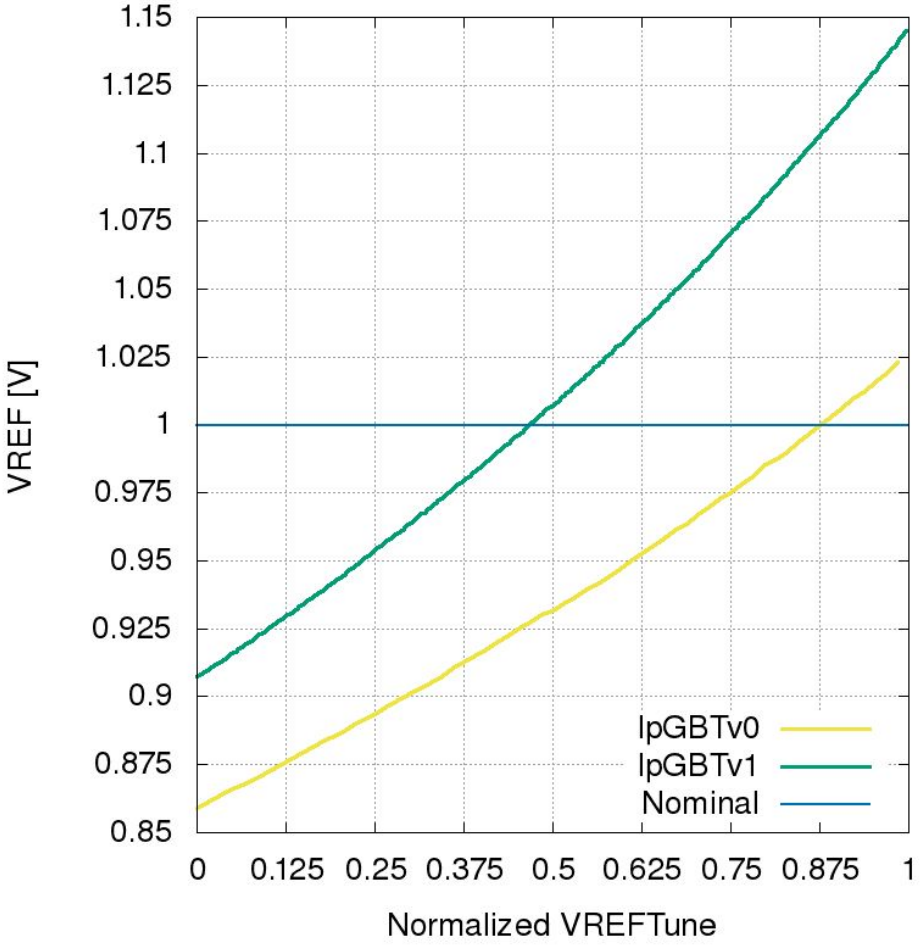
lpGBTv1 ADC and VREF performance

ADC Linearity measurement



ENOB: 9.65 bits

Reference voltage tuning



From lpGBTv0 to lpGBTv1

Function		lpGBTv0				lpGBTv1				
		Functionality	Performance	TID	SEU	Changes	Functionality	Performance	TID	SEU
Process Monitor and Testing	Ring oscillator (x4)	✓	✓	✓	N/A	N/A	✓	⏳		
	SEU Monitoring Memory	✓	✓	N/A	✓	N/A	✓	⏳		
	TMR Testing	❗	N/A	N/A	N/A	🔨	✓	👍		
Power	1.2V (+/- 10%)	✓	✓	✓	✓	N/A	✓	⏳		
Clock Performance	eClocks	✓	❗	❗	✓	🔨	✓	👍		
	phaseShifter	✓	❗	❗	✓	🔨	✓	👍		
	PLL Clock Performance	✓	✓	✓	❗	🔨	✓	👍		
	CDR Clock Performance	✓	✓	✓	❗	🔨	✓	👍		

🔨 **TMR testing:** The I2C slave prevented the test of this feature.

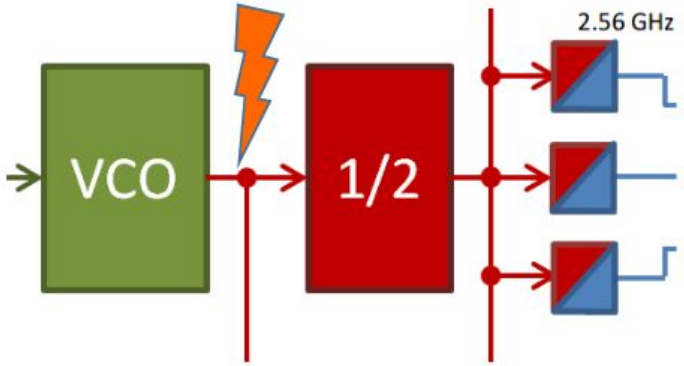
🔨 **CDR/PLL Clock performance:** The feedback loop showed to be sensitive to SEE causing phase jumps in the 200 ps range (more in the next slides).

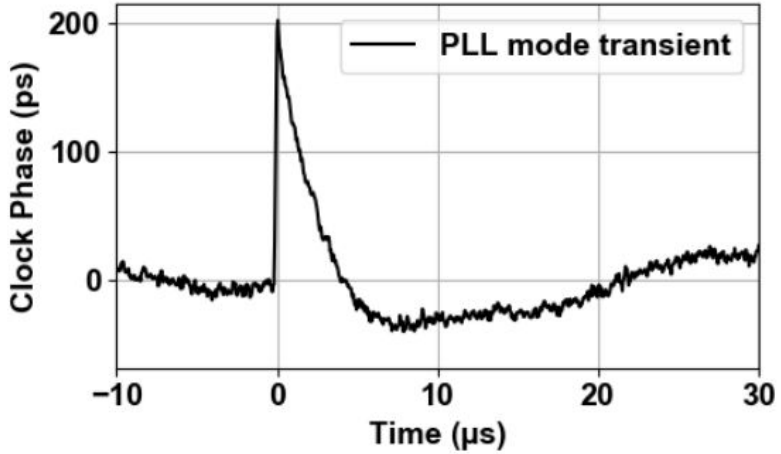
🔨 **eClocks and phaseShifter clock Performance:** The lpGBTv0 suffers from deterministic jitter which relates to the 40 MHz activity in the chip (more in the next slides).

PLL and CDR Clock SEU Performance

Two error mechanisms in the PLL/CDR were identified during SEE testing.

1. In receiver/transceiver/transmitter mode:
   - 200 ps phase jumps in the output clocks which could cause data transmission errors
   - Traced to the non-triplicated clock buffers
   - They have been triplicated in the lpGBTv1





For more details please see: Stefan Biereigel et al. *"The lpGBT PLL and CDR Architecture, Performance and SEE Robustness"* at https://indico.cern.ch/event/799025/contributions/3486152

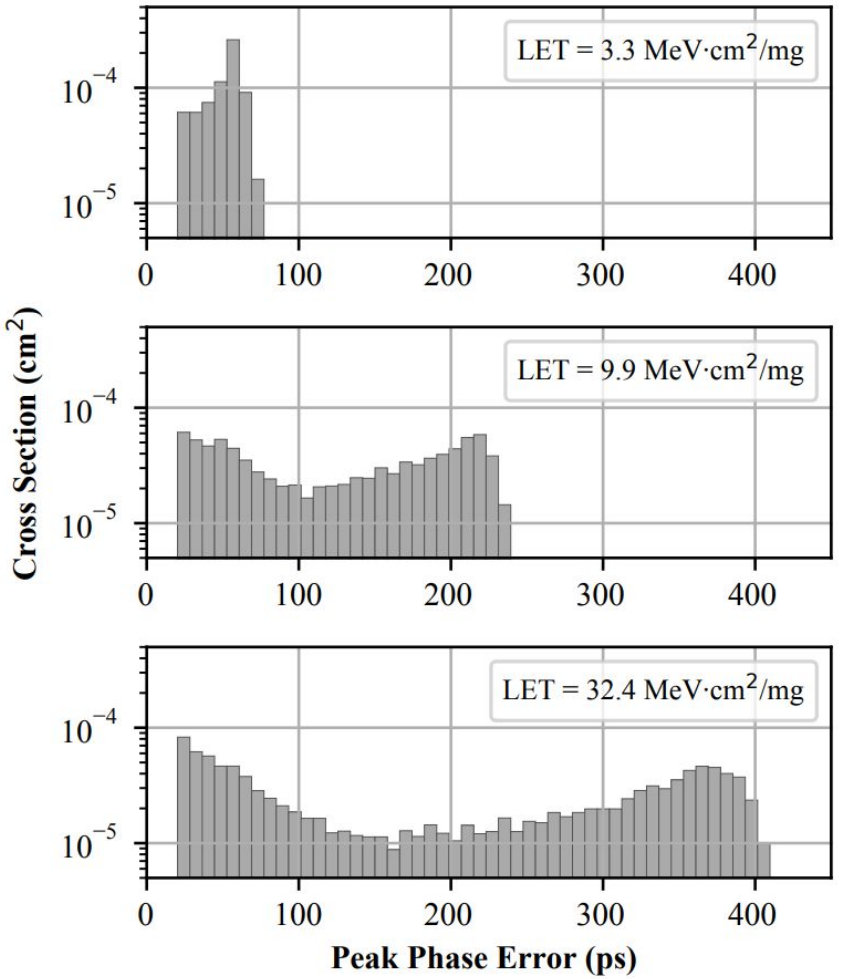
PLL and CDR Clock SEU Performance

2. Transmitter mode only (PLL mode):

- Up to 400 ps phase transients on the output clocks present in Heavy Ion experiment (might be not representative for LHC environment)
- Peak phase error depends on the PLL loop settings and LET
- Hypothesis: charge deposited in the dielectrics surrounding the inductor
- Detailed characterization of this effect was performed for lpGBTv0
- No mitigation was introduced for lpGBTv1
- This effect does not affect data transmission
- For timing detectors, it is recommended to use the lpGBT in transceiver or receiver modes

For more details please see: Stefan Biereigel et al. *"Single-Event Effect Responses of Integrated Planar Inductors in 65 nm CMOS"* in review.

Distribution of the peak clock phase error stimulated by heavy ion (lpGBTv0).



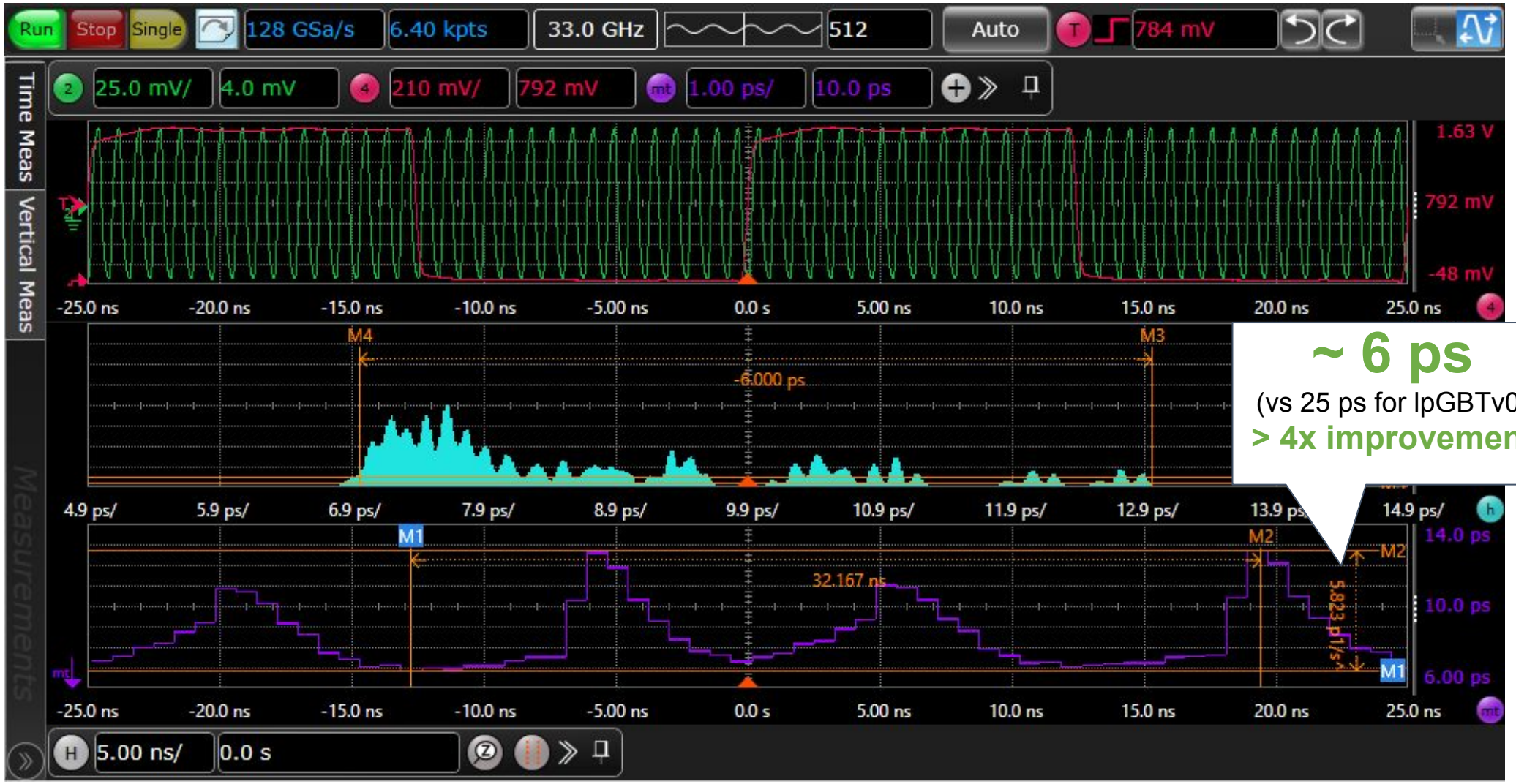
lpGBTv1 eclock performance

eclock operating at 1.28 GHz

Clock waveforms

Time Interval Error (TIE) Histogram

Time Interval Error (TIE) Trend



~ 6 ps

(vs 25 ps for lpGBTv0)

> 4x improvement

Deterministic component repeats with the 40 MHz clock in the lpGBT

lpGBTv1 status summary

- **All lpGBTv1 features (tested so far) appear functional**
  - Data transmission
    - high speed links (various data rates, FEC modes)
    - electrical links (various data rates)
  - Start up methods (fuses, ROM)
  - Configuration methods (I2C, IC, EC)
  - GPIO, reset out
  - Data generators and checkers
- **The performance of all modified blocks seem to be improved**
  - Deterministic jitter, eTx, brown-out detector, ADC, Vref generator, eTx
- Systematic characterization is starting (various power supplies, climatic chamber)
- **TID and SEE campaigns needed to fully qualify the chip**

Main changes from the user point of view

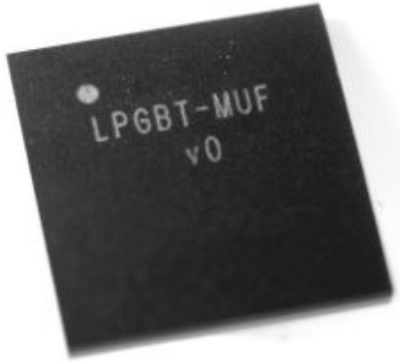
- Pin changes:
  - **SLSDA**, **SLSCL** and **RSTN** have internal pull-up instead of pull-down
  - **M[2:0]SDA**, **M[2:0]SCL** I2C master pins have internal pull-ups instead of pull-down
  - **TSTCLKINN** and **TSTCLKINP** have been renamed to **RSV0** and **RSV1** (not used)
  - **VCOBYPASS** replaced by **BOOTCNF0**
  - **SC_I2C** replaced by **BOOTCNF1**
  - **STATEOVRD** replaced by **EDINECTERM** (enables termination of EC port)
- Configuration block and power-up state machine redesigned:
  - Addition of Read Only Memory (ROM)
  - Addition of Cyclic Redundancy Check (CRC)
  - Register map has been extended and various fields and bits were moved around.
- Multi-drop communication over EC-channel bus
- Serial Control (IC/EC) channel frame structure updated

Complete list available on: https://lpgbt.web.cern.ch/lpgbt/v1/changelog.html

lpGBT Manual(s)

- Both manuals for v0 and v1 are available: https://cern.ch/lpgbt
  - lpGBTv0 manual will be phased-out once the lpGBTv1 becomes available
  - lpGBTv1 manual is regularly updated

lpGBTv0



Prototypes available. The manual is stable. Only minor corrections and clarifications are expected.

lpGBTv1

Prototypes **NOT** available. The manual (and the chip) might change frequently. Use **strictly** for preview of future functionality and pinout.

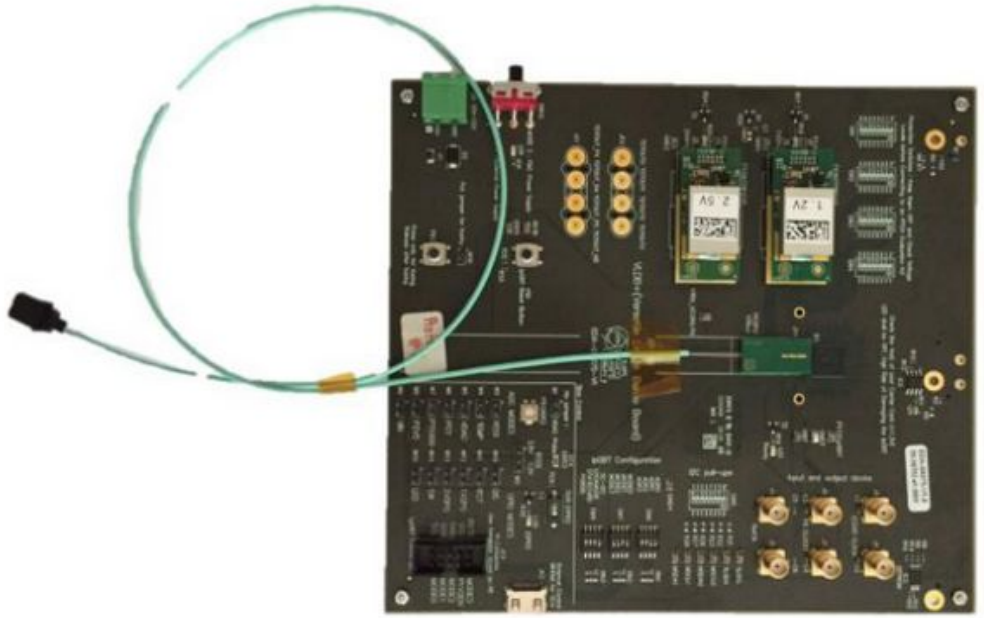
lpgbt_control_lib

- A python library that unifies the configuration and control of the lpGBT ASIC
  - Could be used as a reference for non-python developments
- Implements access methods (“drivers”) for all the lpGBT components
- All configuration interfaces (I2C, EC, IC) of the chip are conceptually supported
  - The implementation of these low-level protocols is to be performed by the library user (examples provided)
- Used by the lpGBT team for functional testing, characterization and production testing
- Contains built-in documentation
- Compatible with lpGBTv0 and lpGBTv1
  - Differences between two versions are “hidden” from the user behind unified interface
  - The lpGBTv1 support is being debugged now, a stable release is expected by the time chips are distributed to the users
- Available at: https://gitlab.cern.ch/lpgbt/lpgbt_control_lib

VLDB+

VLDB+ v2:

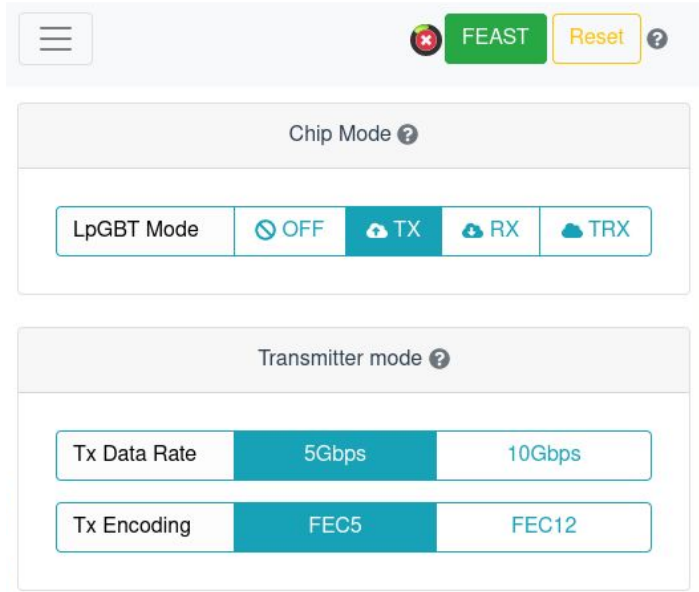
- All known issues from VLDB+ v1 successfully addressed
  - Improved high frequency signals integrity
- Compatible with lpGBTv1
- Almost 40 VLDB+ delivered to users (between VLDB+ V1 and V2 with lpGBTv0)
- 50 VLDB+ v2 PCBs are ready. Will be assembled as soon as first lpGBTv1 chips are available



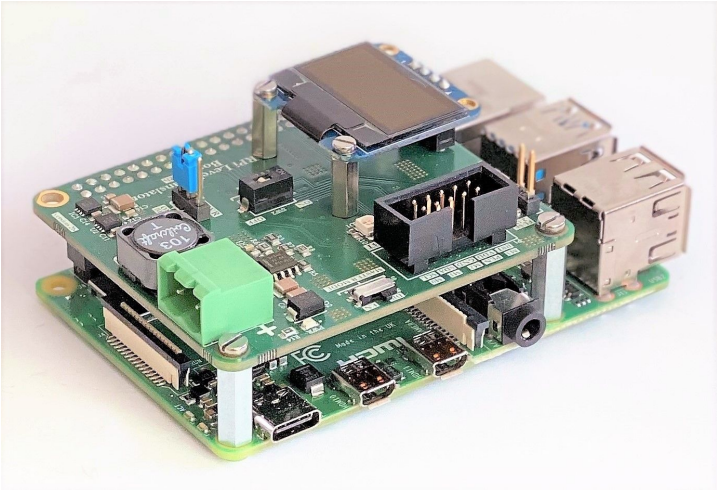
Website/manual/orders: https://vldbplus.web.cern.ch

piGBT

Virtual tour available at:
https://pigbt.web.cern.ch/



- Interfaces with the lpGBT to:
  - Control the chip
  - Program the eFuses
- Implements a “web server” and control is done through a web browser
- Knows how the registers relate to each other and to the modes of operation, preventing the user from doing configuration mistakes
- 40 toolkits delivered to users
- Software V1.3 under development
  - Will use lpgbt_control_lib (for lpGBTv1 support)
  - Will improve the user interface
- Website and manual:
  - https://pigbt.web.cern.ch



Package contents:

1 Raspberry Pi 4
1 Translator board V2b
1 Raspberry PI to LpGBT ribbon cable

Production testing

- The production testing of lpGBTv1 will be done by a subcontractor
- The final hardware is in fabrication
- List of the lpGBT features covered:
  - Uplink and downlink data path at all data rates
  - All eport (rx & tx) data rates exercised
  - All eport clk and phase shifter frequencies exercised
  - Analog peripheral (DAC, ADC, VREF)
    - Calibration will be performed at two temperatures (room temperature and -30C) and results will be stored in efuses
  - Various configuration modes:
    - I2C port
    - IC channel
    - EC channel
  - I2C masters
  - GPIO, POR, BOD and the process monitor oscillators

For more details please see: Nour El Houda Guettouche et al. *"The lpGBT production testing system"* at https://indico.cern.ch/event/1019078/contributions/4444294/

lpGBT schedule and availability

- lpGBTv0: 850 chips distributed (no chips left!)
- lpGBTv1:
  - Submission: **10 March 2021**
  - Prototypes @ CERN: **14 September 2021**
  - Functional testing: **14 September 2021** - … (no problems found so far)
  - Detailed characterization: **October 2021**
  - In house testing of small quantity of chips:
    - A few hundreds chips available to users
    - Only for early adopters (e.g. will not contain full calibration data, no XRAY/SEE results available, etc.)
  - X-ray and SEE testing: end of **November 2021**
  - (pre)production testing at subcontractor: **December 2021**
    - ~6k chips available to users: Q1 2022 (?)
  - Additional **12k** chips in pipeline waiting for confirmation from tests
  - Wafer production start: **December 2021** *)

    *) providing that functional, XRAY,SEE, and (pre)production testing does not reveal any problems
    - Assuming foundry delivery times from the pre-crisis era, production complete in **Q4 2022**. But the foundry has already announced wafer shortage in 2022, so delays are highly likely.
- To keep up to date with the project schedule refer to https://ep-ese.web.cern.ch/content/lpgbt-vl-dcdc-schedule

Please inform your electronics coordinator of your lpGBTv1 needs (date and quantity) for 2021/2022 as soon as possible