Tuesday 5 October 2021
TWEPP 2021 User Group meetings

CERN ASIC Support news and EP R&D WP5 developments

Alessandro Caratelli

CERN

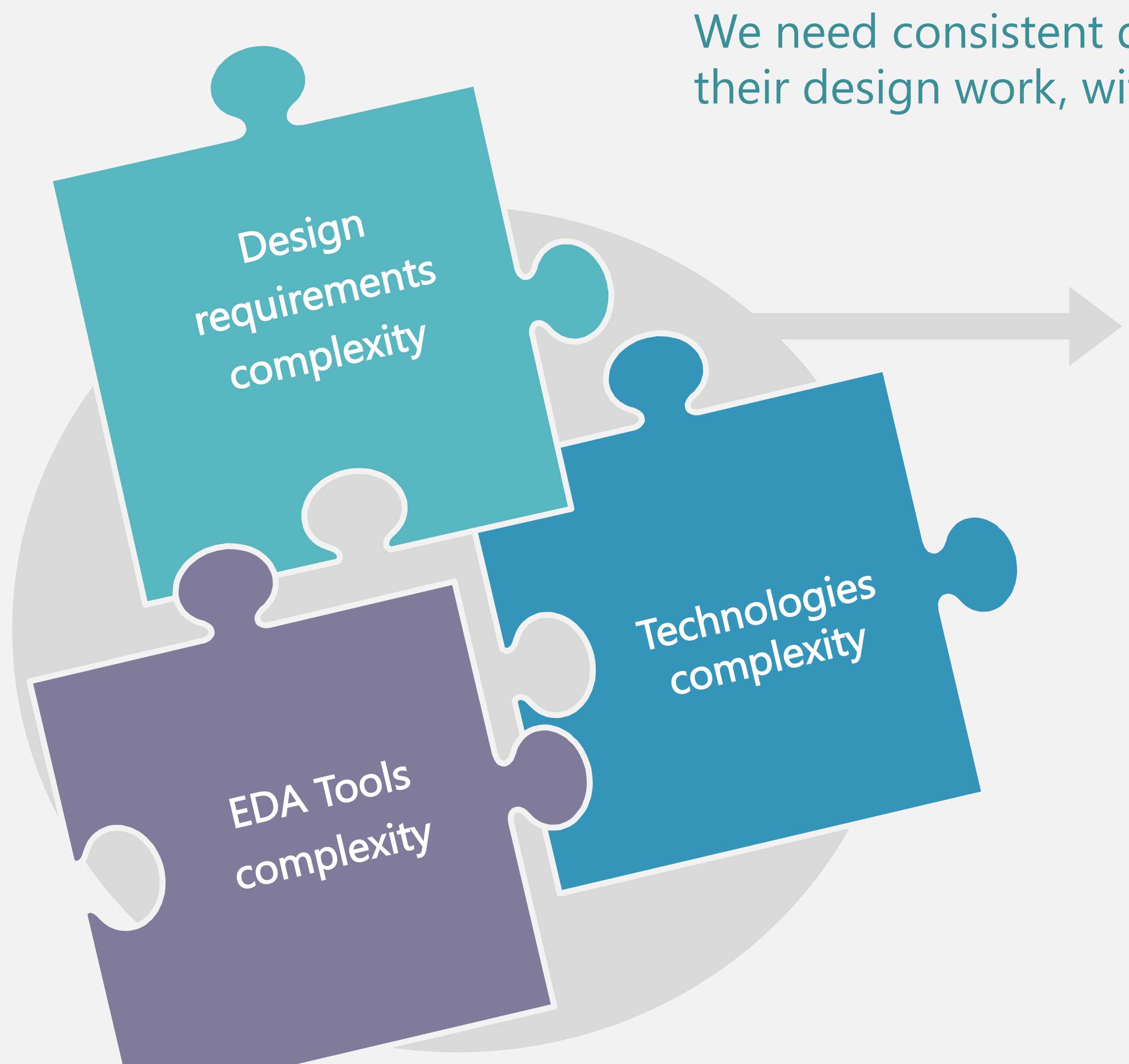
EP-ESE

AGENDA:

- ASIC Technology Support for HEP institutes
- Updates for 130nm & 65nm common design platforms
- 28nm common design platform, technology access and design sharing framework
- EP R&D WP5 – 28nm technology radiation evaluation and IP blocks

ASIC Technology Support for HEP projects

We need consistent desing platforms so that the design teams can focus on their design work, without having to resolve the same integration tasks



ASICs Technology Support

- Develop and maintain *common ASICs Design Platforms*
- Provide *technology and EDA tool support* to designers
- Distribution and maintenance of specific macro blocks and design flows of general use
- Organize and *provide training*
- Provide *support to HEP community* for selected technologies

Foundry Access Services

- Establish *Commercial Contracts* with silicon vendors
- *Establish NDAs*[1] that allow for collaborative work
- Organize & coordinate *silicon fabrication*

Responsible: K. Kloukinas > 20 years service

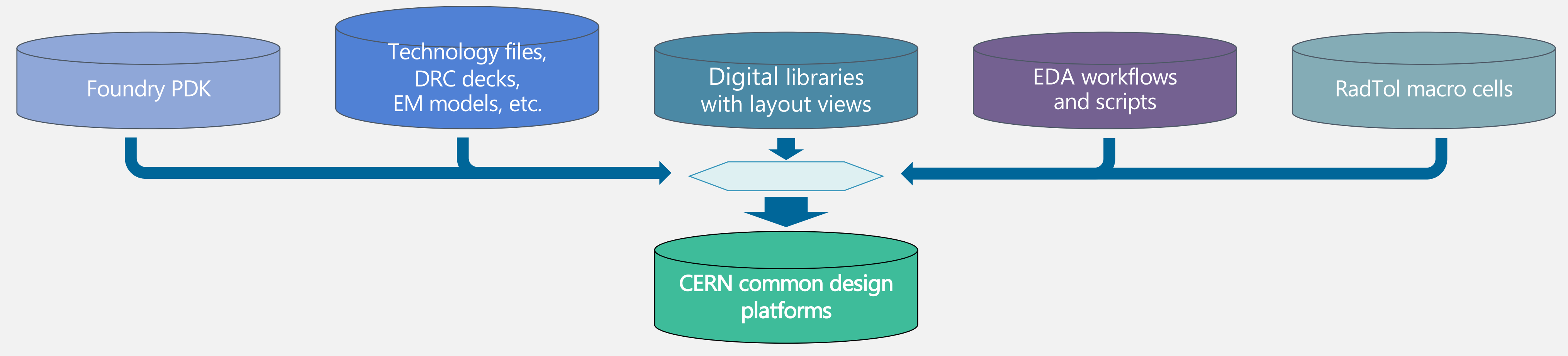
ASIC Technology Support for HEP projects

Kostas Kloukinas	Technology support & Foundry Services coordinator
Wojciech Bialas	Computing infrastructure and EDA tools
Alessandro Caratelli	ASICs technologies and EDA tools support
Marco Andorno	ASICs technologies and EDA tools support
Alessandra Fioriti	ASICs technologies and EDA tools support (unfortunately Alessandra recently changed project)

Common design platforms

The CERN design platform including the release of the Mixed Signal Design Kits for multiple design nodes:

- Provides a common platform to consolidate all technology nodes on the same design flows
- The design platforms are adapted to provide → common design approach →
  - Exchange and support collaborative work
  - Interoperability within the HEP community avoiding incompatibilities across design teams
  - Optimize efforts to integrate a “design environment”
- Minimize differences when moving from one node to another so that the designers do not need to train on multiple methodologies
- The design kits are updated following all the major foundry releases
- Every year the design kits are tested and eventually adapted to support the latest EDA tools Europractice release



Common design platforms

2020/2021 design-kits updates summary:

FOUNDRY 1

130nm 8RF-DM

Cost efficient technology for Mixed-Signal designs

1 Metal stacks supported

STABLE

28nm

High density, High performance technology.

1 Metal stacks (1p8)

Future evaluation

- PDK available
- No active work at the moment

FOUNDRY 2

130nm HPC

Cost efficient technology for Mixed-Signal designs

2 Metal stacks (1p7 and 1p8)

Major updates

- Last release T_v2.6_CERN_v3.1 (Nov. 2020)
- Last update Semptember 2021

65nm LP

High performance technology

3 Metal stacks (1p6 ,1p7, 1p9)

Minor updates

- Last update Feb 2021

28nm HPC

High density, High performance technology.

1 Metal stacks (1p8)

New design kit 2020

- Last update December 2020

28nm HPC+

High density, High performance technology.

1 Metal stacks (1p9, evaluating 1p8)

New design kit 2021

- Last update September 2021

Legacy Common Design Platforms updates

Foundry-2 130nm
Last release V3.1 (Dec. 2020)

[Major release available via IMEC QUERIO platform]

- Added ***1p8 6x1z1u*** metal stack support in addition to the 1p7
- Techfile update:

  The former CERN design kit custom techfile based on the Foundry-2 techfile **v2.4a** was updated and merged with the information from the latest Foundry techfile **2.6b** release of 2020
- Added ICT and qrcTechFiles for *Electro-migration* (EM) analysis in Voltus or Voltus-Fi
- Fixed LVS issues on digital standard cells
- PVS LVS and Extraction deck added to the PDK
- PVS DRC Rules update
- Calibre Dummy Fill rules update
- Added Metal slot Calibre file in the PDK
- Fix M8 routing issues for Cadence Innovus

- Update of Calibre LVS, PEX and extraction rules for 8 metal stack.
- Fixed qrcTechFile
- Fix VIA area discrepancy between qrcTechFile in different corners
- Add AP layer as routing and extraction layer in both metal stacks
- Wire Bond and Bumping Rules Update
- Updated CERN IO pads, comprehensive of .lib files
- Documentation update
- Prepared and tested with:
  - Cadence Virtuoso **v. IC_6.1.7.823**
  - Cadence Genus/Innovus/Tempus/Voltus **v. 19.10**

Legacy Common Design Platforms updates

Foundry-2 65nm
Last release V2.0 (2019) – minor updates patch V2.1 (2021)

[Patch release available via CERN ASIC support]

- EM models (ICT and qrcTechFile) for Voltus and Voltus Fi
- Update of Calibre PEX rules for 1p6 and 1p9 metal stacks
- Update Calibre DRC deck
  - Design Rules, Antenna, wire-bond and bumps ules
- Minor digital library fix
- Documentation update
- Working with:
  - Cadence Virtuoso **v. IC_6.1.7** and **v. IC_6.1.8**
  - Cadence Genus/Innovus **v.19.10** and v.20.10

The 28nm common design platform

The CERN-HEP 28nm Common Design Platform

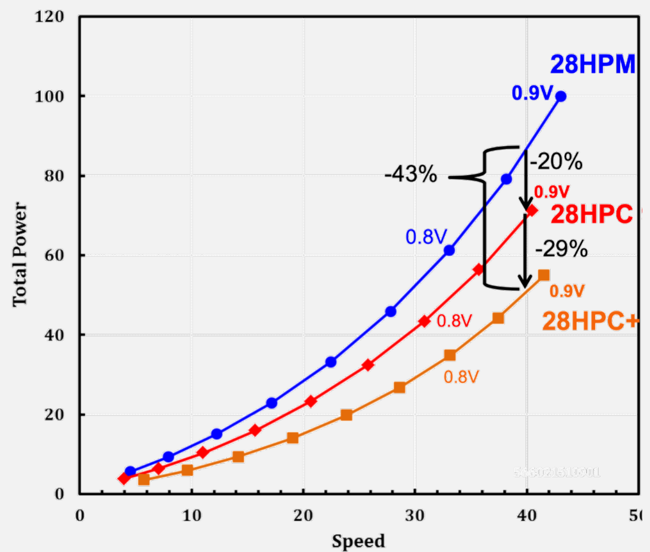
- Foundry PDK
- Digital standard-cell libraries including physical views
- NDAs Commercial contract Framework for collaborative design
- A growing set of macro-cells and RadTol IP blocks
- Several limited-access technology files
- Additional settings and environment setup
- Design workflows for analog, digital and mixed-signal design
- Support for specific EDA tool platforms

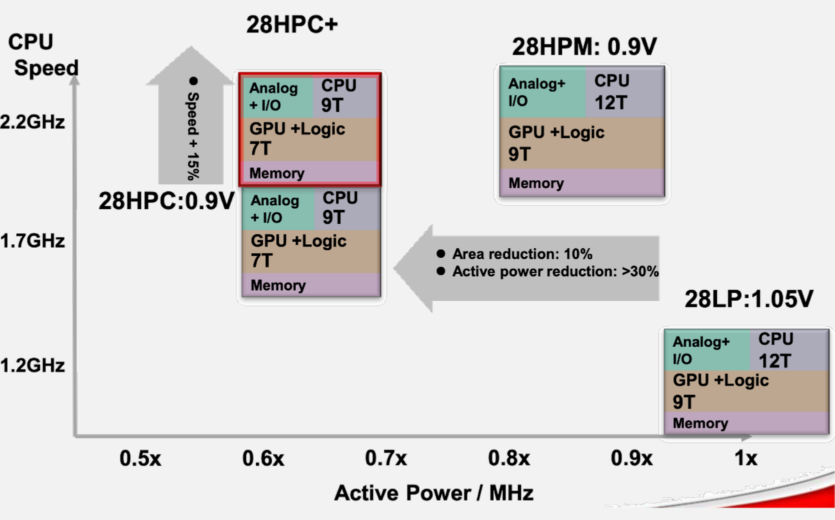
Allowing to:

- Support collaborative work in 28nm
- Mitigate incompatibilities across design teams
- Optimize efforts to integrate a design environment

The 28nm technology PDK flavor

- The design node becomes affordable during the last years and it is expected to become the "mainstream" process for our future developments (similar as 65nm)
- The HPC technology will be gradually replaced by HPC+
  - **HPC+** has become recently the industry standard
  - HPC+ has significant advantages over HPC.
  - As a consequence, in 2021 Europractice provides only one mini@sic in HPC and 3 in HPC+
- The Europractice mini@sic scheme is flexible to allow smaller areas at the lowest possible cost:
  - The number of mini@sic runs increased
  - The minimum area to be used is1mm^2
  - The incremental area is charged per 0.1mm^2
  - The design does not need to be square





The 28nm common design platform

- Multiple metal stack combinations and technology options available for Europractice mini@sic runs

28 HPC	8M	1p8m_5x1z1u_ut-alrdl		
28 HPC+ mmWave PDK	7M	1p7m_4x1y1z_alrdl		
	8M	1p8m_5x2r_alrdl	1p8m_5x2r_ut-alrdl	1p8m_5x1z1u_ut-alrdl
	9M	1p9m_5x1y1z1u_ut-alrd		

mini@sic runs introduced in 2021

- Narrow down choices to enable for a common design platform to facilitate
  - Exchange of IP blocks
  - Work on common projects
  - Sharing prototyping costs

- CERN MSOA Design kits
  - 28 HPC 8M – ~~1p8m_5x1z1u_ut-alrdl~~
  - 28 HPC+ mmWave 9M – **1p9m_5x1y1z1u_ut-alrd**
  - 28 HPC+ mmWave 8M – 1p8m_5x1z1u_ut-alrdl

PDK installed and design platform prepared in 2020 (with Cadence VCAD)
Support dropped since the mini@sic runs are now transitioning from HPC to for HPC+

A new common design platform was prepared in 2021
It is currently the metal scheme adopted by all the CERN projects
Optimal for routing resources

Evaluating future usage
Native support for Inductors

The 28nm common design platform

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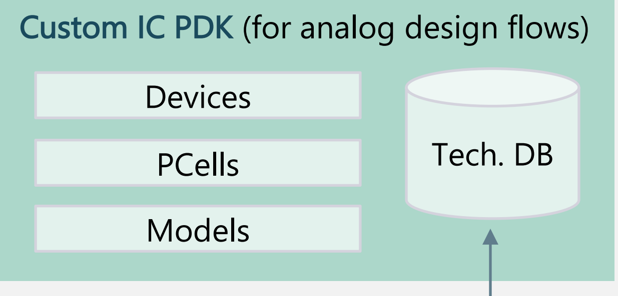
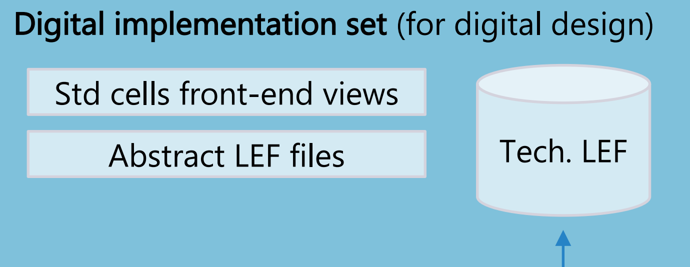
MSOA Design Kit

Allowing to:

- Support collaborative work in 28nm
- Mitigate incompatibilities across design teams
- Optimize efforts to integrate a design environment

The CERN MSOA Design Kits implementation





Back-end views
- Std cells GDS
- Std cells spice models

(usually not accessible)

Other files
- Extraction and DRC deks
- Models, configuration
- Several other design files

Contains:
- Foundry Rules for the metal and cut layers,
- Foundry rules for the masterslice layers (poly, well, and diffusion)

Contains:
- Rules for the metal and cut layers,
- List of valid routing layers and vias.
- Antenna Checking rules
- Current density limits
- Sites definition
- Routing-specific information for routing
  - non-default rules for selected nets.
  - default routing pitch and width

Implementation of a common OA Design Kit (MSOAPDK)

↓

Allow for an OA-based interoperable mixed-signal flows

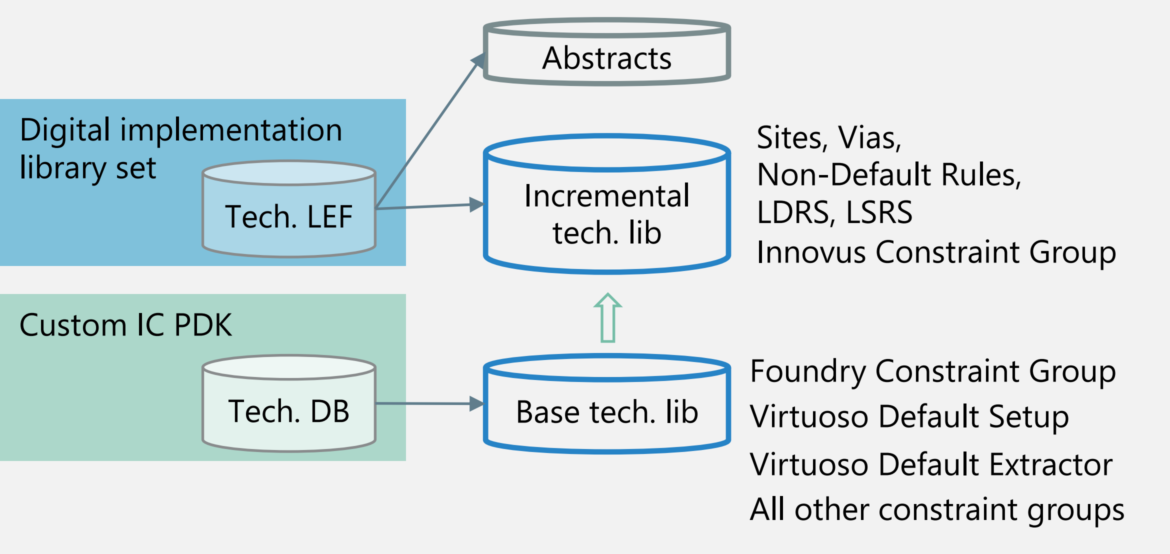
(instead of keeping digital and analog design flows separated)

The 28nm common design platform

The CERN MSOA Design Kits implementation

- Developed by the CERN ASIC Support Team in collaboration with Cadence VCAD Design Services

The ITDB (Incremental Technology Database) MS-OA approach



Suitable for stable process nodes (recently supported by Cadence tools)

- This is the approach used in the F2-28 HPC and HPC+ design kit
- Resolves the inconsistencies between Tech-LEF and Virtuoso tech. lib
- Analog design tools (i.e. Virtuoso) obtain the rules from the tech. lib
- Digital design tools (i.e. Innovus, Voltus, etc.) obtain all the rules from the ITDB Layer which inherits and overrides the tech. lib information
- Presence of a new "foundry group" in the incremental tech file, which will be used exclusively by Innovus for DRC rules
- Facilitate updates without the need of manual handling the tehcnology information like in 130nm and 65nm design platforms

The 28nm common design platform

Foundry digital standard cell libraries

- Foundry libraries
- Front-end and Back-end views are available

  ECSM and CCS models files (with Noise/SI models) — Verilog models — Stage-Based OCV libraries — LEF files — CDK (Cadence DFII view) — GDS — Layout views — Spice models — Extracted Spice models — OA abstract and symbol views — OA schematics — etc

- 120 different library sets:
  - It took more than 2 years of negotiation to get access to the standard cells backend views
  - plus a bit of effort to generate the MSOA ready views and integrate in the common design platforms ready for distribution
- Optimized implementation for Performance and Power
  - Select the best sets and/or exclude cells to optimize Radiation Tolerance, Performance and Power

tcbn28hpcplusbwp30p140	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 9-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 3961 Kgate/mm^2, with 0.9 shrink factor
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tcbn28hpcplusbwp30p140opp	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Standard Vt, 9-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 3961 Kgate/mm^2, with 0.9 shrink factor, need to be used with 9-track core cell library
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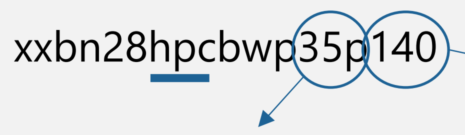
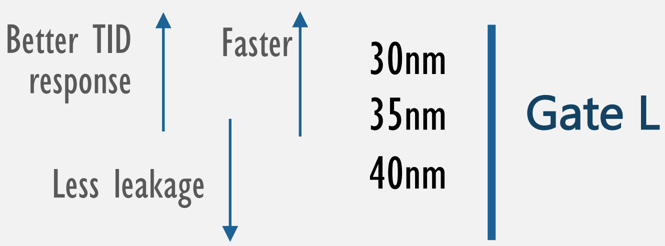
tcbn28hpcplusbwp40p140opp	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Standard Vt, 9-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 3961 Kgate/mm^2, with 0.9 shrink factor, need to be used with 9-track core cell library
tcbn28hpcplusbwp40p140opphvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, High Vt, 9-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 3961 Kgate/mm^2, with 0.9 shrink factor, need to be used with 9-track core cell library
tcbn28hpcplusbwp40p140opplvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Low Vt, 9-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 3961 Kgate/mm^2, with 0.9 shrink factor, need to be used with 9-track core cell library
tcbn28hpcplusbwp40p140oppehvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Extreme High Vt, 9-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 3961 Kgate/mm^2, with 0.9 shrink factor, need to be used with 9-track core cell library
tcbn28hpcplusbwp40p140oppuhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Ultra High Vt, 9-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 3961 Kgate/mm^2, with 0.9 shrink factor, need to be used with 9-track core cell library
tcbn28hpcplusbwp12t30p140	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t30p140hvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t30p140lvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t30p140ulvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra Low Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t30p140cg	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, Coarse Grain cell library, Standard Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor, need to be used with 12-track core cell library
tcbn28hpcplusbwp12t35p140	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t35p140hvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t35p140lvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t35p140uhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t35p140ulvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra Low Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t35p140cg	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, Coarse Grain cell library, Standard Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor, need to be used with 12-track core cell library
tcbn28hpcplusbwp12t40p140	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t40p140hvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t40p140lvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t40p140ehvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Extreme High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t40p140uhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t40p140cg	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, Coarse Grain cell library, Standard Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor, need to be used with 12-track core cell library
tcbn28hpcplusbwp12t40p140cghvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, Coarse Grain cell library, High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor, need to be used with 12-track core cell library
tcbn28hpcplusbwp12t40p140cgehvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Extreme High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp12t40p140cguhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, Coarse Grain cell library, Ultra High Vt, 12-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 2971 Kgate/mm^2, with 0.9 shrink factor, need to be used with 12-track core cell library
tcbn28hpcplusbwp7t30p140	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t30p140hvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t30p140lvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t30p140uhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t30p140ulvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t30p140cg	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t30p140cghvt	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t30p140cglvt	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t30p140mb	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t30p140mblvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t30p140mbuhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t30p140mbulvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t30p140opp	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t30p140opphvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t30p140opplvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t30p140oppuhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t30p140oppulvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Ultra Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 30nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t35p140	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t35p140hvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t35p140lvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t35p140uhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t35p140ulvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t35p140cg	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t35p140cghvt	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t35p140cglvt	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t35p140cguhvt	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t35p140mb	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t35p140mbhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t35p140mblvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t35p140mbuhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t35p140mbulvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t35p140opp	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t35p140opphvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t35p140opplvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t35p140oppuhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t35p140oppulvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, optimized power cell library, Ultra Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 35nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t40p140	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t40p140hvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t40p140lvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t40p140ehvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Extreme High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t40p140uhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t40p140cg	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t40p140cghvt	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t40p140cglvt	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t40p140cgehvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, Coarse Grain cell library, Extreme High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t40p140cguhvt	TSMC 28 NM CMOS LOGIC hpcplus PLUS 0.9/1.8V, Coarse Grain cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t40p140cgcw	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, Common N-Well Coarse Grain cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t40p140cgcwhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, Common N-Well Coarse Grain cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor, need to be used with 7-track core cell library
tcbn28hpcplusbwp7t40p140mb	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t40p140mbhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t40p140mblvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t40p140mbuhvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, core cell library, Ultra High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor,multi-bit flop library,need be used with base library
tcbn28hpcplusbwp7t40p140opp	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, Standard Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t40p140opphvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, High Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor
tcbn28hpcplusbwp7t40p140opplvt	TSMC 28 NM CMOS LOGIC HPC PLUS 0.9/1.8V, power efficient library, Low Vt, 7-track, Routing direction M2H, tapless cell layout structure, gate length 40nm (pre-shrink), poly pitch 140nm, raw gate density = 4289 Kgate/mm^2, with 0.9 shrink factor

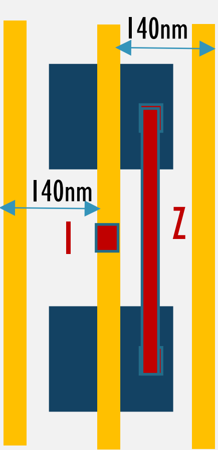
The 28nm common design platform

Foundry digital standard cell libraries

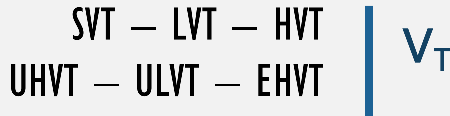




HPC+ 12T	Gate Density KGates / mm²	Speed GHz	Active Power nW/MHz	Static Power nW/MHz
30nm	2,971	x	y	z
35nm	2,971	0.900 x	0.992 y	0.446 z
40nm	2,971	0.806 x	1.003 y	0.232 z



HPC+ 30P	Gate Density KGates / mm²	Speed GHz	Active Power nW / MHz	Static Power nW / MHz
7T	4,289	0.742 x	0.601 y	0.485 z
9T	3,961	0.886 x	0.781 y	0.714 z
12T	2,971	x	y	z



V_T

Limited to max 4 V_T types per design
(in addition to std-V_T, including SRAM V_T)

HPC+ 12T 30P	Gate Density KGates / mm²	Speed GHz	Active Power nW / MHz	Static Power nW / MHz
LVT	2,971	1.351 x	1.235 y	5.305 z
SVT	2,971	x	y	z
HVT	2,971	0.654 x	0.911 y	0.127 z
UHVT	2,971	0.229 x	0.903 y	0.019 z

Access to the Foundry SRAM compilers

- Memory blocks compiled at request
- SRAM types available:
  - Single Port SRAM
  - Dual Port SRAM
  - Ultra High Density - Single Port SRAM
  - Ultra High Density - Dual Port SRAM
- Sleep mode with data retention (power shutdown periphery and control)
- Shutdown without data retention (shutdown entire memory)
- Dual rail supply
- 4 thin metal layers used

Please contact asic.support@cern.ch specifying the type and size of the block required

The SRAMs radiation performances will be characterized in the coming months

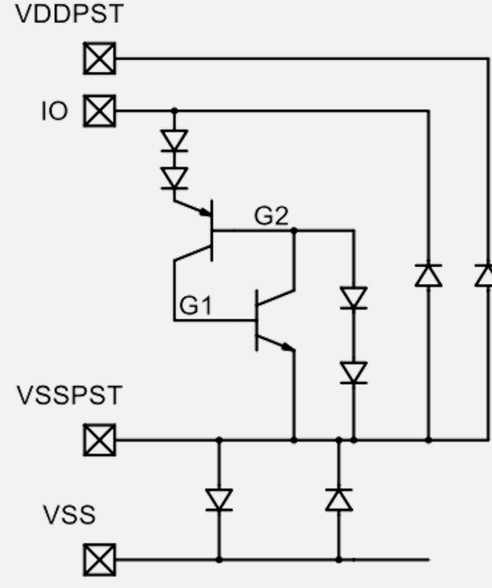
Radiation tolerant pads and ESD protections

Development outsourced to SOFICS

Recently delivered to CERN

- ESD protection design outsourced to Sofics
- Pad ring compatible with the foundry IO pad library.
- Core voltage 0.9V – IO Voltage 1.2V / 1.8V
- List of cells part of the CERN design kit:

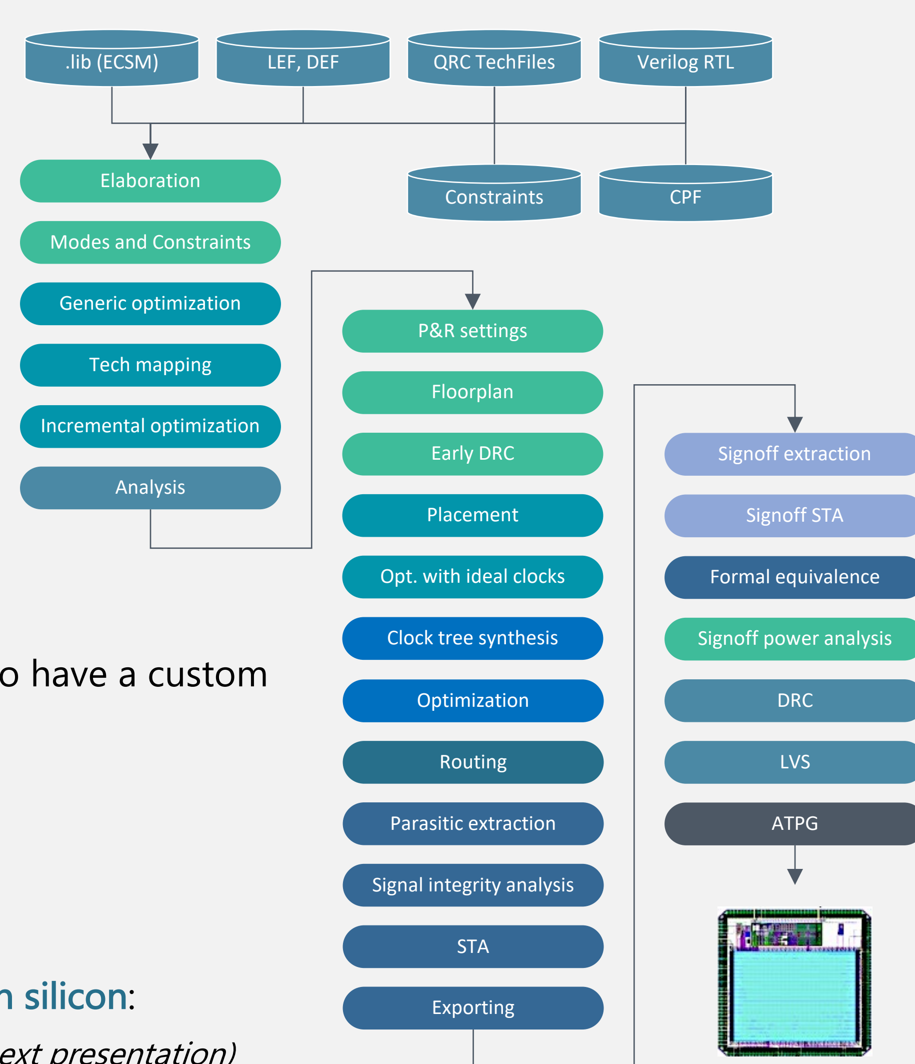
CELL NAME	DESCRIPTION
SF_0V9_POWER_CLAMP_CORE_GROUND	ESD core power rail clamp with PAD connection to core ground rail(VSS)and core side
SF_0V9_POWER_CLAMP_CORE_SUPPLY	ESD core power rail clamp with PAD connection to core supply rail (VDD) and core side
SF_1V2_FULL_LOCAL_CDM	LOCAL CDM ESD protection for 1.2V IO
SF_1V2_FULL_LOCAL	LOCAL ESD protection for 1.2V IO
SF_1V2_OVT	overvoltage Tolerant ESD protection for 1.2V IO
SF_1V2_POWER_CLAMP_IO_GROUND	1.2V ESD IO power rail clamp with PAD connection to IO Ground Rail (VSSPST) and core side
SF_1V2_POWER_CLAMP_IO_SUPPLY	1.2V ESD IO power rail clamp with PAD connection to IO Supply Rail (VDDPST) and core side
SF_1V8_FULL_LOCAL	LOCAL ESD protection for 1.8V IO
SF_1V8_FULL_LOCAL_CDM	LOCAL CDM ESD protection for 1.8V IO
SF_1V8_OVT	overvoltage Tolerant ESD protection for 1.8V IO
SF_1V8_POWER_CLAMP_IO_GROUND	1.8V ESD IO power rail clamp with PAD connection to IO Ground Rail (VSSPST) and core side
SF_1V8_POWER_CLAMP_IO_SUPPLY	1.8V ESD IO power rail clamp with PAD connection to IO Supply Rail (VDDPST) and core side
SF_POWERCUT	Metal only spacer cell to cut all but core ground rail (VSS)
SF_SPACER_W05	Metal only spacer cell to allow interfacing of Rad-Tol cells with Foundry cells



The 28nm common design platform

Digital implementation design flows

- Implementation flow with **Cadence Stylus Common UI**
- **Flowkit based** implementation flow
- Up to date with the latest Europractice release of the Cadence tools
  - For 2021: Innovus 20.1, Genus 19.1, Voltus 20.1, Tempus 20.1, Quantus 20.1, …
- Available at gitlab.cern.ch/asic-design-support/digital-flow-28nm:
- Different approach compared to the previous nodes:
  - The idea is to provide, in addition to a design flow mechanisms for the users to have a custom solutions according their needs
  - Set of advanced procedures for the physical implementation steps
    - **Specific for the design node** and according **foundry and tool vendors recommendations**
    - Specific for **radiation tolerant** design
  - Design-flows and PDKs are **verified by Cadence VCAD**, and will be **validated on silicon**:
    - RISC-V based SoC prototype *(Dec 2021 – M. Andorno, A. Caratelli, R. Pejasinovic - See next presentation)*



The 28nm common design platform

28nm sign-off corners (the flows include scripts to configure the digital design flows and extraction)

	P	V	T	RC corner
Setup	SS	-10%	-40℃	C_worst_T - RC_worst_T
			125℃	C_worst_T - RC_worst_T
Hold	SS	-10%	-40℃	C_worst - RC_worst
			125℃	C_worst - RC_worst
	FF	+10% (5% for 1.0V)	-40℃	C_best - RC_best - C_worst - RC_worst
			125℃	C_best - RC_best - C_worst - RC_worst
			0℃	C_best - RC_best - C_worst - RC_worst

Setup: Variable OCVs per Delay-Corner and per Library

Hold: Variable OCVs per Delay-Corner and per Library
Variable clock uncertainty margins

Minimum 20 Delay Corners for STA sign-off

On-Chip Variations setting for 28nm HPC+ (the flows include a set of .json tables and scripts to setup OCVs and uncertainties)

Process OCV	Flat or Stage-Based*	variable with:	PVT corner	RC corner		
Voltage OCV	Flat only	variable with:	PVT corner	RC corner	Device Vt	IR-drop
Temperature OCV	Flat only	variable with:	PVT corner	RC corner	Device Vt	IR-drop
Wire OCV	Flat or Stage-Based*	variable with:	PVT corner	RC corner		
Spatial OCV	Flat only	variable with:	PVT corner	RC corner	Path length	

Different derates per:
- Capture
- Launch
- Data

Power reduction techniques in 28nm designs

- Architectural changes
- Tune the logic
- Adapt the clock tree
- Use multi Vt cells
- Use multiple transistor lengths
- Use different tracks libraries
- Use Multi-Power domains
- Power shutoff (PSO)

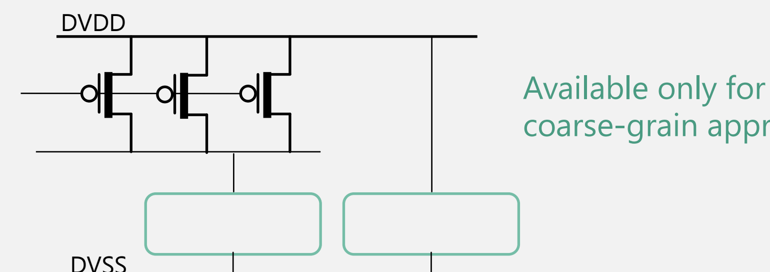
flow support and scripts setup

- Standard-cells selection and multi-library optimization

Gate L	Tracks	V_T
30nm	7	SVT – LVT – HVT
35nm	9	UHVT – ULVT
40nm	12	

flow support and scripts setup

- available libraries for:
  - Power switches
  - Isolation cells
  - Level shifters
  - Retention registers
- Scripts for:
  - Multi power-domains design
  - Block power-down



Available only for coarse-grain approach

28nm technology access & design sharing framework

The design sharing and the distribution of the Common Design Platforms and IP blocks, within the HEP community is subject and must comply to:

Foundry
3-way NDA

- Special NDAs need to be negotiated with the foundry that permit collaborative work

EDA Tool vendor
Design Sharing Agreement

- CADENCE Design Share Agreement related to the EUROPRACTICE software services academic and research laboratory end user agreement

CERN
Design Sharing compliance letter

- Export control compliance
- Design sharing to third parties limitation
- Warranties and condition
- Non-commercial use
- Design work acknowledgment

For more info and to download the forms, lease contact asic.support@cern.ch

The 28nm common design platform

Accessing the 28nm common design platform and design sharing

- The "standard" 3-way NDA does not allow the disclosure of technology information to third parties and thus prohibits collaborative work
- CERN, IMEC and the Foundry negotiated a HEP specific 3-way NDA that permits collaborative among HEP institutes and universities
- The HEP specific 3-way NDA has the same Terms & Conditions as the 3-way NDA covering the 130nm and 65nm technologies from the same Foundry
- On June 30, 2021 the Foundry confirmed the acceptance of all Terms & Conditions
- On Sept. 22, 2021 the Foundry informed CERN that the signatory version of the 3-way NDA will be send out shortly

The 28nm common design platform

Accessing the 28nm common design platform and design sharing

- As soon as CERN - IMEC - TSMC begin the signatory procedure, CERN will invite the HEP institutes and universities to contact IMEC and request to sign the HEP specific 3-way NDA that will give them access to the 28nm common design platform

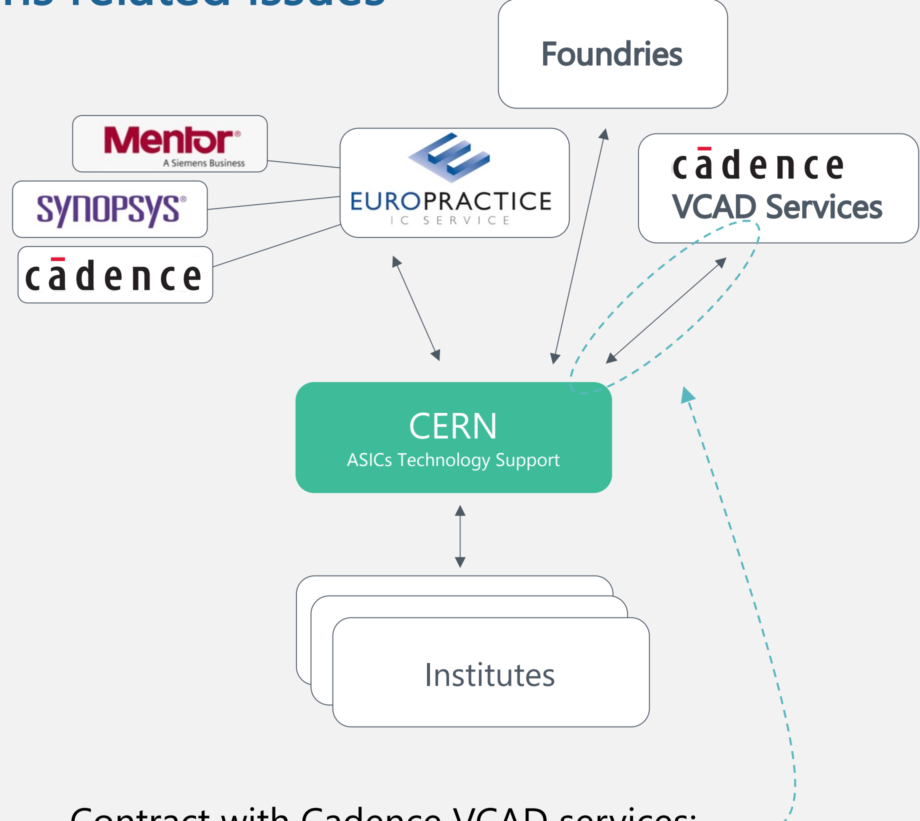
- Similar to the common design platforms for the other technology nodes, the 28nm common design platform will be distributed as follows:

  I. **MSOA PDK** (Mixed Signal Design Kit) via the IMEC QUERIO platform

  II. **IP blocks, Radiation Tolerant Macros, SRAMs, Design Flows**, via CERN ASIC support team

Technical support for the common platform usage and designs related issues

- Designers can contact asic.support@cern.ch
- We receive generic and project specific technical requests:
  - Support for design specific issues related to the EDA tools and Design Flows
  - Support for issues with the Common Design Platform and PDKs
  - Project specific suggestion requests
  - Distribution of shared IP blocks (i.e. generation of SRAM blocks and assistance for design integration)
  - More administrative-like requests (NDA sign, technology information access, design kits download)
  - If the question require more expertise than what we can provide:
    - We involve Cadence VCAD services
    - Request technical information and documentation to the foundries
    - We reach out for suggestions from our CERN EP-ESE collogues
    - We forward the request to CHIPS



Contract with Cadence VCAD services:

- Integration & maintenance of design kits
- Outsourcing technical tasks related to the common design platforms or critical requests
- Training courses

Technical support and resources

Training courses

- System Verilog Advanced Verification Using UVM
  - A Cadence Training Course adapted for CERN-HEP users
- Digital Hierarchical Implementation workshop
  - Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
  - Lab sessions based on:
    - The Cadence tools (Europractice release version)
    - the CERN-HEP Common Design Platforms
      (using the Foundry-2 65nm PDK at the moment)
  - Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD design services
- Digital Implementation in 28nm – Not yet available
  - Availability according Foundry Design Sharing Agreements sign
  - We expect to run this course starting from middle 2022

- 3-day courses involving hands–on examples
  - Morning lectures and afternoon practical exercises
  - Use of CERN microelectronics computing facilities (Servers, licenses)
  - Also this year the courses will be held remotely
- Training team
  - Morning lectures
    - B. Genneret - Cadence (Digital Implementation)
    - O. Dennewald - Cadence (UVM)
  - Lab session preparation and exercises
    - M. Andorno, W. Bialas, A. Caratelli, A. Fioriti

Digital Design Hierarchical Implementation workshop

19-20 November 2019	*1-3 July 2020*	*4-6 November 2020*	*2-4 December 2020*
12 participants	*12 participants*	*10 participants*	*13 participants*
CERN Training Room	*Webinar*	*Webinar*	*Webinar*

3 days course – 12h of theory and 12h or lab sessions

Next session: November 2021

For subscription please contact asic.support@cern.ch

Course program:

Digital Hierarchical Implementation Flow (VLSI)

Skip to Session

Day1: digital block synthesis and floorplanning
- Digital IC intro
- Timing constraints
- Synthesis and optimization
- Scan test synthesis

Lab1: synthesis
- Floorplanning

Lab2: floorplanning

Day2: digital block implementation
- Placement
- Timing/Power analysis
- Optimizations
- Routing
- Signal Integrity

Lab3: place and route

Day3: hierarchical analysis and signoff checks
- Backannotated simulations

Lab4: simulation
- Block models generation
- Top level analysis

Lab5: hierarchical flow
- Signoff STA with Tempus
- Signoff irdrop with Voltus
- Signoff drc/lvs with PVS

Lab6: signoff analysis

Learning Type: Classroom

Domain: Electronic engineering

Format: Lectures & Hand-on examples

Target Audience:
- ASIC designers specializing in electronics for HEP experiments
- CAD engineers

Objectives:
- Floorplan and create partitions for your design
- Implement the blocks and the top-level design
- Learn and use customized scripts (CERN Flow Scripts) that contain the recommended commands and options to implement your design
- Use of TMR techniques for SEU mitigation in digital designs

Contact: technical.training@cern.ch

Course Price (CHF): 0

Number of Hours: 24

Additional Requirements: Verilog HDL, Cadence Innovus Implementation System

Course code: 194DHI01

System Verilog Advanced Verification Environment Using UVM

12-14 November 2020
10 participants
CERN Training Room

2-4 December 2020
13 participants
Webinar

3 days course – 12h of theory and 12h or lab sessions

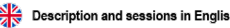
Next session: December 2021

For subscription please contact asic.support@cern.ch

Course program:

SystemVerilog Advanced Verification Environment using UVM

Skip to Session



Description and sessions in English

- Introduction to UVM methodology and Universal Verification Component (UVC) structure
- Overview of the router lab project
- Stimulus modeling
- Simulation phases
- Creating a simple environment
- Test classes
- Configuration, Type Overrides and the Factory
- UVM sequences
- Connecting to a DUT
- Interface and module UVCs
- Multichannel sequences (virtual sequences)
- Building a scoreboard
- Transaction-level modeling (TLM)
- Functional coverage modeling
- Register Modeling in UVM
- Conclusions

- Lab exercises are structured around the verification of a real-life router design. The lab sessions include:
- Creating simple stimuli
- Universal Verification Component (UVC) architecture
- Factories and configuration control
- Sequences
- Integrating multiple UVCs
- Writing multichannel and system-level tests
- Building a scoreboard
- TLM connections
- Functional Coverage
- Simple register modeling

Learning Type: Classroom

Domain: Electronic engineering

Format: Lectures & Hand-on examples

Target Audience:
- ASIC Design Engineers
- Verification Engineers

Objectives:
- Understand the features and capabilities of the UVM class library for SystemVerilog
- Create and configure UVCs for your verification environments
- Combine UVCs to implement a verification environment based on a proven methodology for creating reusable, scalable, and robust verification components

Contact: technical.training@cern.ch

Course Price (CHF): 0

Number of Hours: 24

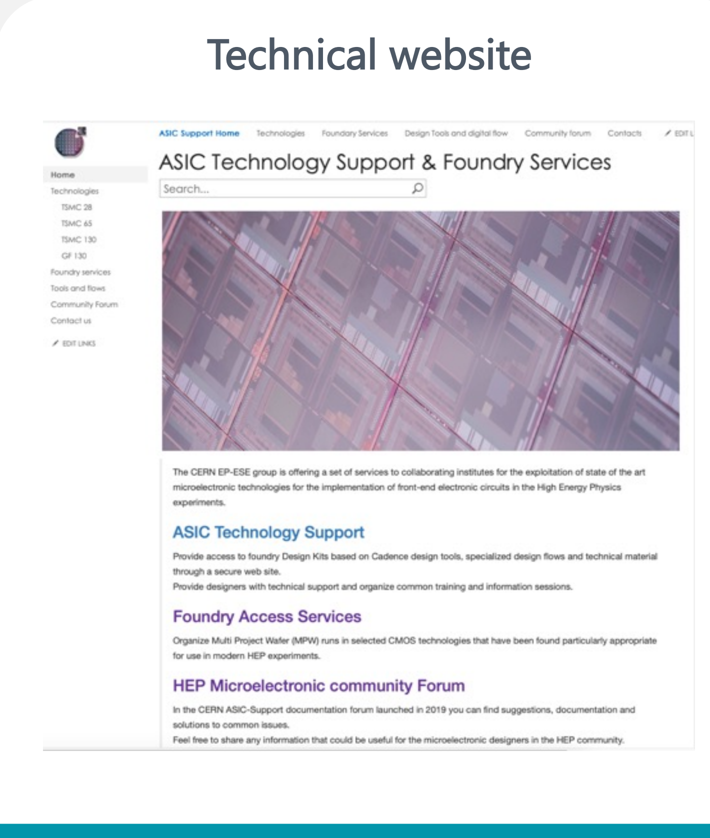
Additional Requirements: Verilog HDL, SystemVerilog, Cadence UVM

Course code: 194SAV01

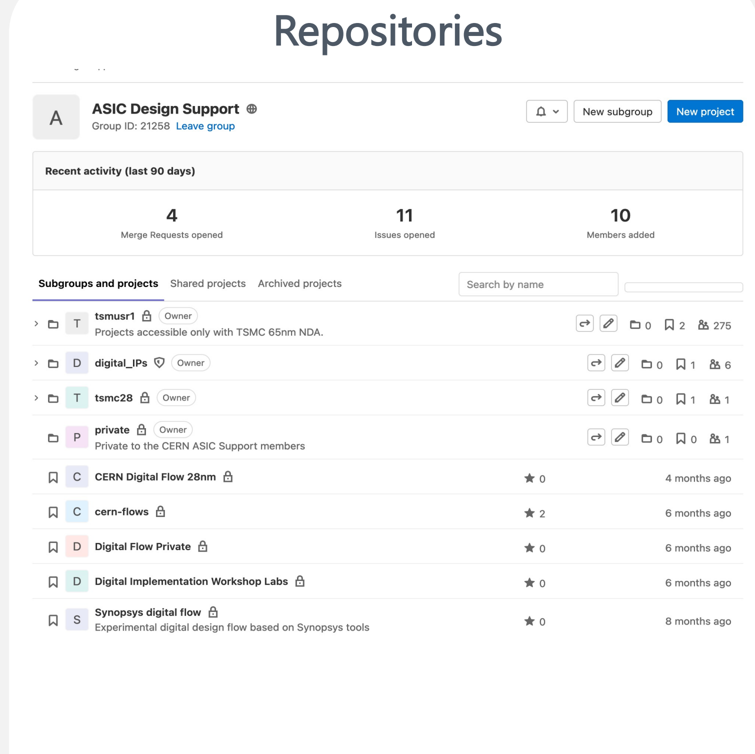
Technical information access and knowledge sharing among the community

We are currently building a new (and better looking) website where it will be possible to access additional technical material and usefull information in a more easy and structured way, in particular for the 28nm node.

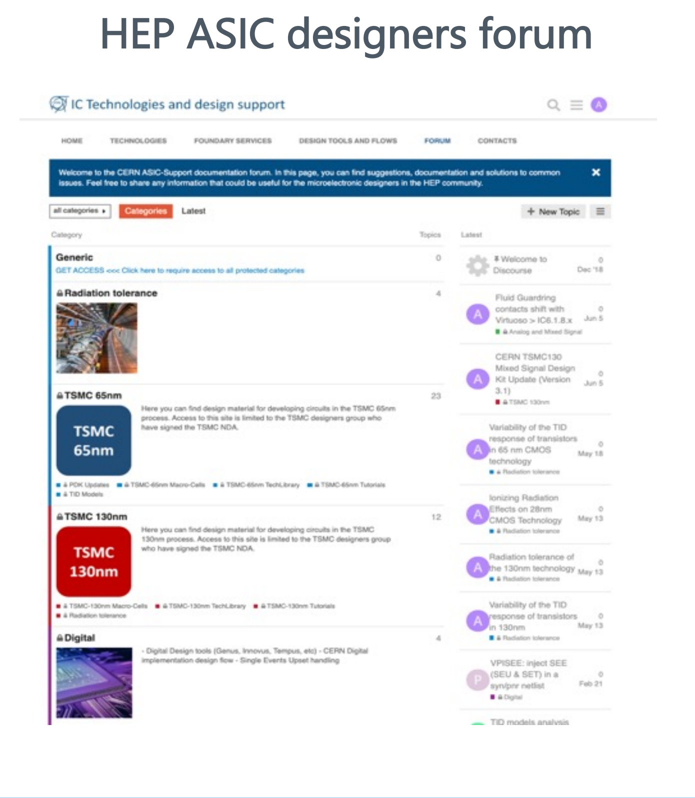
Technical website



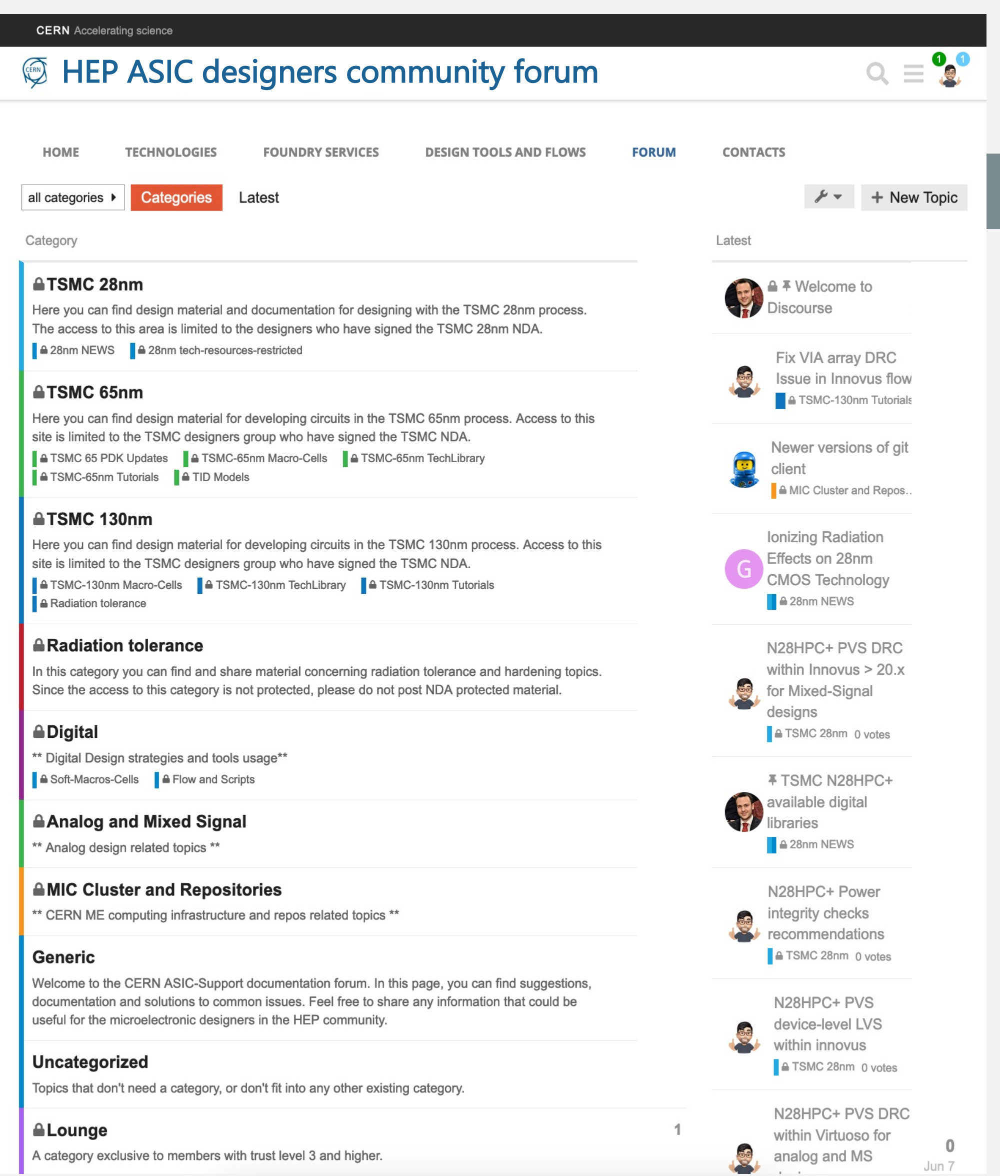
Repositories



HEP ASIC designers forum

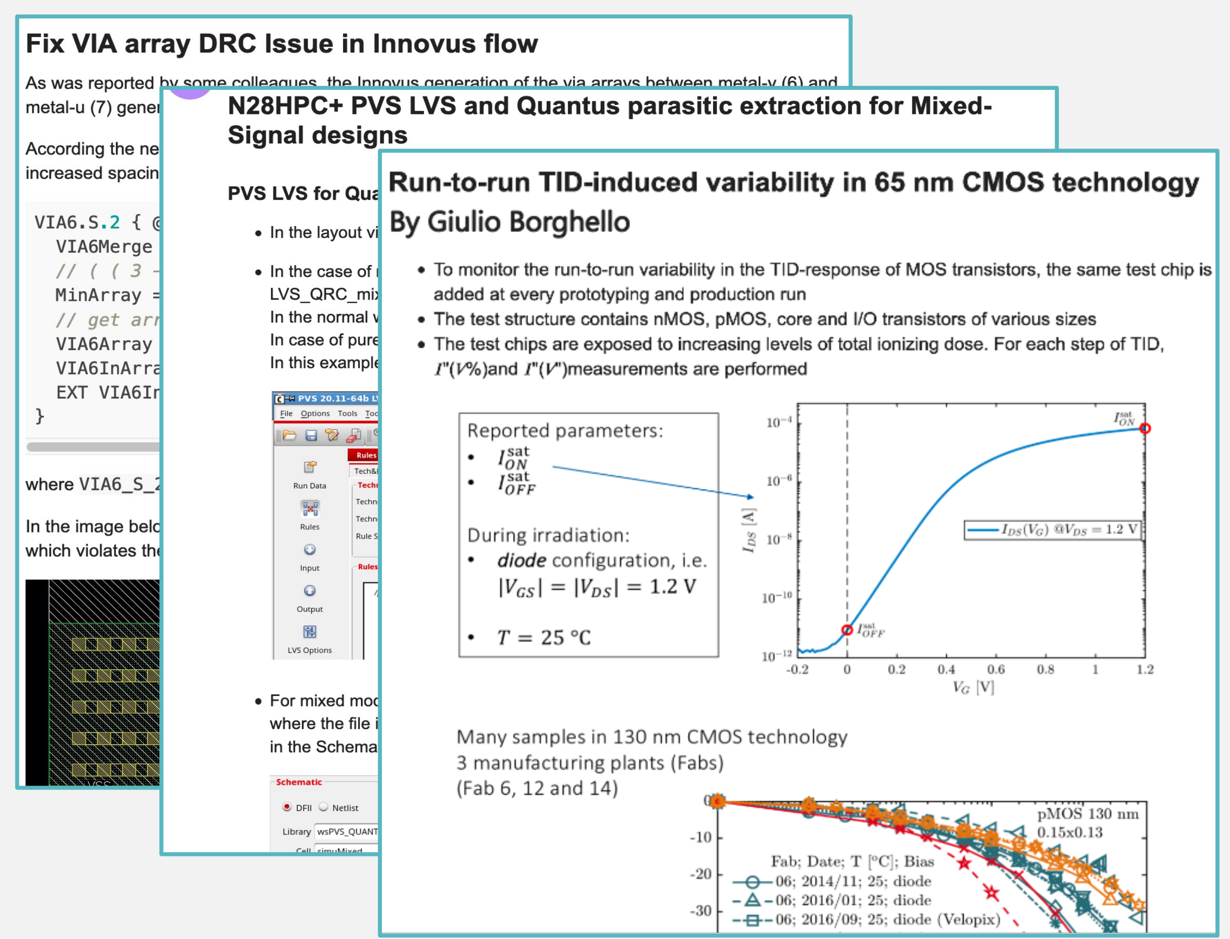


Technical support and resources



The idea of the forum is that everybody can benefits from the findings, solutions and scripts of the others without having to deal with the same issues.

You are invited to partecipate and share any usefull information and material!



Workpackage 5. – IC technologies

CERN-OPEN-2018-006

Strategic R&D Programme on Technologies for Future Experiments

CERN
Experimental Physics Department

December 2018

CERN

WORK PACKAGES

1.1 Hybrid Pixel Detectors
Hybrid pixel sensors with advanced features to be combined with high performance readout ASICs. These developments target small pixels, high-resolution timing and high-rate applications and comprise...
Read more 6

1.2 Monolithic Pixel Detectors
Development of monolithic CMOS sensors for the innermost radii for maximum performance, and for the outer-layers as cost effective pixel trackers with high granularity and low material budget...
Read more 22

1.3 Module Development
Within the EP R&D the module work package (WP 1.3) focusses on the study and development of new module concepts for hybrid and CMOS pixel detectors and their integration for future applications...
Read more 6

1.4 Simulation and Characterization
Detector simulations and modelling of radiation damage, as well as the development of dedicated characterization setups and flexible data-acquisition systems for testing purposes. Mailing List...
Read more 7

2 Gas Detector
Gas based detectors will remain a key technology for radiation detection in particle physics experiments. They provide excellent performances for large area, low mass, radiation hard, relatively cheap...
Read more 4

3 Calorimetry and Lightbased detectors
Calorimetry and light-based detectors have been combined in a work package, as there are several potential synergies. Three topics for calorimetry and one topic each for Ring Imaging Cherenkov (RICH)...
Read more 7

4 Mechanics
Detector mechanics and infrastructure such as detector cooling systems have often a crucial impact on detector design, operation and ultimately also on physics performance. Mechanics usually has to...
Read more 5

5 IC Technologies
ASICs for HEP should follow the microelectronics industry in order to benefit from the intrinsic density of more downscaled transistors and also the intrinsic high speed and lower power consumption...
Read more 7

6 High Speed Links
Radiation-hard high speed data links play an ever growing role in modern experiments. The state-ofthe-art marked by the lp-GBT under development for the LHC Phase-II upgrades, provides data rates of...
Read more 6

7 Software
Software forms a critical part of the HEP programme, recognised in the European Strategy Update of 2020. From the generation and simulation of physics events, to the data acquisition systems and...
Read more 12

8 Experimental Detector Magnets
Detector magnets and magnet systems are key components of future experiments. In order to cope with in some cases tremendously increased requirements, challenges in different domains need to be...
Read more 6

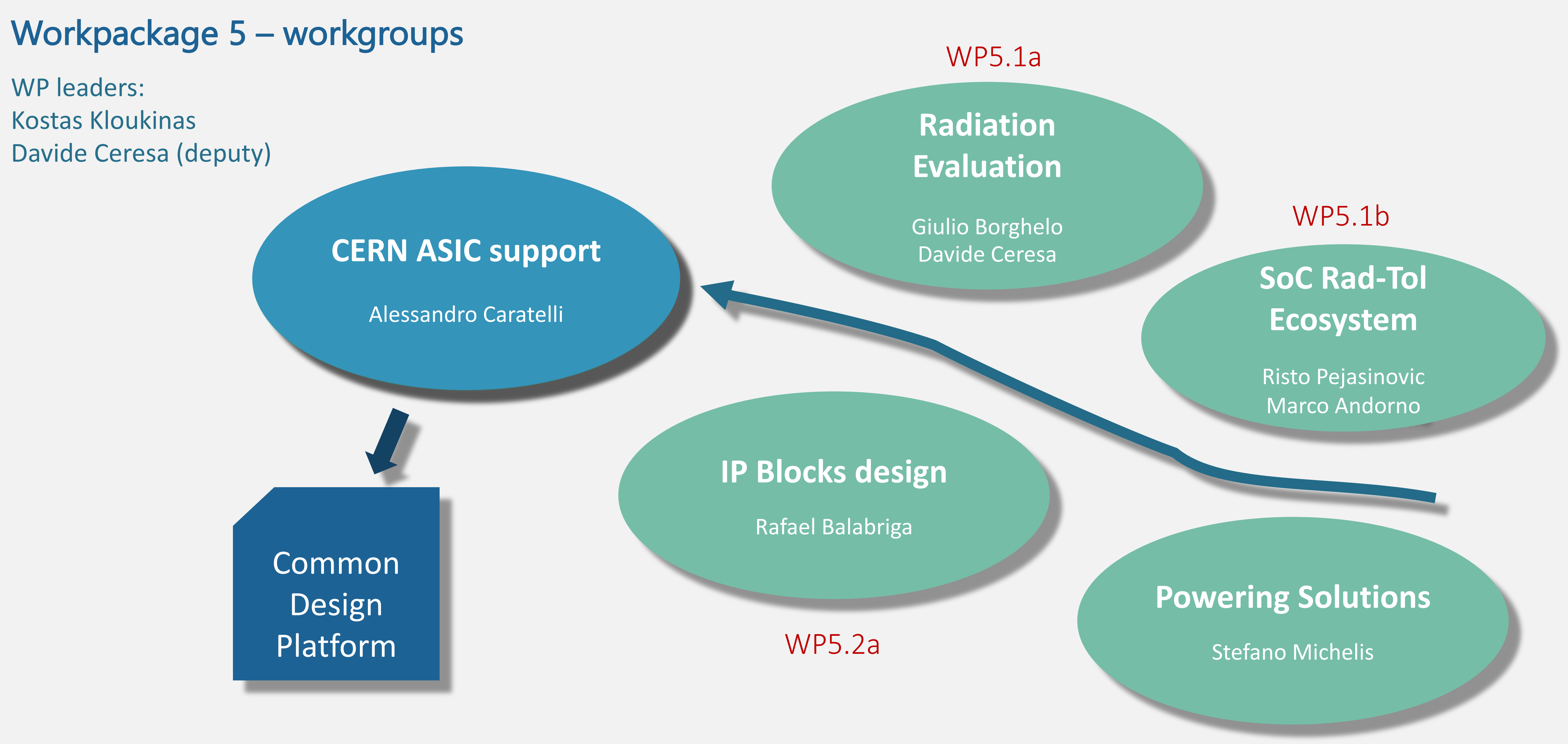
⇨

WP5. Objective:

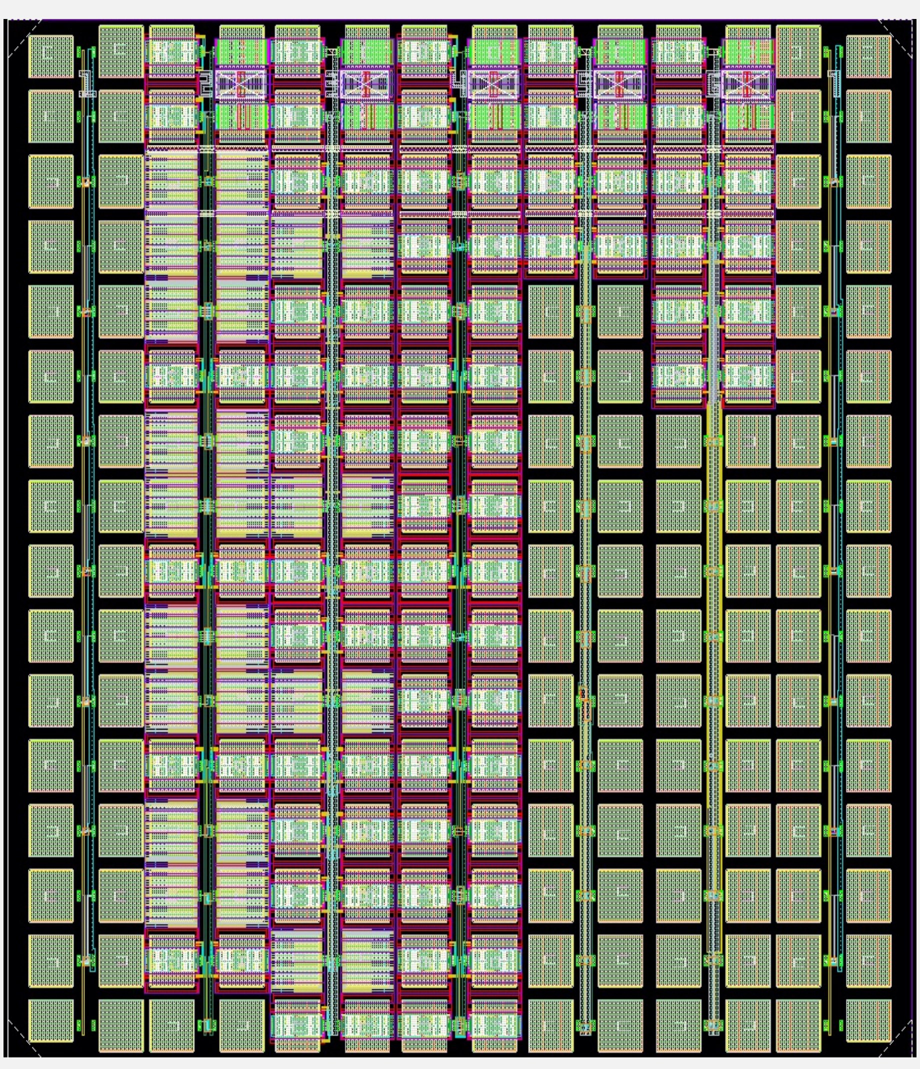
Provide the HEP community with solid infrastructure in state of the art CMOS technologies for the design of complex ASICs

Workpackage 5 – workgroups

WP leaders:
Kostas Kloukinas
Davide Ceresa (deputy)



WP 5.1a – 28nm device-level radiation effects evaluation – [ref. G. Borghello, D. Ceresa]



TID TEST CHIP:

- Study of TID effects on single devices
- Submitted June, 2021
- To complete measurements at 2 different temperatures:
    - Time needed to irradiate 1 structure to 1 Grad: ~1 week
    - 8 structures x 2 temperatures: 3.7 months (if everything works on the first try)
    - However, only few weeks are needed to have the first important results

WP 5.1a – 28nm device-level radiation effects evaluation – [ref. G. Borghello]

1	OTHER 1		
18	VDD	VSS	19
17	p SOURCE	n SOURCE	20
16	gate p	gate n	21
15	p 100x100	n 100x100	22
14	p 1ux100	n 1ux100	23
13	p 1ux1u	n 1ux1u	24
12	p 400x400	n 400x400	25
11	p 1ux1u X9S	n 1ux1u X9S	26
10	p 1ux500 X19S	p 1ux500 X19S	27
9	p 1ux50 X49S	p 1ux50 X49S	28
8	p 3ux30 S	p 3ux30 D	29
7	p 3ux30 G	n 3ux30 G	30
6	n 3ux30 S	n 3ux30 D	31
5	p 2.775ux1u S	p 2.775ux1u D	32
4	p 2.775ux1u G	n 2.775ux1u G	1
3	n 2.775ux1u S	n 2.775ux1u D	2

2	VARIABILITY		
18	VDD	VSS	19
17	pSOURCE	nSOURCE	20
16	gate p 1	gate n 1	21
15	gate p 2	gate n 2	22
14	p 100x30	n 100x30	23
13	p 100x30	n 100x30	24
12	p 100x30	n 100x30	25
11	p 100x30	n 100x30	26
10	p 100x30	n 100x30	27
9	p 100x30	n 100x30	28
8	p 100x40	n 100x40	29
7	p 100x40	n 100x40	30
6	p 100x40	n 100x40	31
5	p 100x40	n 100x40	32
4	p 100x40	n 100x40	1
3	p 100x40	n 100x40	2

3	DIGITAL		
18	VDD	VSS	19
17	pSOURCE	nSOURCE	20
16	gate p	gate n	21
15	p 100x35	n 100x35	22
14	p 100x40	n 100x40	23
13	p 200x30	n 180x30	24
12	p 200x35	n 180x35	25
11	p 200x40	n 180x40	26
10	p 310x30	n 255x30	27
9	p 310x35	n 255x35	28
8	p 310x40	n 255x40	29
7	p 480x30	n 370x30	30
6	p 480x35	n 370x35	31
5	p 480x40	n 370x40	32
4	p 600x30	n 600x30	1
3	p 600x40	n 600x40	2

4	VTH 1		
18	VDD	VSS	19
17	pSOURCE	nSOURCE	20
16	gate p (UL + L)	gate n (UL + L)	21
15	gate p (L + UH)	gate n (L + UH)	22
14	p UL 100x30	n UL 100x30	23
13	p UL 100x40	n UL 100x40	24
12	p UL 200x30	n UL 180x30	25
11	p UL 200x40	n UL 180x40	26
10	*p L 100x30*	*n L 100x30*	27
9	*p L 100x40*	*n L 100x40*	28
8	*p L 200x30*	*n L 180x30*	29
7	*p L 200x40*	*n L 180x40*	30
6	**p UH 100x30**	**n UH 100x30**	31
5	**p UH 100x40**	**n UH 100x40**	32
4	**p UH 200x30**	**n UH 180x30**	1
3	**p UH 200x40**	**n UH 180x40**	2

5	VTH 2		
18	VDD	VSS	19
17	pSOURCE	nSOURCE	20
16	gate p (UL + L)	gate n (UL + L)	21
15	gate p (L + UH)	gate n (L + UH)	22
14	p UL 310x30	n UL 255x30	23
13	p UL 310x40	n UL 255x40	24
12	p UL 480x30	n UL 370x30	25
11	p UL 480x40	n UL 370x40	26
10	*p L 310x30*	*n L 255x30*	27
9	*p L 310x40*	*n L 255x40*	28
8	*p L 480x30*	*n L 370x30*	29
7	*p L 480x40*	*n L 370x40*	30
6	**p UH 310x30**	**n UH 255x30**	31
5	**p UH 310x40**	**n UH 255x40**	32
4	**p UH 480x30**	**n UH 370x30**	1
3	**p UH 480x40**	**n UH 370x40**	2

6	DIFF. BIAS		
18	VDD	VSS	19
17	pSOURCE	nSOURCE	20
16	p gate 1	n gate 1	21
15	p gate 2	n gate 2	22
14	p gate 3	n gate 3	23
13	p gate 4	n gate 4	24
12	p 100x30	n 100x30	25
11	p 3ux30	n 3ux30	26
10	p 100x1u	n 100x1u	27
9	p 100x30	n 100x30	28
8	p 3ux30	n 3ux30	29
7	p 100x1u	n 100x1u	30
6	p 100x30	n 100x30	31
5	p 100x1u	n 100x1u	32
4	p 100x30	n 100x30	1
3	p 100x1u	n 100x1u	2

7	OTHER 2		
18	VDD	VSS	19
17	p SOURCE	n SOURCE	20
16	gate p	gate n	21
15	p 3ux100 12f ULVT	n 3ux100 12f ULVT	22
14	p 40nx35n SRAM	n 65nx35n SRAM	23
13	SOFICS PADS		24
12			25
11			26
10			27
9	IN_STOP	OUT_RO	28
8	IN_SLEEP_H	OUT_RO_H	29
7	IN_SLEEP_F	OUT_RO_F	30
6	VDDPST	VSSPST	31
5	VDD	VSS	32
4	IN	OUT	1
3	OUT_FROM_IN	IN_TO_OUT	2

8	I/O		
18	VDD	VSS	19
17	pSOURCE	nSOURCE	20
16	gate p	gate n	21
15	p I/O 270x150	n I/O 270x150	22
14	p I/O 500x150	n I/O 500x150	23
13	p I/O 1ux150	n I/O 1ux150	24
12	p I/O 2ux150	n I/O 2ux150	25
11	p I/O 4ux150	n I/O 4ux150	26
10	p I/O 4ux300	n I/O 4ux300	27
9	p I/O 4ux500	n I/O 4ux500	28
8	p I/O 4ux650	n I/O 4ux650	29
7	p I/O 270x2u	n I/O 270x2u	30
6	p I/O 500x2u	n I/O 500x2u	31
5	p I/O 2ux1.335u	n I/O 2ux1.335u	32
4	FOXFET GATE	nWell-n+	1
3	nWell-nWell	n+ - n+	2

8 test structures to study:

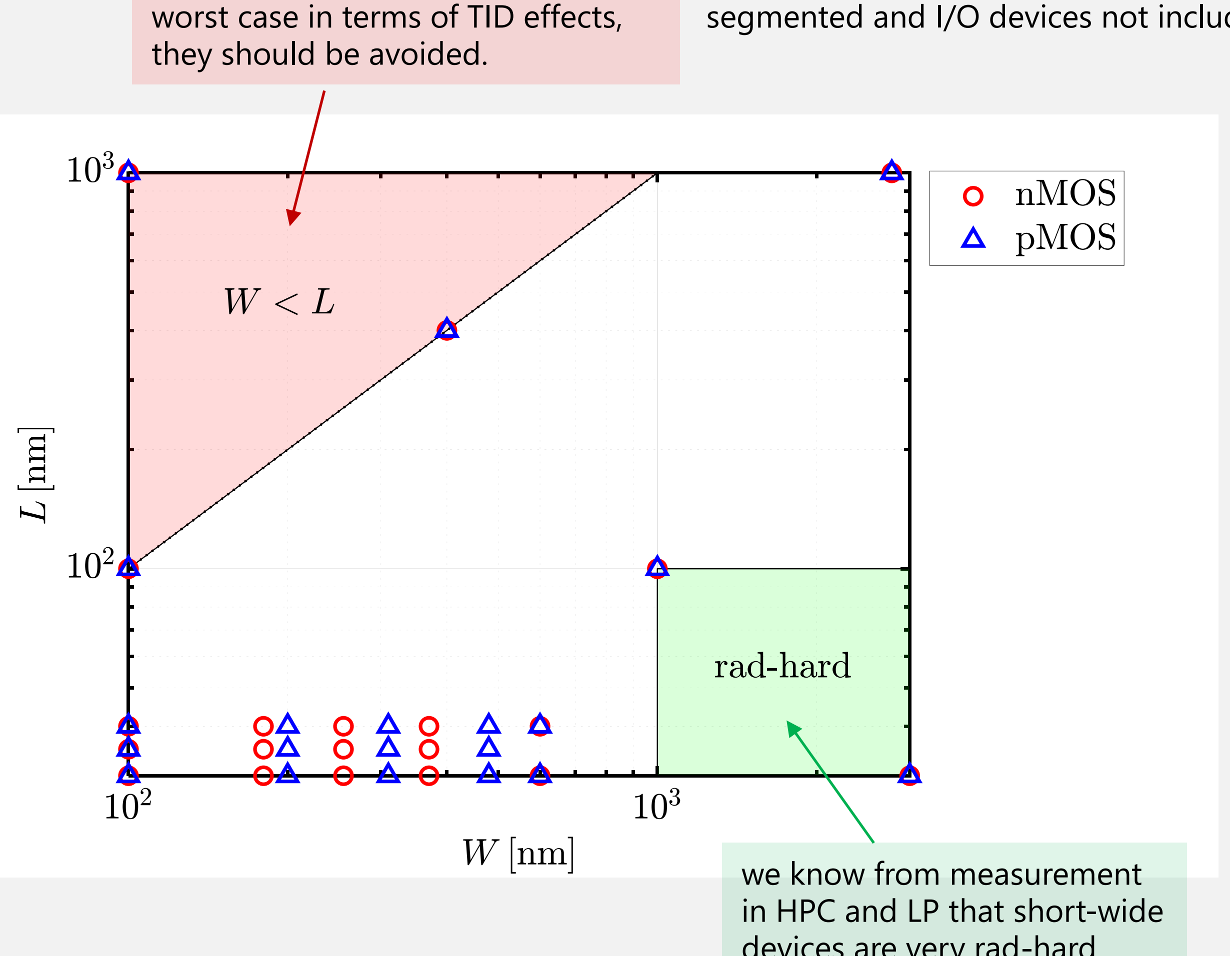
- Several device W
- Several device *L*
- Various V_{TH}
- I/O devices
- variability
- effect of the bias
- segmented devices
- SRAM-size device
- IO PADs
  - Foundry pads
  - CERN RadTol pads
- no-ESD device
- FOXFET
- well-well leakage

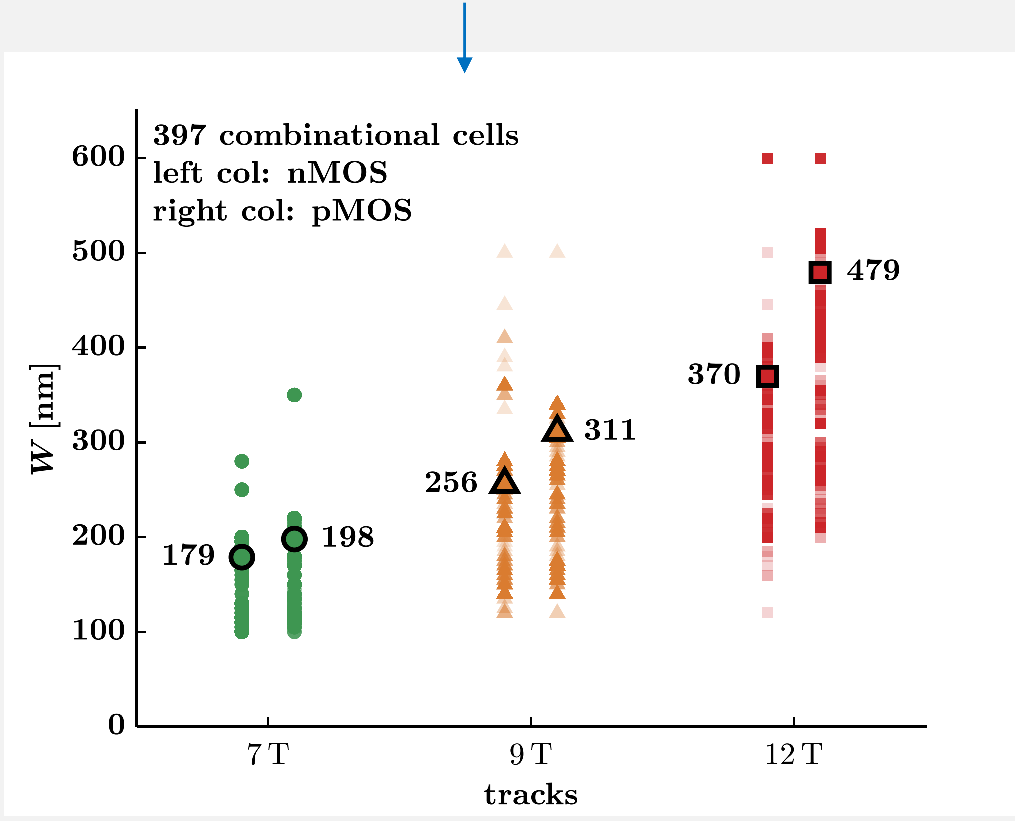
WP 5.1a – 28nm device-level radiation effects evaluation – [ref. G. Borghello]

since narrow & long devices are the worst case in terms of TID effects, they should be avoided.

SIZE MAP (SVTH)
segmented and I/O devices not included

The device W are chosen looking at the average Ws of the standard cells for different tracks





we know from measurement in HPC and LP that short-wide devices are very rad-hard

WP 5.1a – 28nm Digital circuits Radiation Tolerance studies

Study of TID effects on digital circuits

Single event effects studies on digital circuits

Evaluation of foundry memory-compilers

- Test structures designed by D. Ceresa and G. Borghello
- Ring-oscillators for various cells types and standard libraries
- 23 Libraries
  - 7 power domains
  - 16 power gated)

cell name	Min W 7T	delay [ns]
INVD0	100n/110n	9.15
INVD1	200n/220n	7.83
ND2D0	110n/110n	13.12
ND4D0	115n/110n	25.08
NR2D0	100n/110n	13.29
NR4D0	200n/220n	26.26
XOR2D0	100n/110n	40.03
CKBD0	100n/160n	17.65
CKBD1	160n/190n	16.16
CKBD4	160n/190n	15.21
DFCNQD1	100n/100n	
LHCNQD1	100n/110n	

7 T	ULVT	LVT	SVT	~~HVT~~	UHVT	EHVT
30 P	X	X	X	~~X~~	X	
35 P	~~X~~	~~X~~	X	~~X~~	~~X~~	
40 P		X	X	~~X~~	~~X~~	X

9 T	ULVT	LVT	SVT	~~HVT~~	UHVT	EHVT
30 P	X	~~X~~	X	~~X~~	X	
35 P	~~X~~	~~X~~	X	~~X~~	~~X~~	
40 P		X	X	~~X~~	~~X~~	X

12 T	ULVT	LVT	SVT	~~HVT~~	UHVT	EHVT
30 P	X	X	X	~~X~~		
35 P	~~X~~	~~X~~	X	~~X~~	~~X~~	
40 P		X	X	~~X~~	X	X

WP 5.1a – 28nm Digital circuits Radiation Tolerance studies

Study of TID effects on digital circuits

Single event effects studies on digital circuits

Evaluation of foundry memory-compilers

Single event effects studies on digital circuits [tapeout expected December 2021]

- Test structures designed by Sandeep Miryala and Davide Ceresa
- Evaluate latch-up effects
- Cross-Section measurements of standard cells of different V_T flavours
- Evaluate minimum distances for multi-bit upsets and transient lengths
- Evaluation of different triplication techniques

WP 5.1a – 28nm Digital circuits Radiation Tolerance studies

Study of TID effects on digital circuits

Single event effects studies on digital circuits

Evaluation of foundry memory-compilers

Evaluation of Foundry Memory compilers [tapeout expected December 2021]

- Test structures designed by G. Bergamin and D. Ceresa
- Characterization of the Foundry memories for TID and for SEE
  - Multiple flavours (i.e. single port, dual port, UHD)

WP 5.2a – Development of 28nm macro-blocks – [ref. Rafael Ballabriga]

ON CHIP VOLTAGE REFERENCES:

- Bandgap voltage reference, Temperature monitor [INFN Bergamo, Submission December 2021]

CONVERTERS:

- Digital to Analog Converter for biasing [M. Piller, Submission December 2021]
- Analog to Digital Converter for monitoring applications

OPERATIONAL AMPLIFIERS:

- Rail to Rail Operational Amplifier (fast (UGBW> 250MHz e.g. gain boosting)) [J. Kaplon, Submission December 2021]
- Rail to Rail Operational Amplifier (slow (e.g. monitoring in unity gain configuration))

Special IO pads:

- Differential line drivers/receivers [F. Bandi, Submission December 2021]

GENERIC PLL :

- General purpose PLL [F. Bandi, Design start January 2021]

**The blocks will be distributed while respecting the conditions applicable at the moment related to sharing blocks designed with Cadence tools*

WP 5.2a – 28nm macro-blocks design – [ref. Rafael Ballabriga]

ON CHIP REFERENCES:

- Bandgap voltage reference, Temperat

CONVERTERS:

- Digital to Analog Converter for biasin
- Analog to Digital Converter for monit

OPERATIONAL AMPLIFIERS:

- Rail to Rail Operational Amplifier (fast ... nber 2021]
- Rail to Rail Operational Amplifier (slov

DATA TRANSMISSION:

- Differential line drivers/receivers [F. Ba

GENERIC PLL :

- General purpose PLL [F. Bandi, Design

Radiation hard bandgap voltage reference

- **Designers:**
  - Bergamo-Pavia in collaboration with the INFN Falaphel project (Main designer: G. Traversi)
- **Specifications:**
  - Supply voltage .... 0.9 ±10% V
  - Output voltage .... 450 mV
  - Power consumption .... 100 mV
  - DVREF MAX vs TEMP .... -40 to 60 ^{O}C
  - DVREF MAX vs VDD±10% ...... 3 mV
  - Target PSR (low frequencies) .. 40 dB

WP 5.2a – 28nm macro

ON CHIP REFERENCES:

- Bandgap voltage refere

CONVERTERS:

- Digital to Analog Conv
- Analog to Digital Conv

OPERATIONAL AMPLIFIERS:

- Rail to Rail Operationa
- Rail to Rail Operationa

DATA TRANSMISSION:

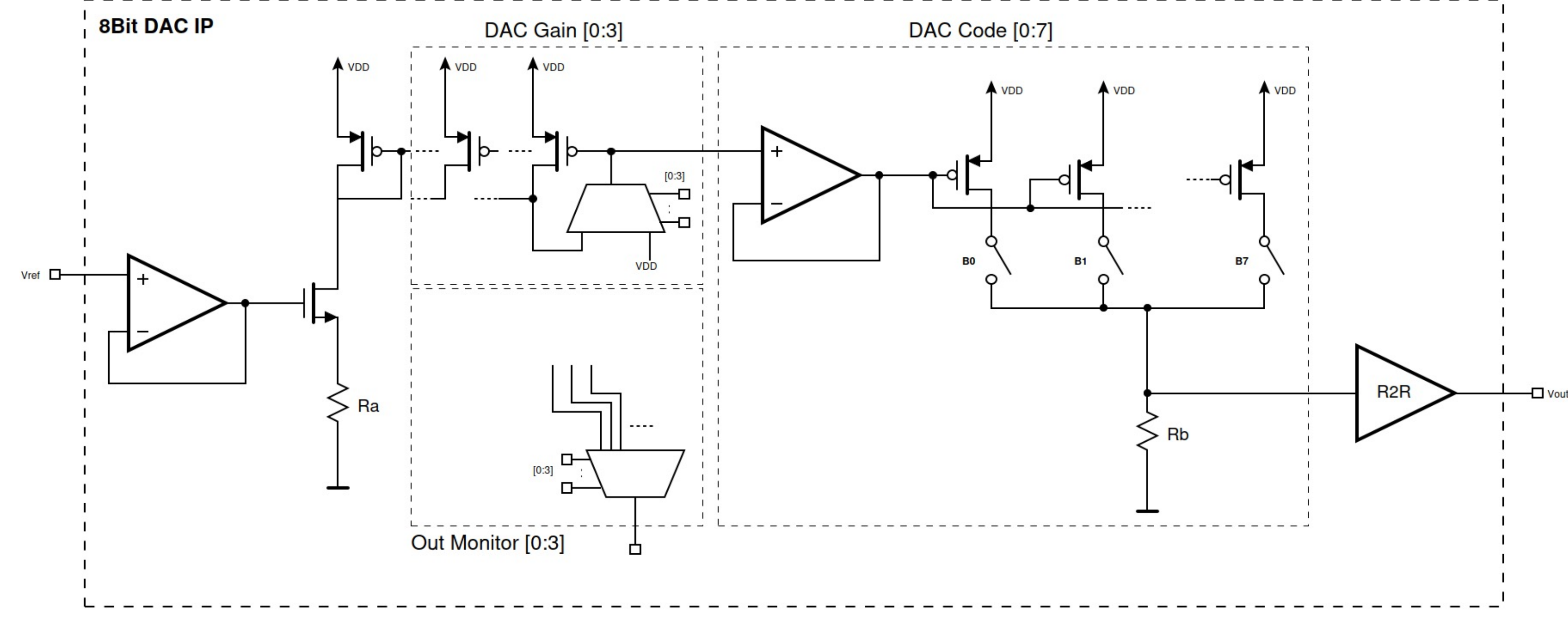
- Differential line drivers

GENERIC PLL :

- General purpose PLL [F

Radiation hard 8-bit DAC

- **Designer**: Markus Piller (CERN / U. Graz)
- **Architecture**: Binary weighted current source architecture
- **Status**: Schematic ongoing.



WP 5.2a – 28nm macro-blocks c

ON CHIP REFERENCES:

- Bandgap voltage reference, Tempe

CONVERTERS:

- Digital to Analog Converter for bia
- Analog to Digital Converter for mo

OPERATIONAL AMPLIFIERS:

- Rail to Rail Operational Amplifier (f
- Rail to Rail Operational Amplifier (s

DATA TRANSMISSION:

- Differential line drivers/receivers [F

GENERIC PLL :

- General purpose PLL [F. Bandi, Des

Radiation hard Operational Amplifier

- **Designer**: J. Kaplon
- **Design:**
  - Architecture: *R. Hogervorst, J. P. Tero, R. G. H. Eschauzier and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," doi: 10.1109/4.340424.*
  - Input stage: Without equalization of the gm
  - Output stage: Class AB
- **Status:**
  - 1st version of schematic completed. Started layout.
  - Evaluating the Phase Margin for unity gain configuration
- **Specifications:**
  - OPEN LOOP GAIN .... 65 dB
  - GBWP (uncompensated)A .... 3.3 GHz
  - SETTLING TIME (1%) for 50mV step .. 13 ns
  - CURRENT CONSUMPTION.................. 250 uA
  - AREA (without compensation) .... 14x14 um^2

WP 5.2a – 28

ON CHIP REFERE

- Bandgap vo

CONVERTERS:

- Digital to A
- Analog to D

OPERATIONAL A

- Rail to Rail
- Rail to Rail

DATA TRANSMIS

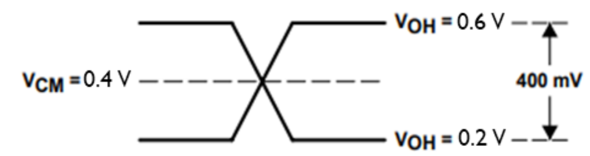
- Differential

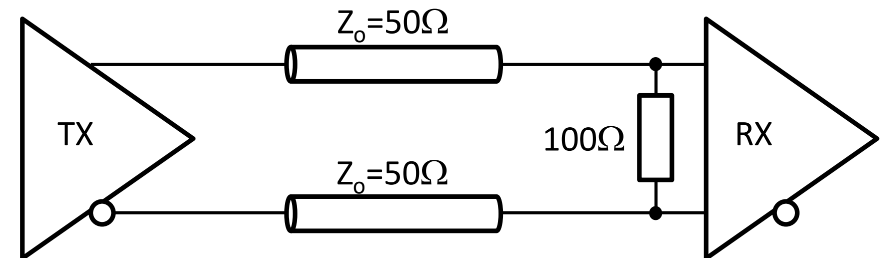
GENERIC PLL :

- General pu

SLVS Driver and Receiver

- Requirements:
  - Radiation hardness up to 1 Grad (thin gate transistors)
  - Interface between the core voltage and the I/O Supply voltage
  - Configurable current to tune differential signal amplitude from 50mV to 400mV
  - Speed up to 1.28 Gbps
  - Self-biased





GENERAL	MIN	TYP	MAX	UNIT
IO VOLTAGE SUPPLY	1.08	1.2	1.32	V
CORE VOLTAGE SUPPLY	0.72	0.9	1.05	V
TEMPERATURE RANGE	-40		125	C

SLVS RECEIVER	MIN	TYP	MAX	UNIT
AMPLITUDE[A]	50		450	mV
COMMON MODE[B]	0.05		1.15	V
TERMINATION IMPEDANCE[C]	90	100	110	Ohm
DATA RATE			1.28	Gbps
TOTAL CURRENT			1	mA
AREA with ESD		100 x 60		um^2
METAL STACK		1-2-(3 POWER)		metals

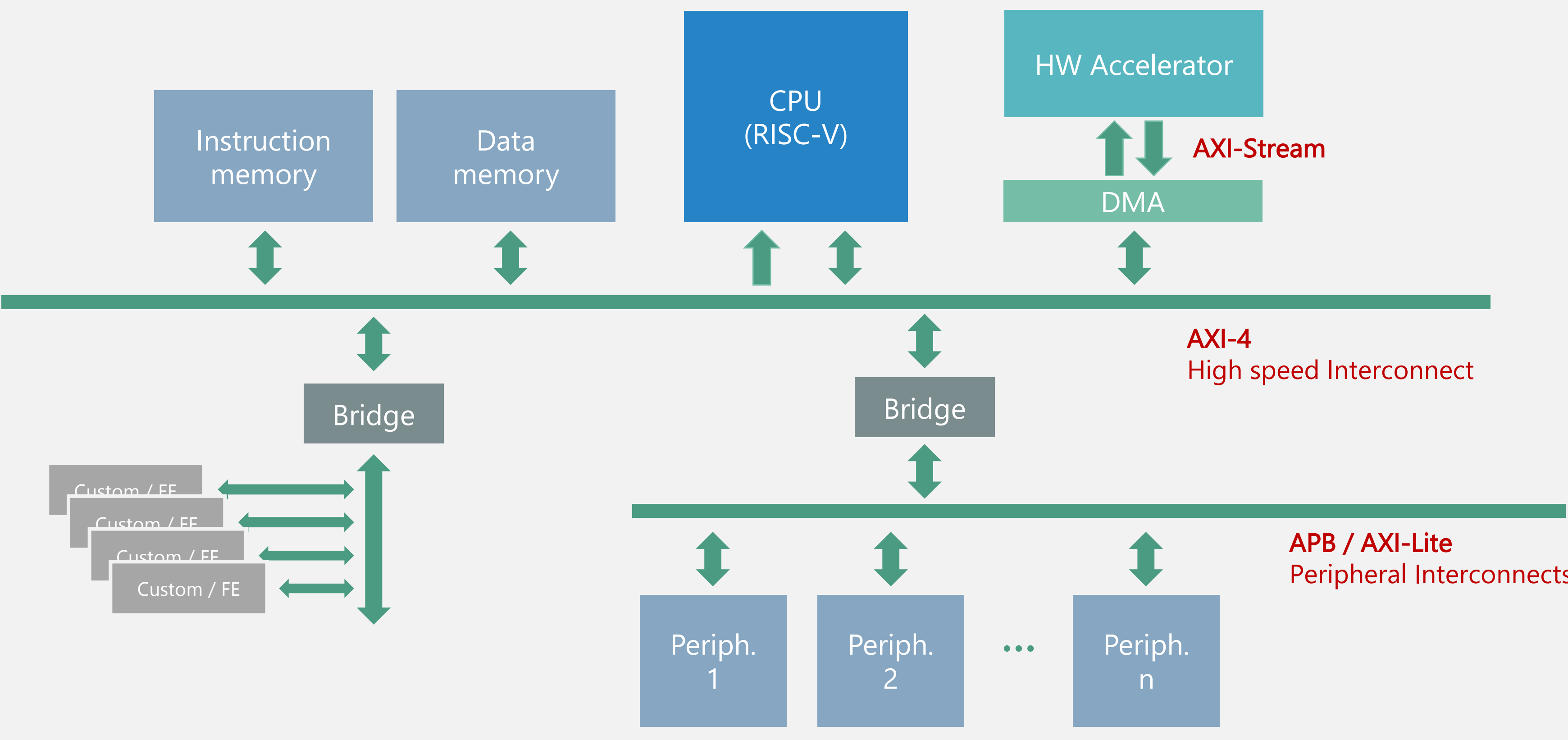
SLVS TRANSMITTER	MIN	TYP	MAX	UNIT
AMPLITUDE	50		400	mV
COMMON MODE		0.4		V
DATA RATE	0		1.28	Gbps
LOAD CURRENT (CONFIGURABLE)	0.5		4	mA
TOTAL CURRENT			6	mA
AREA with ESD		100 x 60		um^2
METAL STACK		1-2-(3 POWER)		metals

WP 5.1b – SoC RadTol Ecosystem

- **People involved:** Risto Pejasinovic, Marco Andorno, Alessandro Caratelli, Kostas Kloukinas
- **Motivation:**
  - Meet the challenges of future FE ASIC designs
  - Introduce a more abstract design methodology
  - Reduce Development time and expedite Verification phase
- **Proposed solution:**
  - Complement the Common Design Platform with a System On Chip (SOC) Radiation Tolerant Ecosystem
  - Develop & Package frequently-used Building Blocks of higher complexity
    - Digital & Mixed-Signal blocks
    - Adhere to a standardized interconnect
    - Validated physical implementation and timing characterization
    - Support Hierarchical digital Implementation and Verification tasks
  - Employ Radiation Tolerant design techniques

WP 5.1b – SoC RadTol Ecosystem

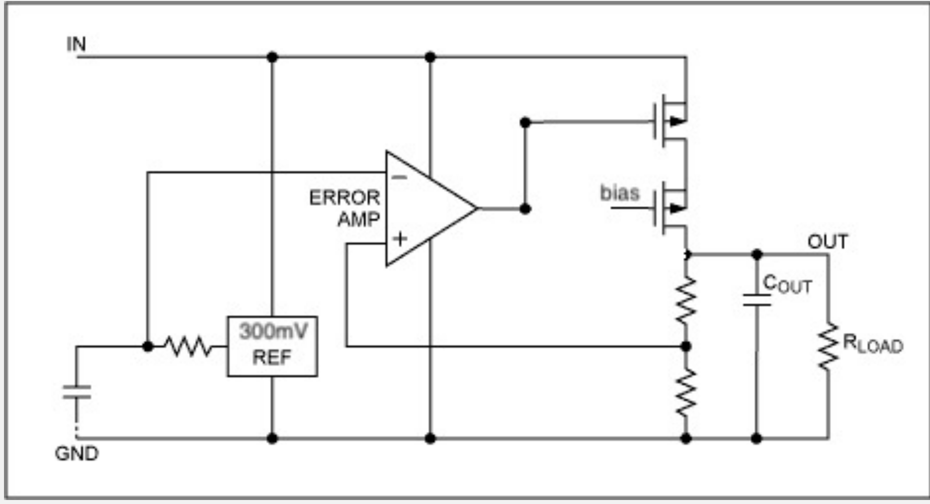
- A dedicated presentation by Risto Pejasinovic follows

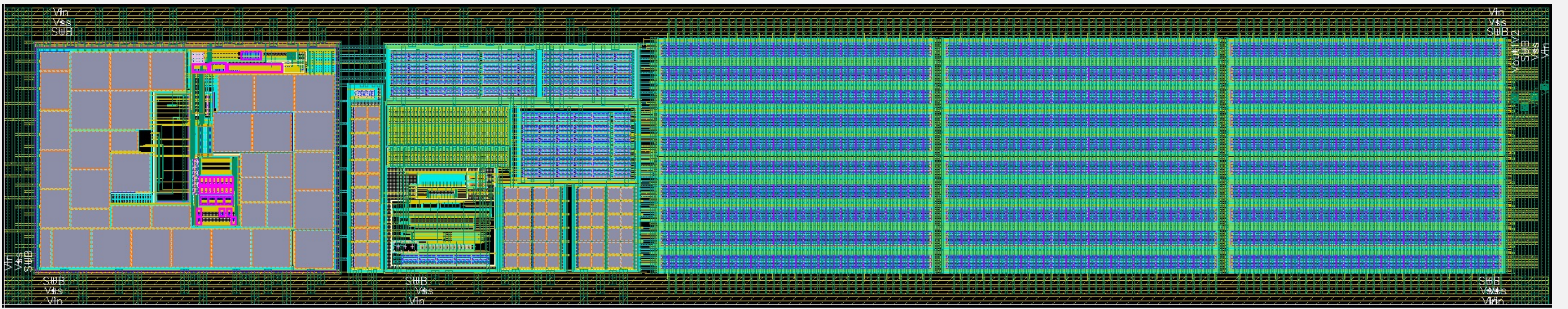


WP 5.2b – Powering solutions [ref. Stefano Michelis]

LDO Macroblock in 65nm

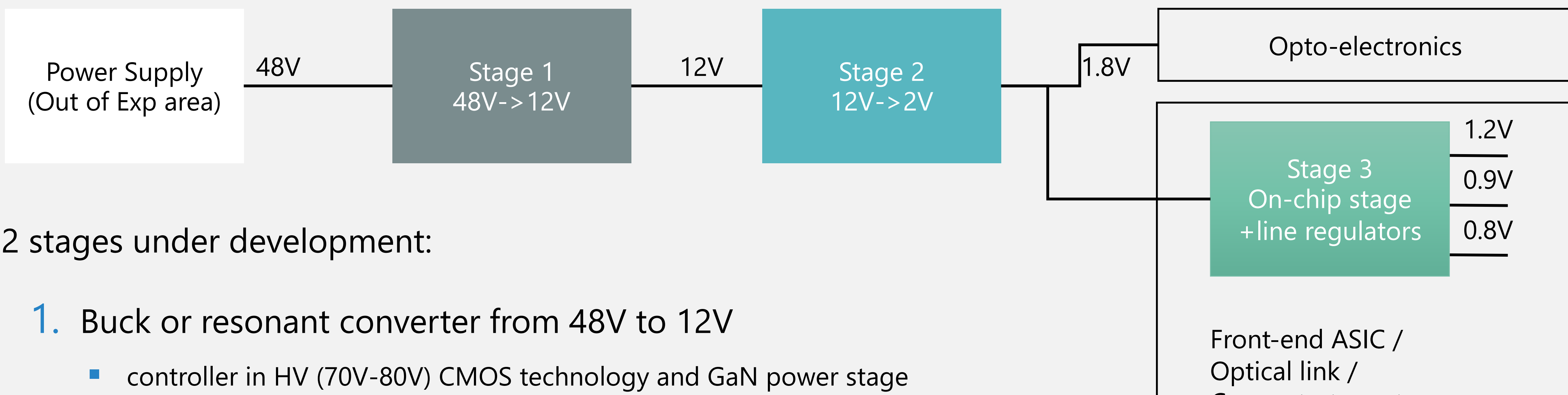
- Dimensions 2100x410 um2 (of which 1200x410um are capacitor)
- Fully integrated (including output capacitor)
- Vin=1.3V to 1.7V
- Vout=1.2V
- Ioutmax=200mA
- Temperature: -30C to 100C
- Internal reference voltage
- GBW from 300kHz to 820kHz (all corners)
- Phase margin > 72 degrees





WP 5.2b – Powering solutions [ref. Stefano Michelis]

Power distribution



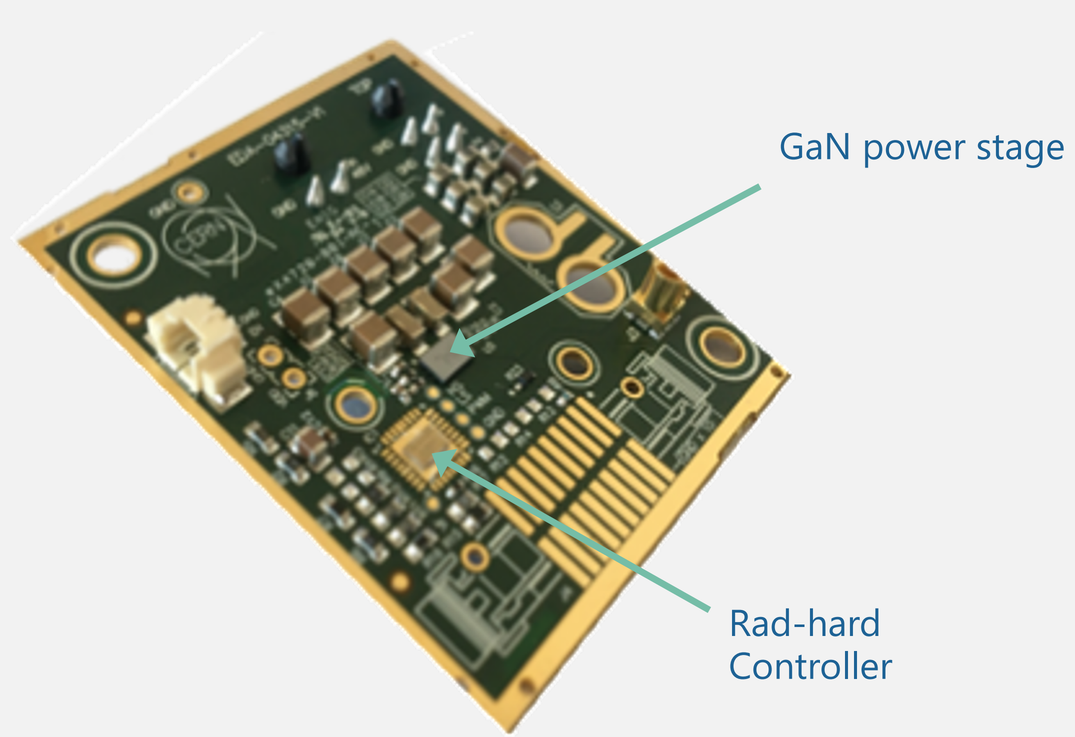
2 stages under development:

1. Buck or resonant converter from 48V to 12V
   - controller in HV (70V-80V) CMOS technology and GaN power stage
2. On-chip regulation in 28 nm technology
   - fully integrated high frequency converter
   - linear regulators and LDO

WP 5.2b – Powering solutions [ref. Stefano Michelis]

bPOL48V

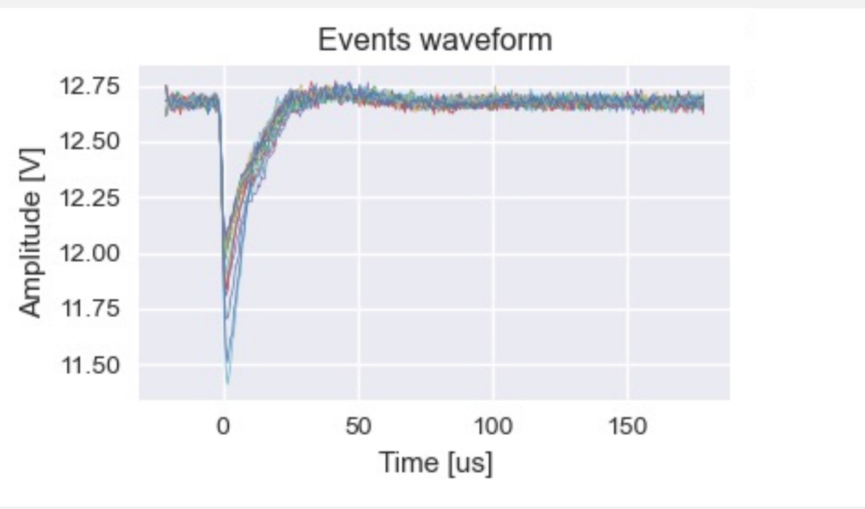
- Very high efficiency, up to 90% at Iout=12A (48V to 12V)
- Radiation tests:
  - TID: up to 50Mrad
  - SEE: up to LET=45 MeV/(mg/cm^2), only transient <5% of Vout
  - DD should be up to 4e14n/cm2 (1MeV equivalent).
- The DCDC design team has developed a converter able to convert 48V to 11-12V, max Iout=12A.
- Power stage is done with GaN COTs
- rad-hard controller is designed by the CERN team.
- Large production is happening this year, 40.000 samples available

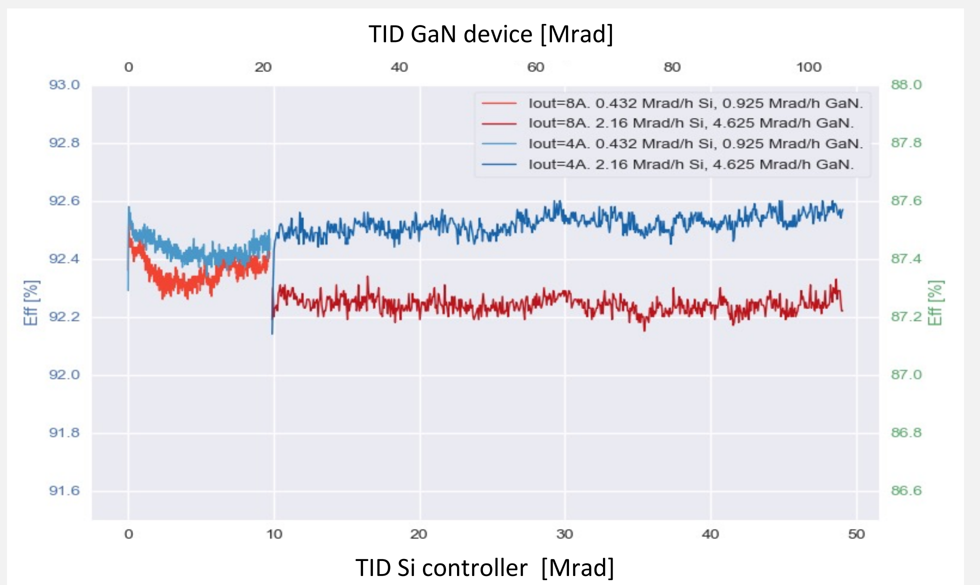


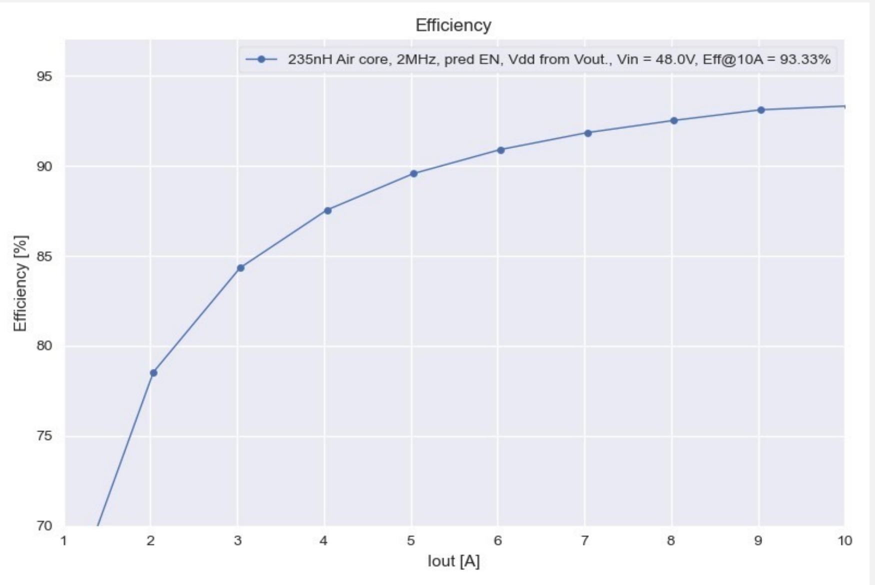
WP 5.2b – Powering solutions [ref. Stefano Michelis]

bPOL48V

- Very high efficiency, up to 90% at Iout=12A (48V to 12V)
- Radiation tests:
  - TID: up to 50Mrad
  - SEE: up to LET=45 MeV/(mg/cm^2), only transient <5% of Vout
  - DD should be up to 4e14n/cm2 (1MeV equivalent).





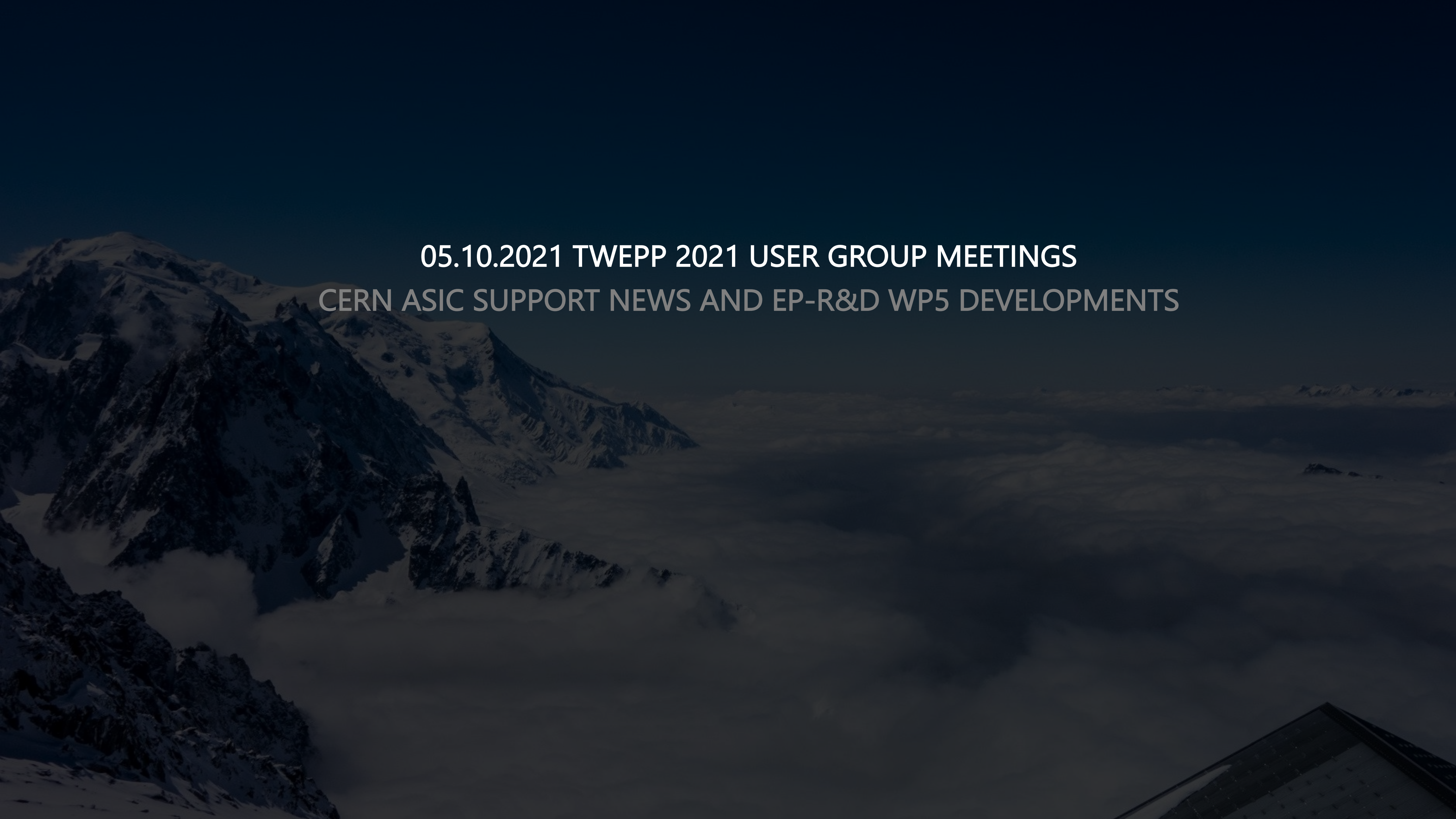


Conclusions

The goal of the CERN ASIC Support and of the Foundry Access Services is to be as useful as possible for CERN users and for all the institutes part of the high energy physics collaborations by:

- simplifying the collaborative works and knowledge sharing
- Provide technology and EDA tool support to designers
- developing and maintaining common ASICs Design Platforms
- providing mechanisms for users to build their custom solutions according their needs
- establishing commercial contracts with silicon vendors and NDAs that allow for collaborative work *[K. Kloukinas]*
- organizing & coordinating silicon fabrication *[K. Kloukinas]*

Any contribution that can help improving the support and sharing of knowledge is very welcome!


05.10.2021 TWEPP 2021 USER GROUP MEETINGS
CERN ASIC SUPPORT NEWS AND EP-R&D WP5 DEVELOPMENTS

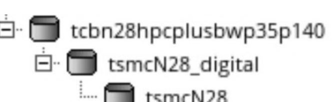
BACKUP SLIDES

28nm CERN MSOA PDK build 1/3

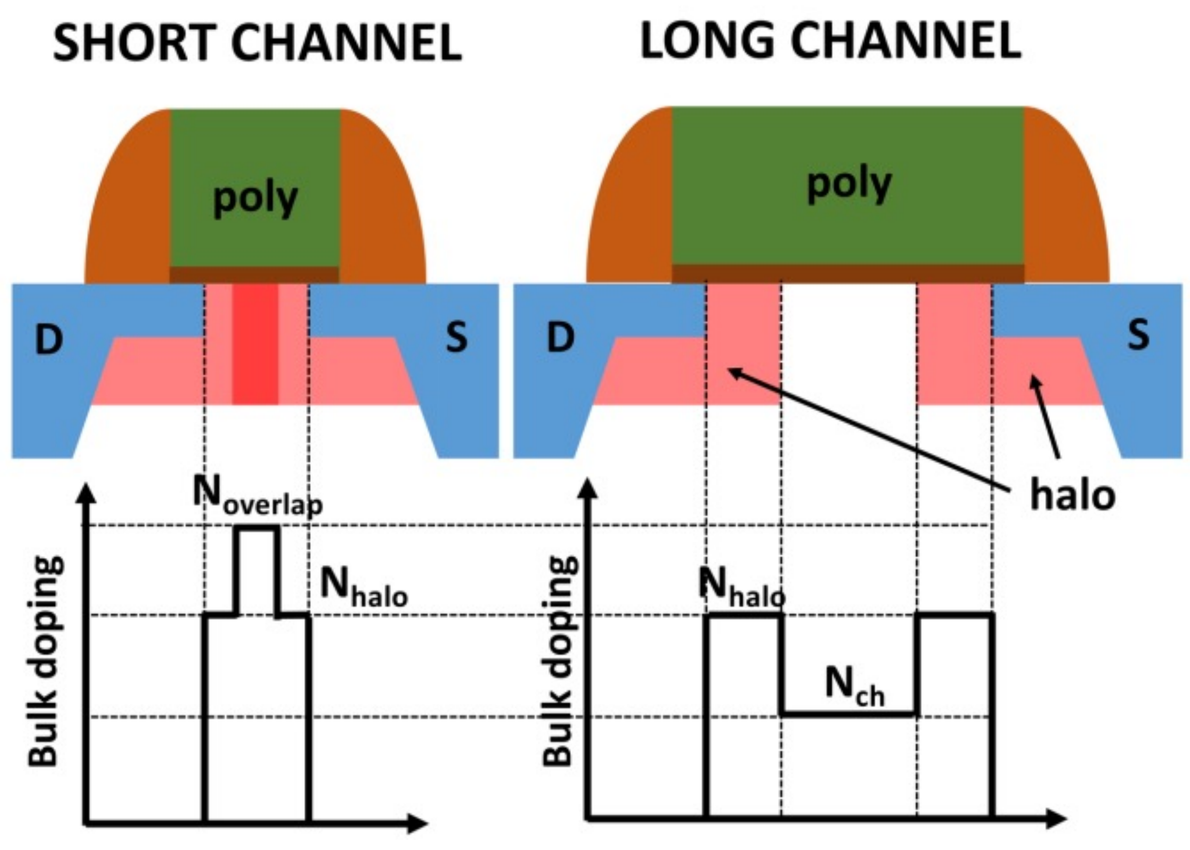
- Install foundry PDK
- Techfile updates:
  - Merge F2N28 layer and via definition to latest techfile v2.0 (no rules included)
  - Add the new layers into the gds2 layer mapping file ..layermap
  - Merge the display.drf
- Define tsmN28_digital (ITDB MSOA PDK)
  - Via Innovus it is possible to export the tech LEF and the MACROs LEF from the SVt digital library
    - Adapt LAYER / CUTCLASS / NDR names in the LEF to be consistent with those in the Base PDK
    - Fix some logical layer numbering which are inconsistent
    - Adapt layers and via naming
  - Process and create the new F2N28_digital reference library
    - This has created the technology library (F2N28_digital) that contains all the rules necessary for Innovus PnR (rules and Vias are the same as described in the original LEF file)
    - This is an ITDB structure referencing the base technology library (F2N28) which doesn't require any change
    - All vias and rules mandatory for the PNR are stored into this ITDB structure
- Add additional files:
  - DRC decks, LVS and Extraction decks (Calibre and PVS)
  - Add filling rules and scripts
  - Install guard-rings, inductors etc..
  - Install MOM caps
  - Add other technology related files useful for design (like IRCX files, IMX, etc.)
  - Generate ICT and QRC tech files for Electromigration analysis
  - Create the top-level model files .scs files to facilitate analog simulation setup
  - Fetch and add useful documentation, etc..

28nm CERN MSOA PDK build 2/3

- Add standard cells front-end views
  - Add ~~NLDM~~, ECSM, CCS lib files (with Noise/SI models)
  - Add Stage-Based OCV libraries
  - Add Verilog models
- Add standard cells back-end views
  - Add the CDK (Cadence DFII view) archive containing the standard cells definitions and layouts if available
    - Otherwise create the cells layouts out of the GDS
  - Reference all the digital libraries to the ITDB-layer technology library (a scriptable workaround is loading and merging a dummy tf)
  - Add the standard cells GDS (for gds-merging in stream-out)
  - Add Spice models (SPI)
  - Include spice netlist capability for Analog and Mixed Signal simulation of standard cells:
    - For the all logical gates include the LPE SPICE models
    - Create per each library a SCS files which includes the spice models for each corner section

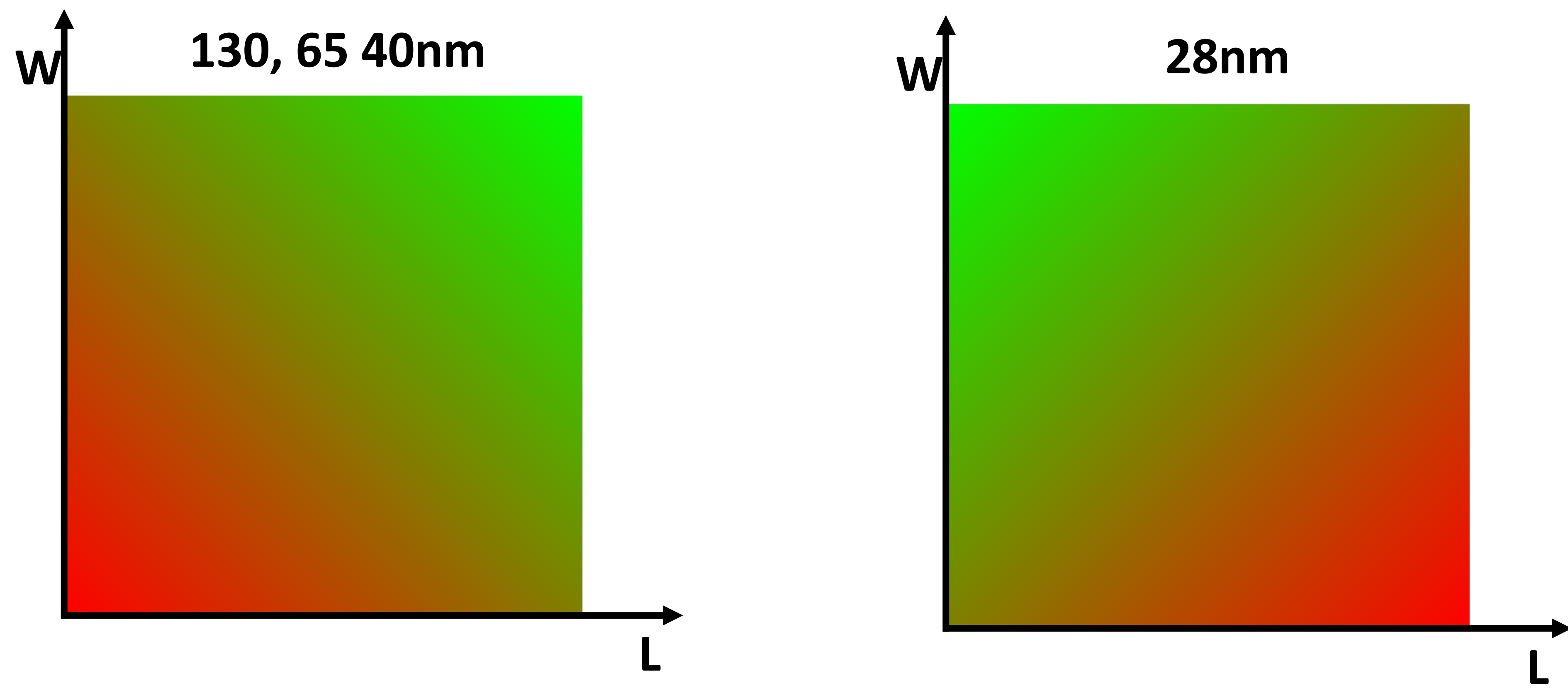


- Add standard cells OA front-end views
  - Extract the LEF file from the SEF removing technology information and site definition
  - Add LEF files (Macros only)
    - Correct eventual discrepancies (i.e. the UHVT libraries have inconsistent site definitions sizes for the CORE sites) -> poly pitch inconsistencies
  - Generate OA abstract views from the LEF files using as tech ref the F2N28_digital library
  - Create the symbol views
  - Add the OA Verilog stopping-views
  - Replace the base gds2-layer-mapping with the main layer map according to the metal stack
  - Add Verilog netlist for each cell in the OA structure



S. Bonaldo *et al.*, "Influence of Halo Implantations on the Total Ionizing Dose Response of 28-nm pMOSFETs Irradiated to Ultrahigh Doses," in *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 82-90, Jan. 2019, doi: 10.1109/TNS.2018.2876943.

TID sensitivity VS transistor size



minimum size devices are not the worst case for 28nm technology!

- very good news for digital applications!