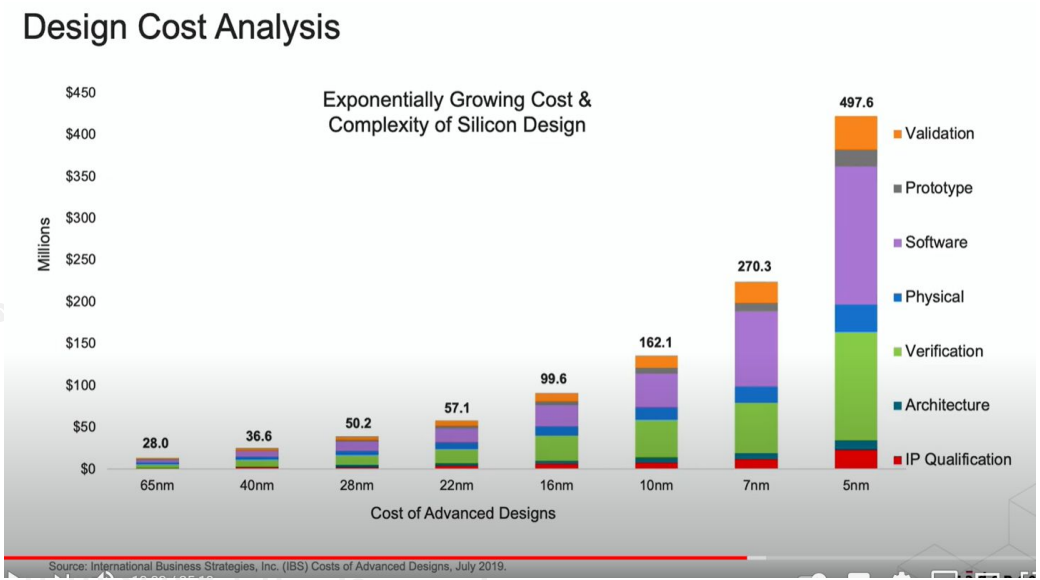
# ChipFlow - Commercial Open Source EDA

Rob Taylor, CEO

# EDA is inefficient




- Proprietary & High Cost
- Innovation costly and constrained
- Waterfall Methodology
- Niche programming languages
- Esoteric skillbase

# Why is it inefficient?

## Software Security & Quality

2021 Code Dx
2020 Tinfoil Security
**2017 Black Duck Software**
2017 Forcheck*
2016 Codiscope
**2016 Cigital**
2015 Goanna Software
2015 Protecode
2015 Seeker* (from Quo
**2015 Codenomicon**
2014 Kalistick
**2014 Coverity**

## Verification & Prototyping

2020 Terrain Technologies
2019 DINI Group
2019 QTronic GmbH
2016 WinterLogic
**2015 Atrenta**
**2012 SpringSoft**
**2012 EVE**
2012 ExpertIO
2011 nSys
2010 ZeroSoft

2010 VaST Systems
2010 Nusym
2010 CoWare
**2008 Synplicity**
[illegible]Pit* (from ProDesign)
2000 VirSim* (from [illegible])
1999 Covermeter* (from Advanced Technology
1999 Apteq
1998 Systems Science
1998 Radiant
**1997 Viewlogic**
1995 Arkos
**1994 Logic Modeling**
1994 CADIS
1994 Arcad
1993 Fault Simulation* (from ExperTest)
1990 Zycad

## Silicon IP

2020 INVECAS IP*
2019 eSilicon IP*
2018 Silicon and Beyond
2018 Kilopass Technology
**2010 Virage Logic**
2009 MIPS Analog
2007 MOSAID SIP
2005 TriCN
2004 LEDA Design
2004 Cascade
2004 Accelerant
2004 Progressant
**2002 inSilicon**
1995 Silicon Architects
1993 Compiled Designs

## Silicon Engineering

2020 Light Tec
2018 PhoeniX Software
2016 Gold Standard Simulations
2016 Simpleware
2014 Brandenburg Gmbh
[illegible] RSoft Design Group
[illegible]nologies)

## Chip Design

2020 Moortec
2020 Dorado DA
2020 Qualtera
2012 Ciranova
**2012 Magma**
2011 Extreme DA
2010 Synfora
2009 TeraRoute
2009 Gemini
2007 Sandwork

2005 Nassda
2004 Monterey
2004 iRoC SA
2004 ADA
2003 InnoLogic Systems
**2002 Avanti**
2000 The Silicon Group 1999 Gambit
1999 Stanza
[illegible]st Technologies

Highly acquisitive dominant players force everything into the **same market model**
- Think MS circa 2000..

# What is the effect of this?

**Lack of technology innovation** - Innovation constrained to those with the code!

**Lack of market innovation** - wedged into traditional high-touch direct sales and high cost-per-seat model.

**Low reuse** - Plenty of reinventing the wheel, due to highly proprietary/protective behaviour across the space

**Low transferable skills** - Every workplace has different tooling, flows and standards

**Higher risks** - Waterfall development, with specialised roles places high risk on system architects

**(Very!) Long development cycles** - Development cycles as long as a software startup takes to get to series C!

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THE 90's CALLED. THEY WANT **EVERYTHING** BACK!!!1

# Barriers to solving the problem

Industry conservatism

Tightly bound small ecosystem of traditional players

Computationally difficult problems

High cost of failure

Difficult for existing players to consider other ways of working

# Can we modernise IC development??

# Looking back..

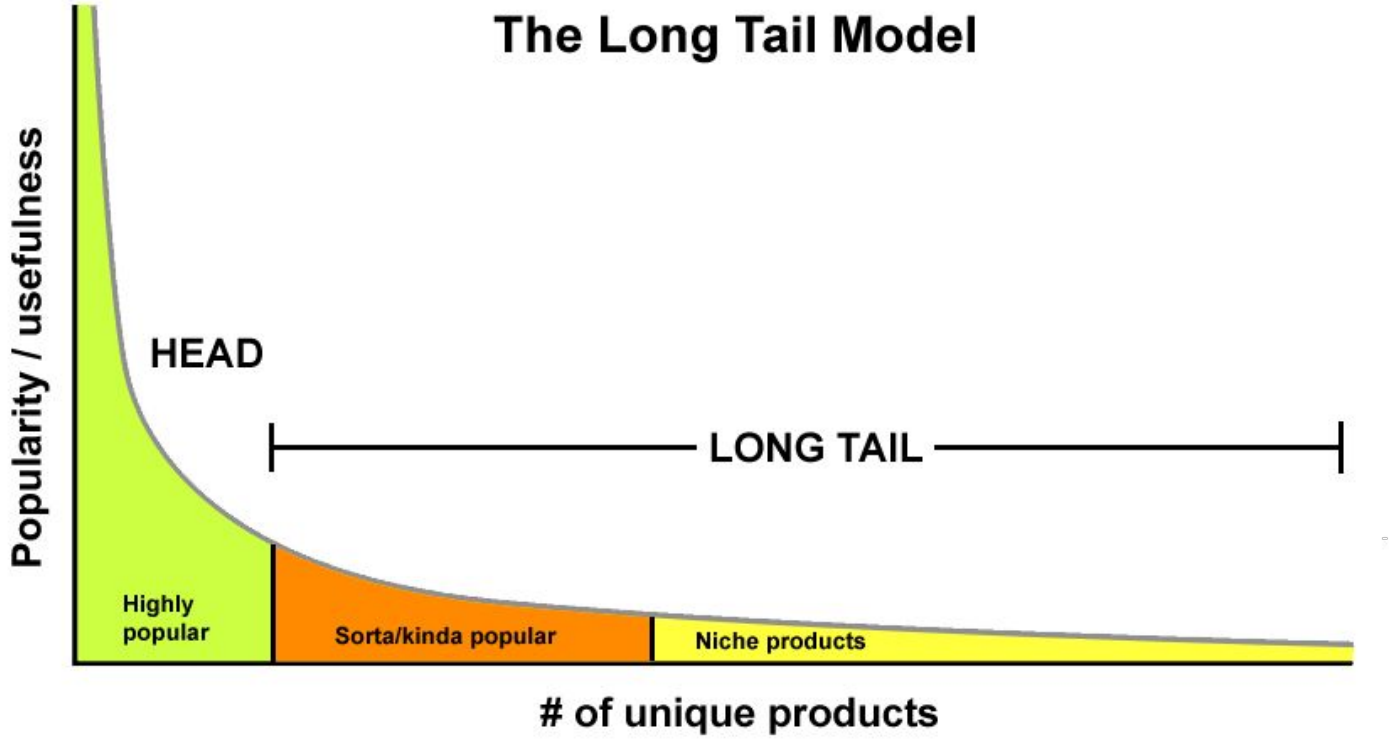
Looking back to the early days of Open Source Software ...

**No one won** going head to head with MS/Oracle etc

The wins were **enabling** products and business models that couldn't be supported by the incumbents

This gave us **Google, Facebook, Amazon, Netflix, and the modern internet.**

# Enabling a long tail?



# Enabling a long tail?

1) Those with insufficient volume, the economics are not viable. They could be shipping half a million a year, and struggle for a custom design to be justifiable.

2) For those companies that ship sufficient volumes, it's often a “bet the company” problem, even if they can allocate the 10 million USD that is needed to get started.

3) Even for product companies with sufficient volumes, most lack the business and technical expertise to consider building a chip.

# A vision

**Simple** python-based development environment

**Curated** & verified library of open source IP

**High-level** debugging with full design introspection

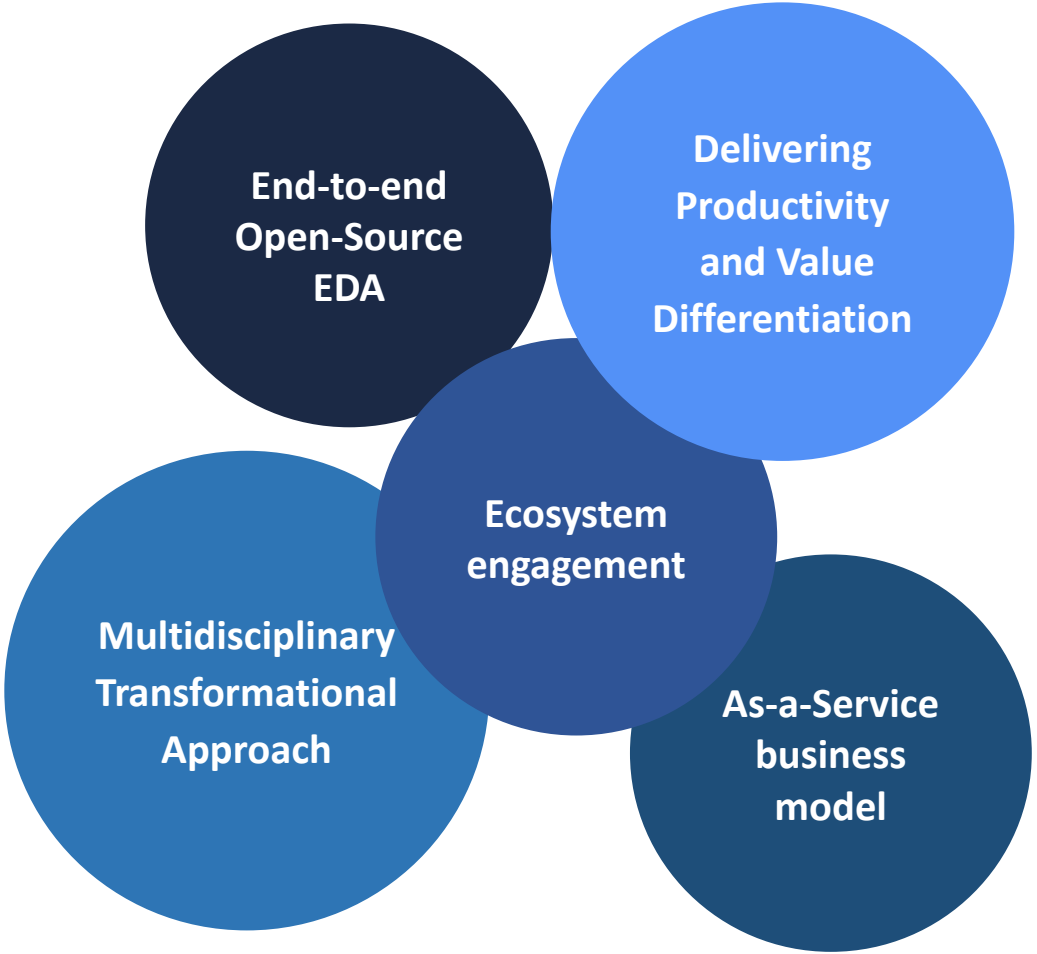
**Automated** physical flow

**Click-to-fab**, with straightforward pricing and predictable time lines

# Chipflow in a nutshell

**Disrupting the EDA market**
because it needs to happen, and
*the time is right*

- **Headquartered in UK**
- **Integrated with Europe's advanced research ecosystem**
- **Partially H2020 funded**
- **1st Customer contract signed**
- **Multidisciplinary team**
- **DNA not for sale**
- **Geopolitics agnostic**



# ChipFlow Team

OSS — Open-Source Software and Open-Source Hardware leaders

EDA — EDA Veterans and innovators

IP — World leading IP designers

T12N — Global technology transformation experts

**Robert Taylor, M.A.**

Leader in Commercial Open-Source

**Staf Verhaegen, M.Eng.**

Open-Source Physical Design expert (PDKMaster)

**Tomi Rantakari M.Sc (x2)**

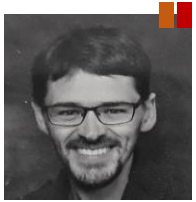
Global leader in Digital Transformation

**Matt Venn**

Open Source HW Go-To-Market expert (incl. Yosys HQ)

**Michael Laudes**

35 years of EDA Leadership



**Pepijn de Vos**

Open-Source Analog and Physical Design

**Olof Kindgren M.Sc**

Open-Source Hardware Thought Leader

**Myrtle Shah M.Sc**

Open-Source Place and Route Expert

**Dr. Barry Cook**

Space ASIC & FPGA Expert

**Ian Page**

Founder, Celoxica, Professorships at Oxford & Imperial

**To Be Announced**

A World Leading AI Chip Design authority

# The approach

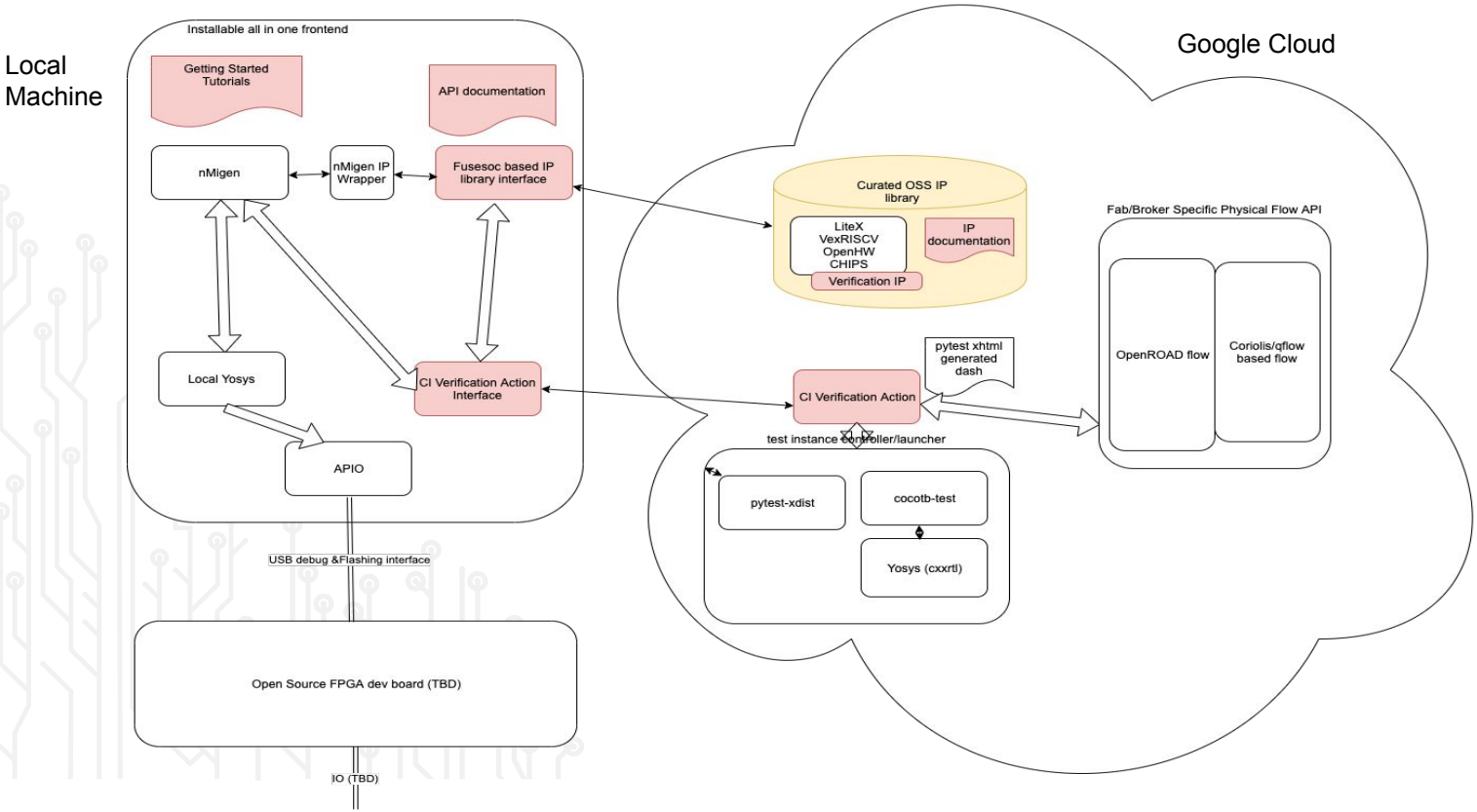
Start **constrained** - Target specific market sectors, constrained solution space

Focus on **developer experience**, productivity and predictability.

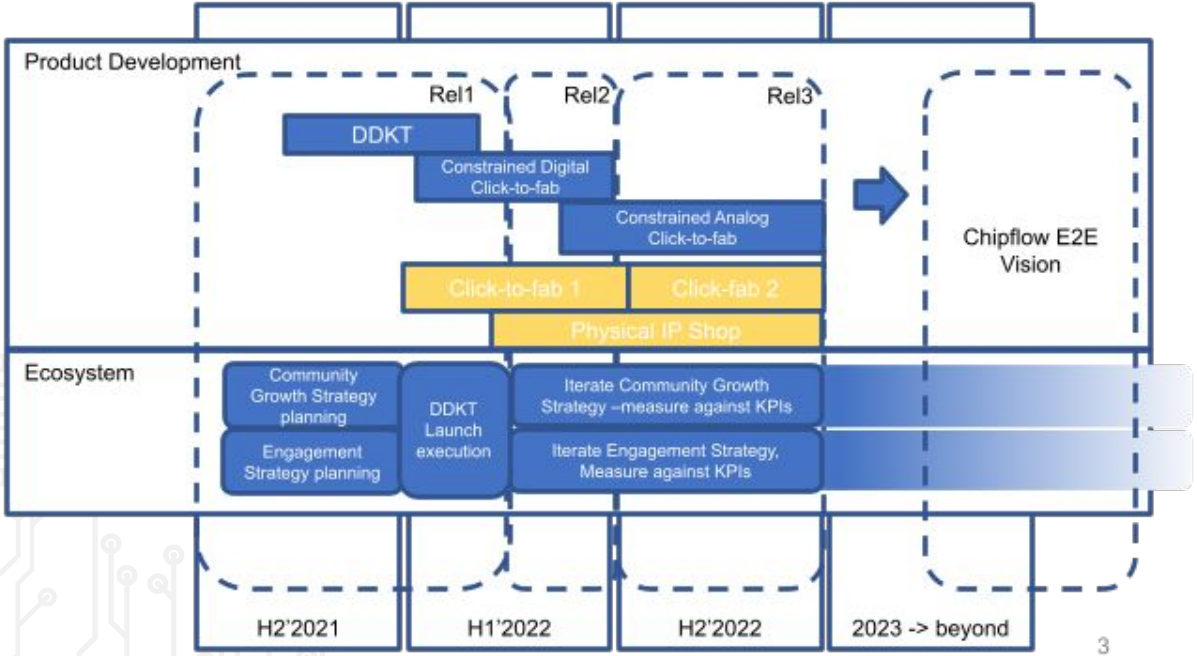
**Integrated** approach for physical flow - one framework to encompass the design from techmapping to final routed output, covering both digital and analog.

Work with foundries, brokers to reduce test chip **round-trip-time**.

# The technology - Rel 1&2 (WIP!)



# Roadmap - First steps



# Get Involved!

Collaborations? Joint projects?

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