

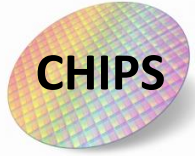


# **CHIPS: CERN-HEP IC design Platform & Services**

**F. Faccio** on behalf of X. Llopart

EP-ESE-ME

5 October 2021



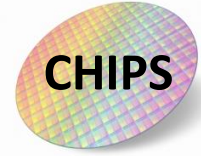
# CHIPS is an ASIC support service for HEP

- The CHIPS service started in January 2020 to address the concern, expressed by the CERN SPC (Scientific Policy Committee), that delays in the development of some ASICs could have serious repercussions on the physics programmes of the HL-LHC experiments
- These delays were attributed to the increased complexity of both the ASICs and the tools required for their development in the sub-micron technologies chosen for the upgrades

## CHIPS: CERN-HEP IC design Platform & Services

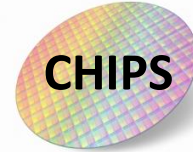
- ASIC design support from EP-ESE-ME experienced designers to HEP community
- Subcontract specialised ASIC design tasks
- Train and coach HEP ASIC designers in medium to long term

Responsible: X. Llopart  
From January 2020



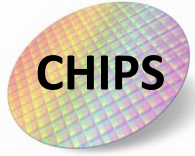
# CHIPS Manpower

- Support requests are shared amongst the EP-ME-ESE ASIC expert designers:
  - 5 FTE: Analog and macroblock design, radiation effects
  - 5 FTE: Digital implementation, timing closure and physical verification
  - 1 FTE: Functional verification and top-level simulation
- In addition, 4 engineers are at present fully committed to directly provide support, being integrated in the team developing specific ASICs
  - 2 Fellows (1 Digital + 1 Verification)
  - 2 Staff members (Verification)



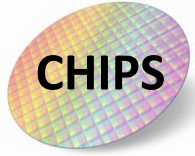
# Sustained support provided in 2020-21

	ASIC	Experiment	Support
WP1	MPA and SSA	CMS outer tracker	<ul style="list-style-type: none"><li>• 1 fellow (digital design) 11 months full time + 6 months at 50%</li><li>• 1 fellow (verification) 16 months full time + 3 months at 100%</li></ul>
WP2	ALTIROC	ATLAS HGTD	<ul style="list-style-type: none"><li>• Host 1 engineer for 1 month (Hot desk)</li><li>• 1 fellow (digital design) 9 months at 50%, now assigned for 9 months at full time</li><li>• 1 fellow (verification) now assigned for 9 months at full time</li></ul>
WP3	RD53_ATLAS and _CMS	ATLAS & CMS pixel detector	<ul style="list-style-type: none"><li>• 1 staff member (verification) full time for 11 months, now assigned for another 9 months</li></ul>
WP4	ECON-T and ECON-D	CMS HGICAL	<ul style="list-style-type: none"><li>• Occasional technical support (tools, digital flow scripts, SEE fault injection verification and use of TMRG tool,...)</li><li>• 1 staff member (verification) full time for 9 months, now assigned for another 3 months</li></ul>
WP5 WP6	HCCstar	ATLAS ITK (Strip Detector)	<ul style="list-style-type: none"><li>• Rolling-review process: 25 meetings during 9 months</li><li>• Occasional technical support (SEE, TMRG, VOLTUS)</li><li>• Evaluation and development of blocks to prepare a possible backup in 65nm (now dropped)</li></ul>



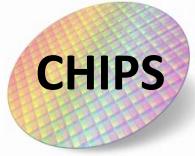
# Occasional support provided in 2020-21

- CHIPS coordinates the participation of the ME-ESE engineers in ASIC Design Reviews and technical design meetings (verification, power analysis, TMR strategy):
  - More than 25 ASIC reviews since January 2020 with the participation of 2-4 ESE engineers
- Support given since January 2020 to:
  - ATLAS: RD53, ITK (HCC\*, AMAC, ABC\*), AM08, ALTIROC2, LAr ADC, BCM
  - CMS: RD53, HGCal (HGCROCs, ECON-T), TOFHIR, LiTE-DTU, OT(MPA2, SSA2, CIC2.1), ETROC2
  - Others: IpGBT chipset, ALICE ITS3, H2M, BLM, ACCURATE, MALTA, ...



# Most common type of Support

- By order of effort required:
  1. Functional verification:
    - Lack of strategy from project start: Mixed signal, gate-level netlist, SEE verification?
    - Appropriate choice of methodology: Tools, randomization approach,...
  2. SEE robust design (TMR):
    - Task is often taken too late in the project → larger than expected area/power increase
  3. Digital flow scripts
  4. Power analysis (Voltus)
  5. Transition to digital-on-top (DoT) designs:
    - Characterization of Memories and full custom blocks
  6. Analog design support



# Summary

- CHIPS is a service aimed to give ASIC design support to HEP ASIC designers:
  - Involve experienced practitioners (EP-ESE), sometimes adding them directly to the design Teams
  - Train and coach ← After the COVID stop, we can resume “hot desks” for on-site coaching
- Service is hosted in the EP-ESE-ME (chips.support@cern.ch):
- Support was given to many projects in 2020-21:
  - Occasional support in the form of dedicated reviews, specific SEE meetings, TMRG tool, ...
  - Long term support to the development of ASICs for 6 detector systems: CMS Outer Tracker, CMS pixels, ATLAS pixels, ATLAS ITK, CMS HGAL, ATLAS HGTD
- The support is widely acknowledged to make a difference in increasing the quality of the design process, and most often to shorten the time to complete the development