RD50 CMOS Meeting

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16/09/2021

UNIVERSITY OF LIVERPOOL

Agendas

- TestStructure with Capacitor Measurement Circuit
- NMOS Trim DAC Variations
  - NMOS Trim DAC TUNE_IN + TUNE_TH
  - NMOS Trim DAC TUNE_IN
  - NMOS Trim DAC TUNE_TH

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TestStructure with Capacitor Measurement Circuit

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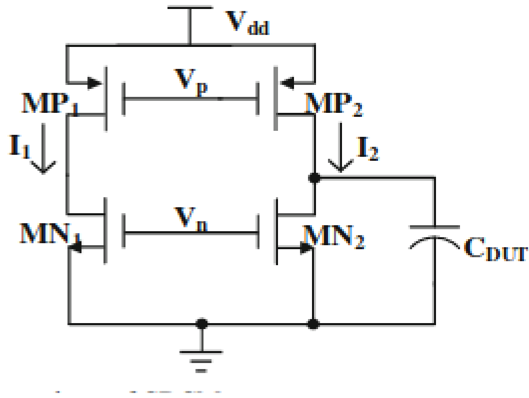
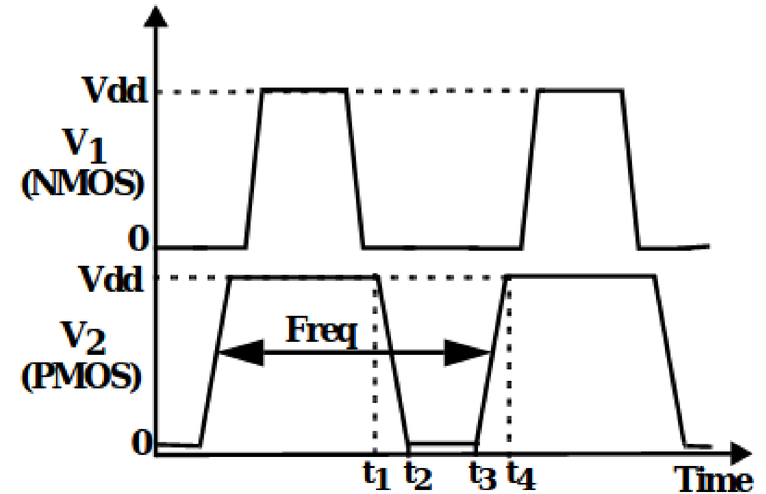
Theory from Literature



$$C_{\mathrm{DUT}} = \frac{(I_1 - I_2)}{V_{\mathrm{dd}} \cdot f}.$$

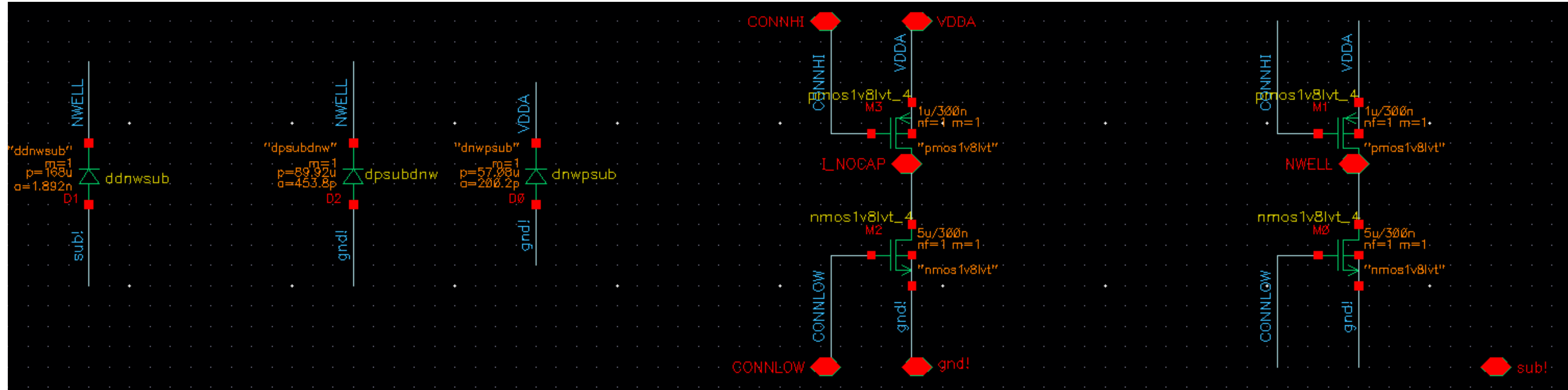


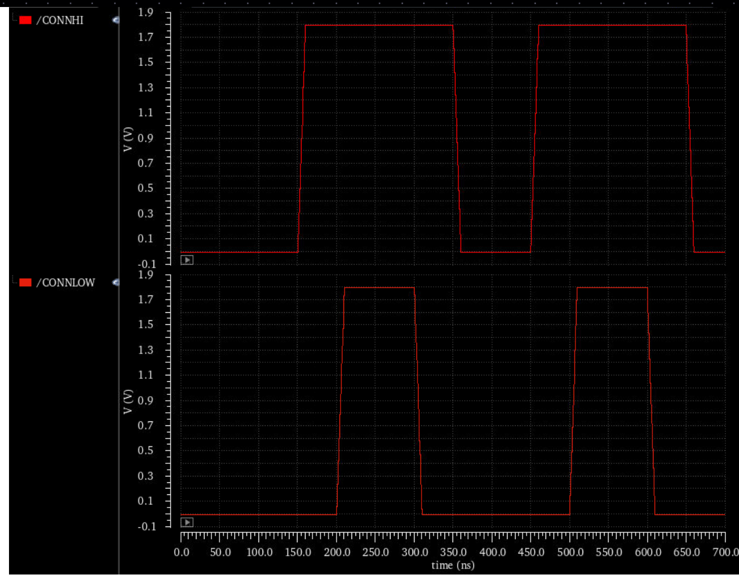
1. Zhu, D., Mo, J., Xu, S., Shang, Y., Wang, Z., Huang, Z., & Yu, F. (2016). A new capacitance-to-frequency converter for on-chip capacitance measurement and calibration in CMOS technology. Journal of Electronic Testing, 32(3), 393-397.

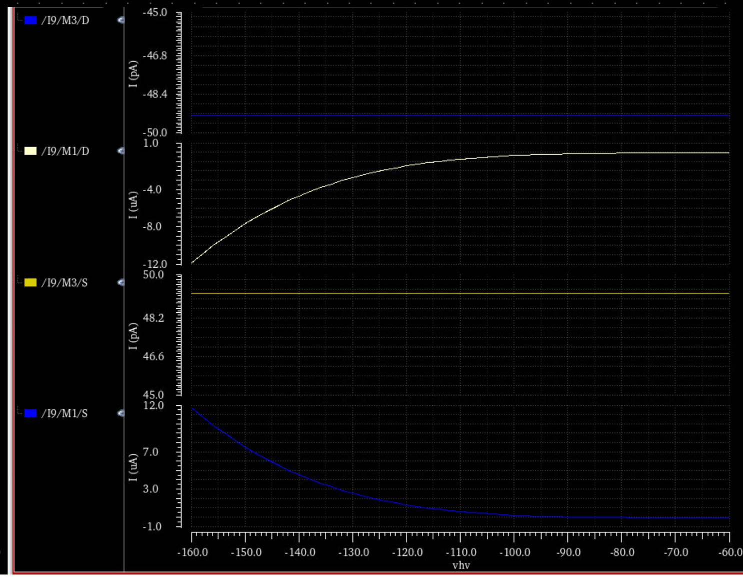
2. Chang, Y. W., Chang, H. W., Lu, T. C., King, Y. C., Ting, W., Ku, J., & Lu, C. Y. (2006). Interconnect capacitance characterization using charge-injection-induced error-free (CIEF) charge-based capacitance measurement (CBCM). IEEE transactions on semiconductor manufacturing, 19(1), 50-56.

3. Chen, J. C., McGaughy, B. W., Sylvester, D., & Hu, C. (1996, December). An on-chip, attofarad interconnect charge-based capacitance measurement (CBCM) technique. In International Electron Devices Meeting. Technical Digest (pp. 69-72). IEEE.

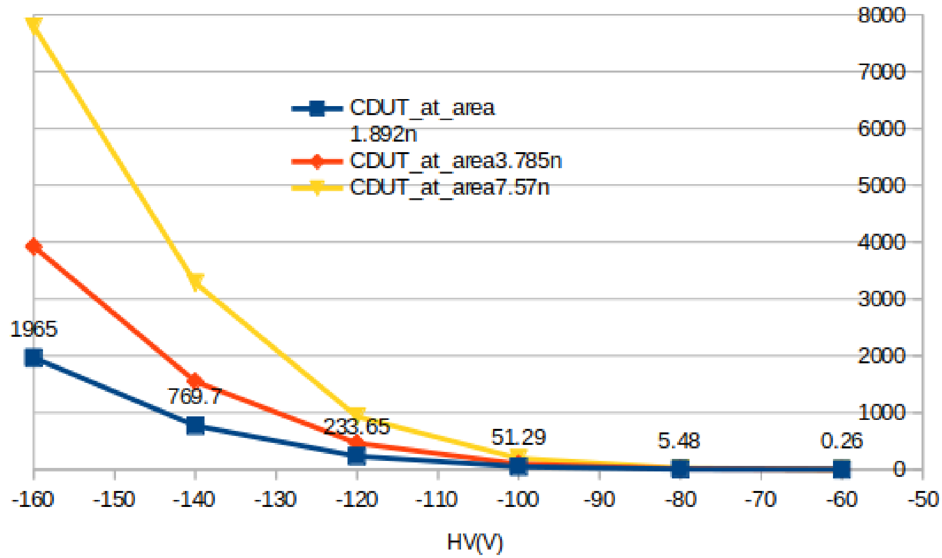
Schematic & Simulation Waveforms



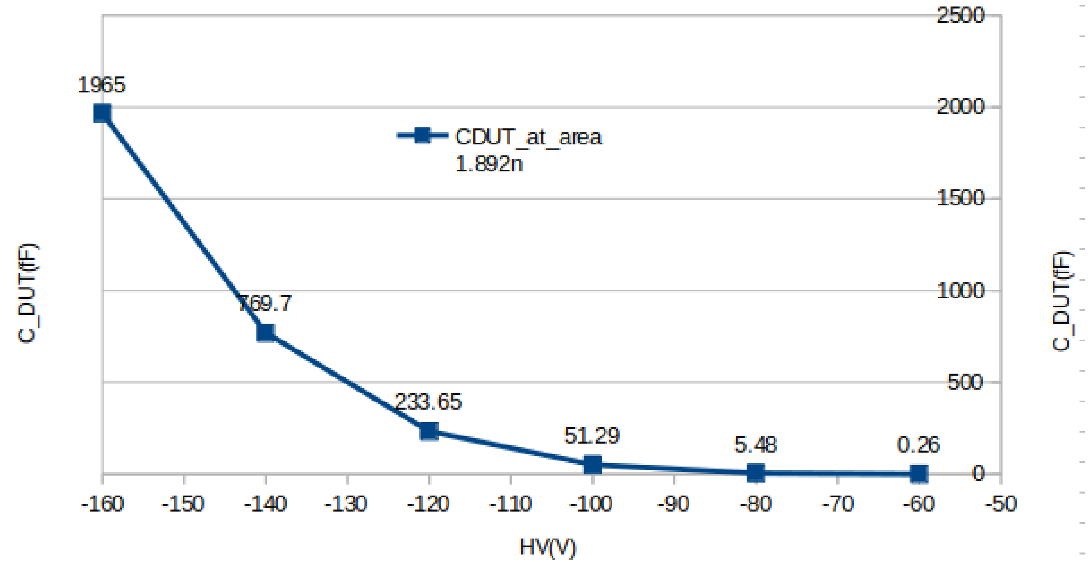




HV(V) vs. Capacitance of the NWELL



Considering different arbitrary areas to check if C_DUT changes with area



Considering the area in the designed teststructure

Note: The area corresponds to ddnwsub

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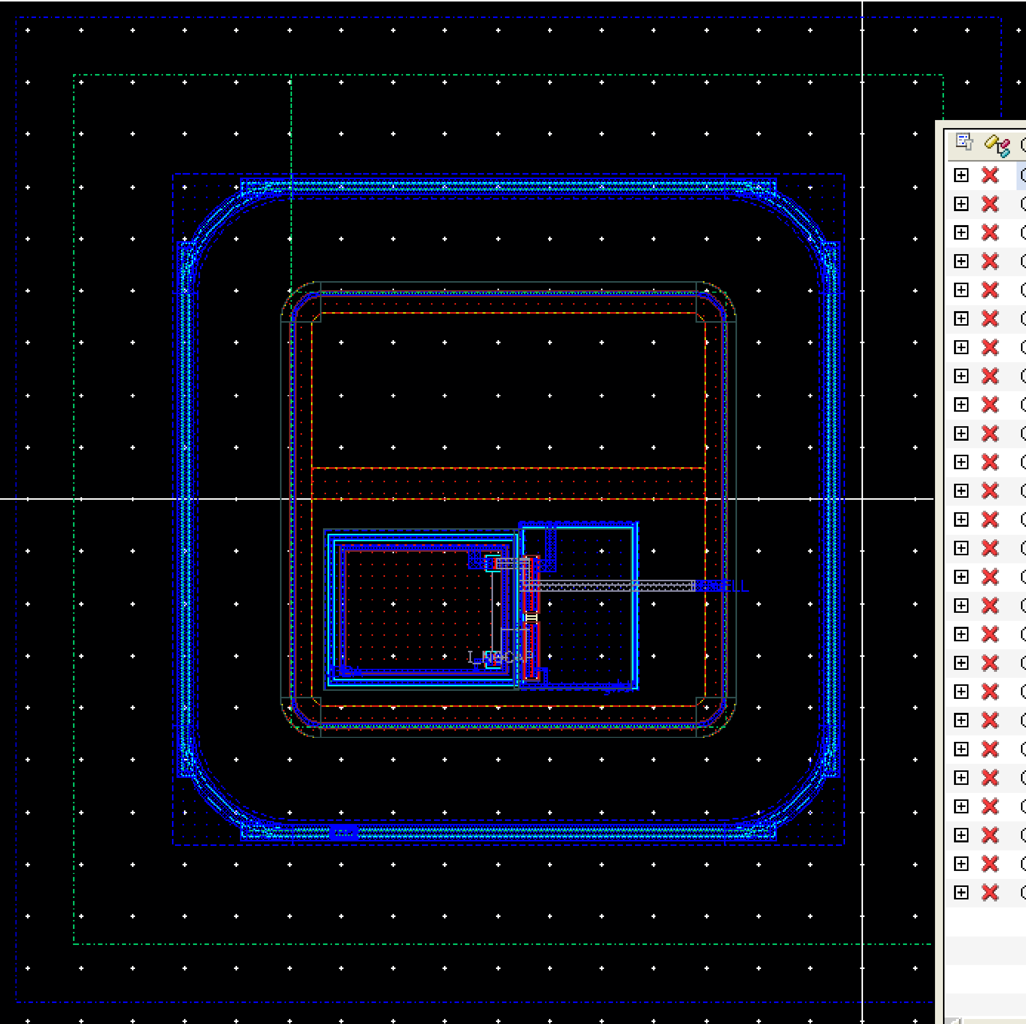
Verifications



Check / Cell	Results
Check METAL1.WIDTH	4
Check DNWRING.WIDTH	8
Check NISO.WIDTH	8
Check NISO_recommended.CLEARANCE.UC.NWELL	2
Check PWELL.WIDTH	6
Check PWELL_C.WIDTH	6
Check DNWELL.NEED.PSUB	2
Check DNWELL10.OVERLAP.NISO10	4
Check DNWELL10.OVERLAP.NWELL10	4
Check NISO.OVERLAP.NWELL	4
Check DIF.MINDENS.1	1
Check DIF.MINDENS.2	1
Check POL.MINDENS.1	1
Check POL.MINDENS.2	1
Check ME1.MINDENS.1	1
Check ME1.MINDENS.2	1
Check ME2.MINDENS.1	1
Check ME2.MINDENS.2	1
Check ME3.MINDENS.1	1
Check ME3.MINDENS.2	1
Check ME4.MINDENS.1	1
Check ME4.MINDENS.2	1
Check ME5.MINDENS.1	1
Check ME5.MINDENS.2	1
Check MEF.MINDENS.1	1
Check MEF.MINDENS.2	1

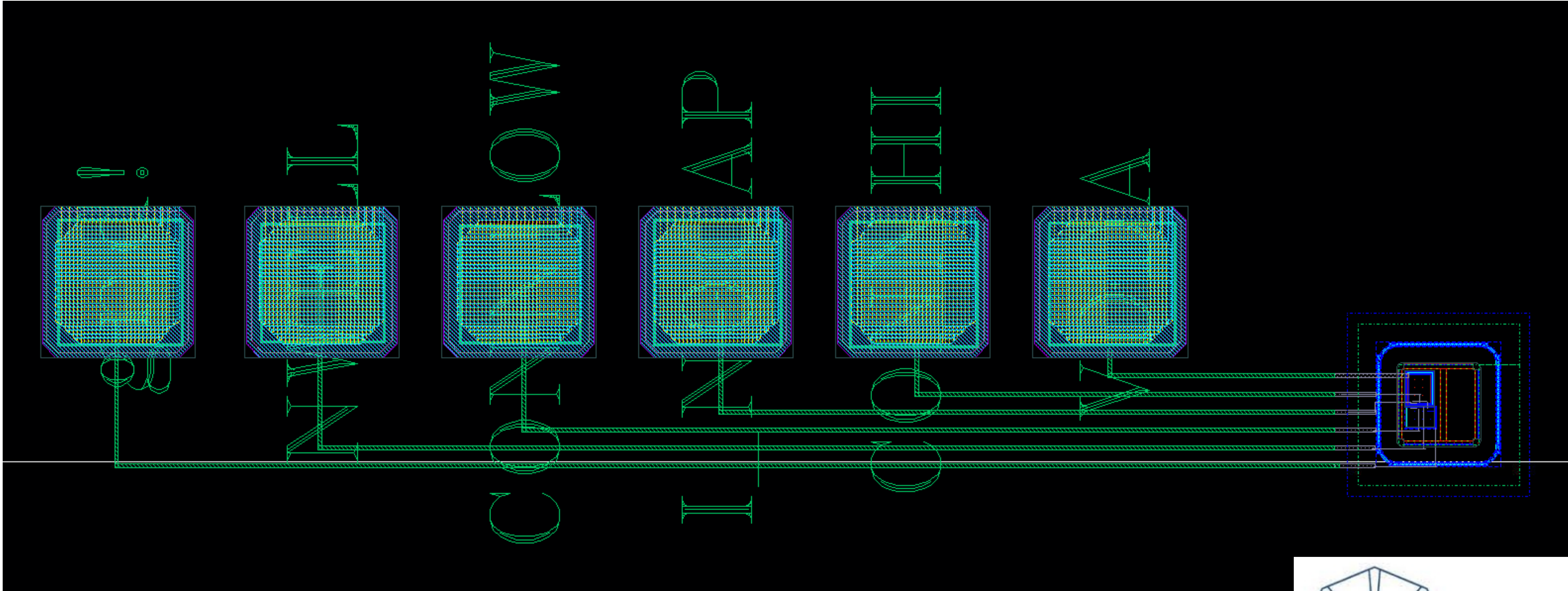
Cell DIODE_CAP_MEAS_four_transistor Summary (Clean)

```
                    CELL COMPARISON RESULTS ( TOP LEVEL )

                   #        ###################
                  #         #                 #
             #   #          #     CORRECT     #       _   _
              # #           #                 #         |
               #            ###################       \___/

LAYOUT CELL NAME:         DIODE_CAP_MEAS_four_transistor
SOURCE CELL NAME:         DIODE_CAP_MEAS_four_transistor

--------------------------------------------------------------------------

NUMBERS OF OBJECTS
------------------

                   Layout    Source        Component Type
                   ------    ------        --------------
 Ports:               7         7

 Nets:                7         7

 Instances:           2         2          MN (4 pins)
                      2         2          MP (4 pins)
                      3         3          D (2 pins)
                   ------    ------
 Total Inst:          7         7


**************************************************************************
                         INFORMATION AND WARNINGS
**************************************************************************
```

Cell DIODE_CAP_MEAS_four_transistor (Stamping conflict #1)

```
⚠ Warning: #1 in DIODE_CAP_MEAS_four_transistor
WARNING:  Stamping conflict in SCONNECT - Multiple source nets stamp one target net.
          Use LVS REPORT OPTION S or LVS SOFTCHK statement to obtain detailed information.
```

With PAD Connections



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NMOS Trim DAC Variations

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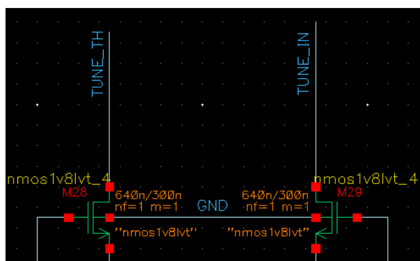
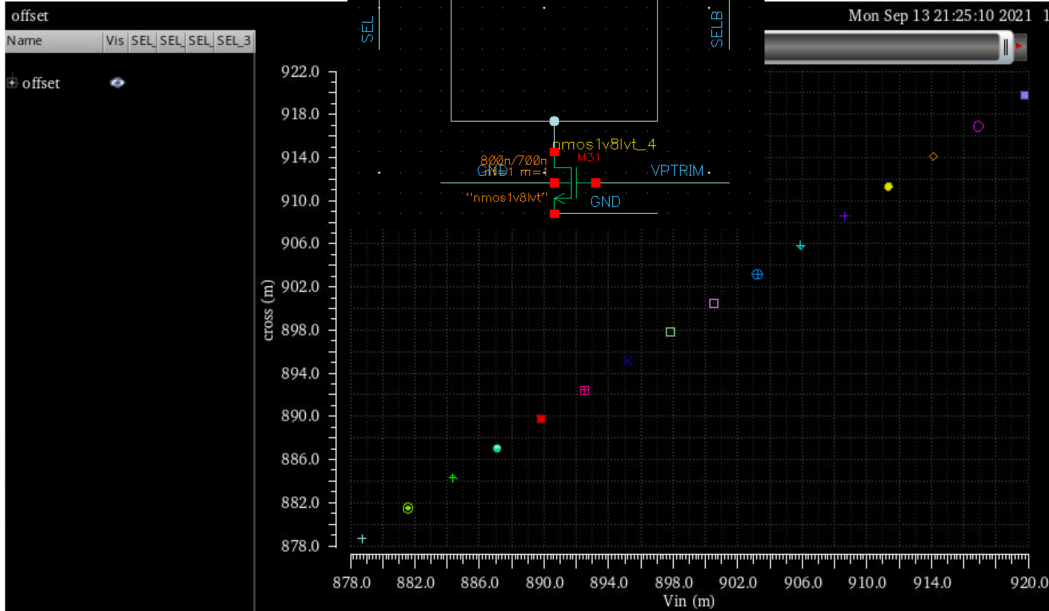
NMOS TRIM-DAC Cell with only TUNE_IN & TUNE_TH

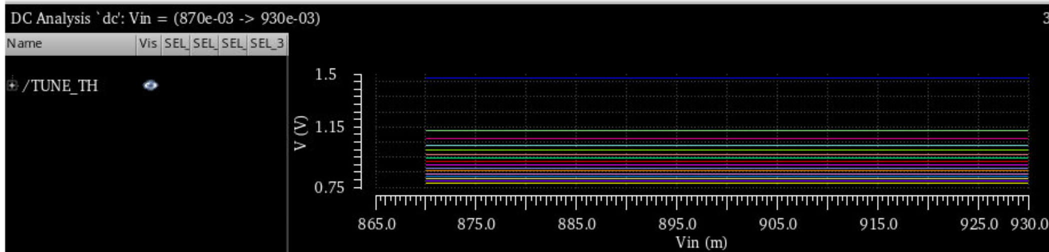


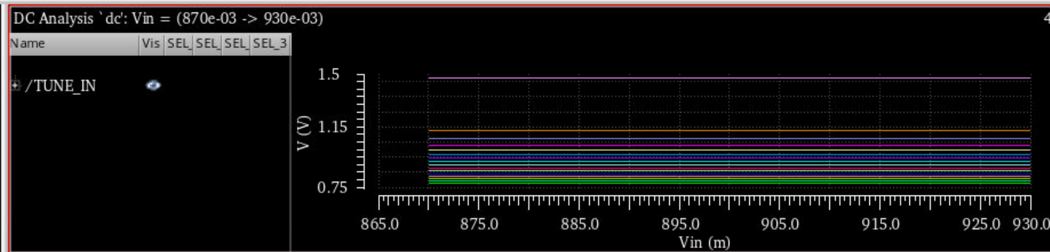
Number = 300
Mean = 898.662m
Std Dev = 6.86279m

3Xstd dev=20.58

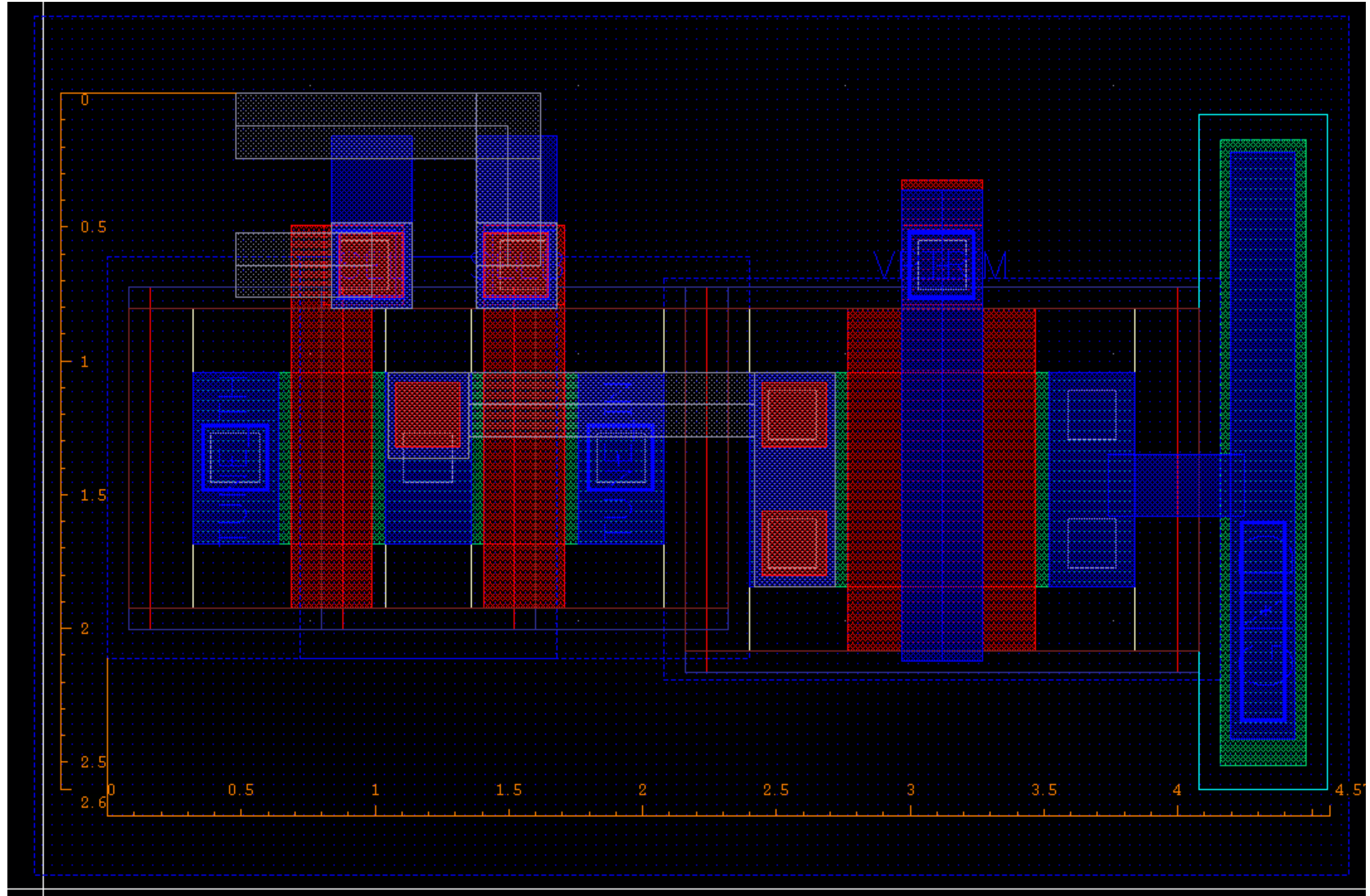


DC Response
Mon Sep 13 21:25:10 2021 2
Name Vis SEL SEL SEL SEL_3
/COMPOUT
V (V)
Vin (m)





NMOS TRIM-DAC Cell with only TUNE_IN & TUNE_TH (LAYOUT)



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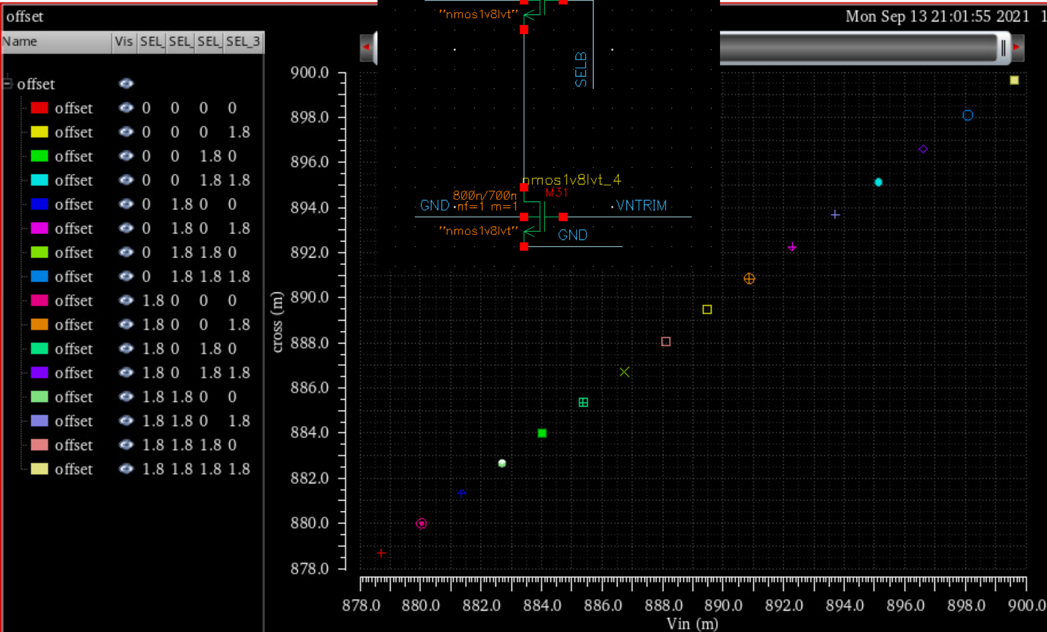
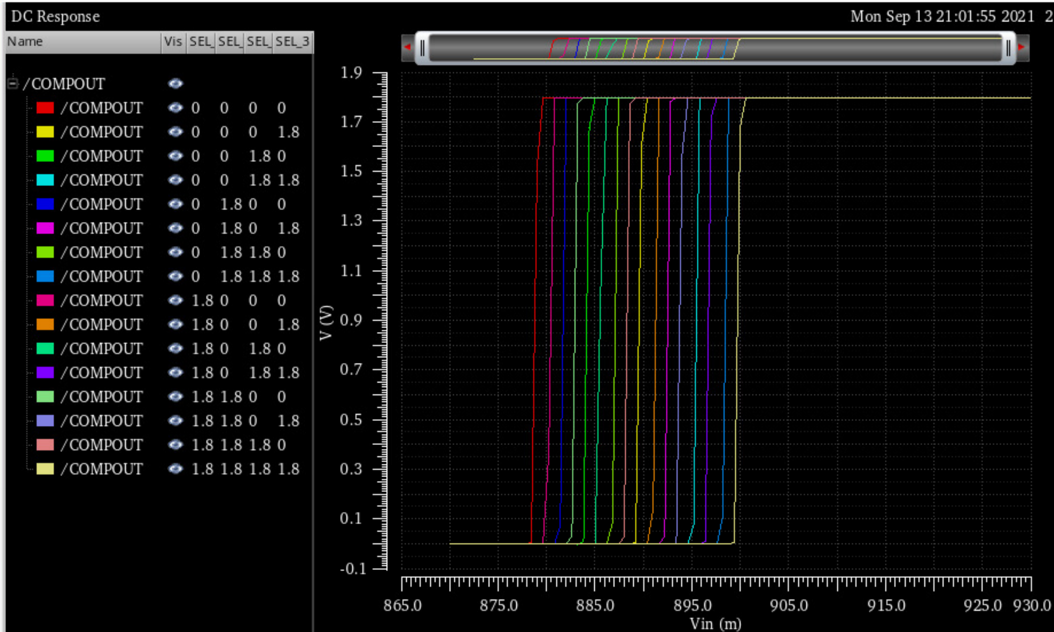
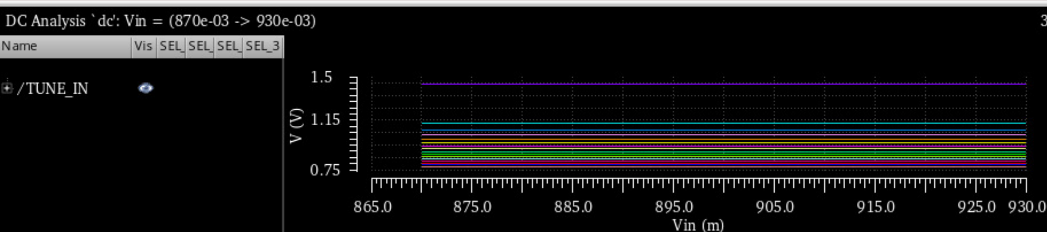
NMOS TRIM-DAC Cell with only TUNE_IN

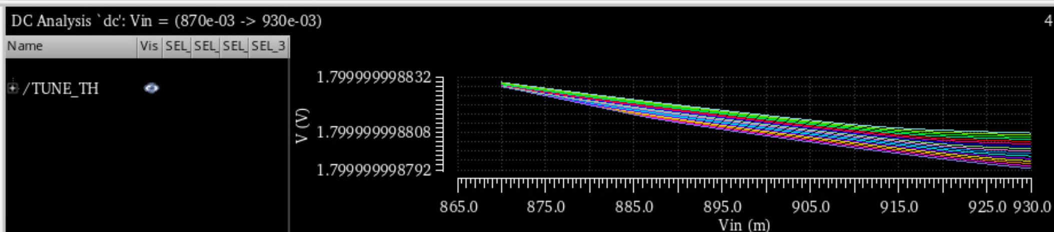
Number = 300
Mean = 898.662m
Std Dev = 6.86279m

3Xstd dev=20.58





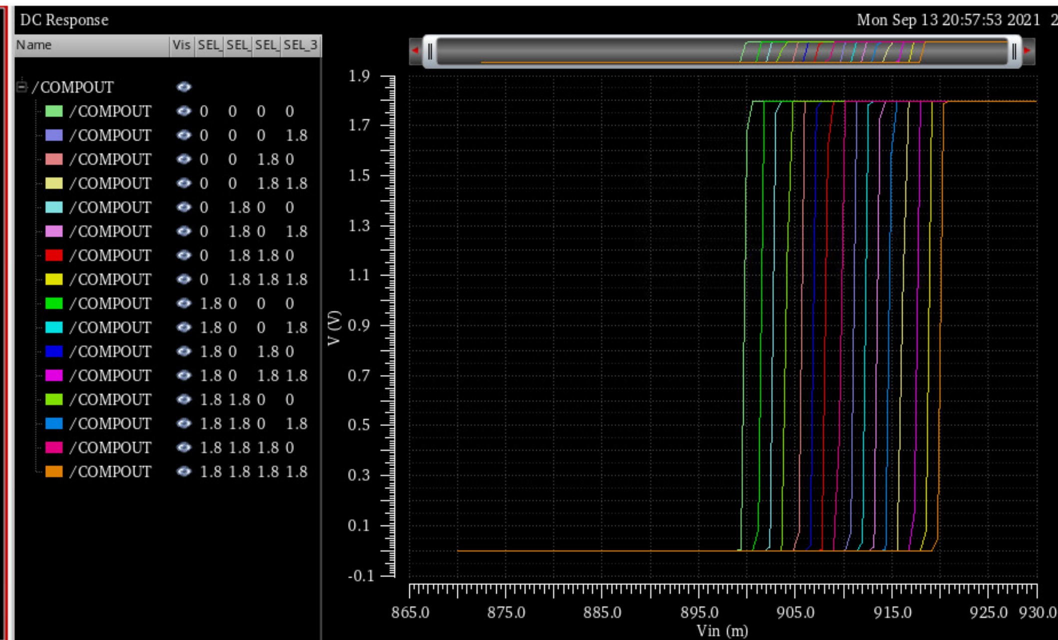


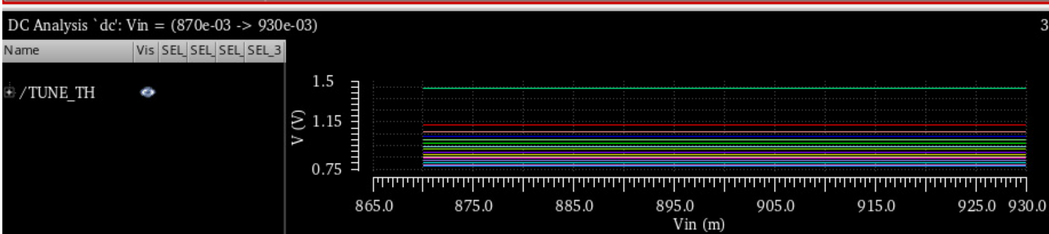


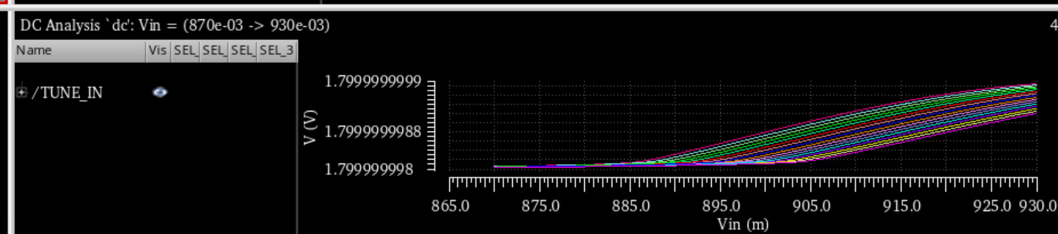
NMOS TRIM-DAC Cell with only TUNE_TH

Number = 300
Mean = 898.662m
Std Dev = 6.86279m

3Xstd dev=20.58







AtlasPix

Virtuoso® Schematic Editor L Reading: ADC DAC_V2 schematic

The inverted gate input/SELB is taken out. Which means TUNE_TH is used only.

THANK YOU

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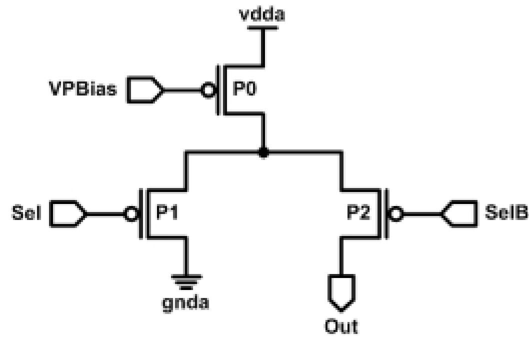
H35DEMO



TUNE_IN is used here since OUT is from SELB.