Experiment Control System (ECS) for the LHCb Outer Tracker Electronics Upgrade possibilities and problems

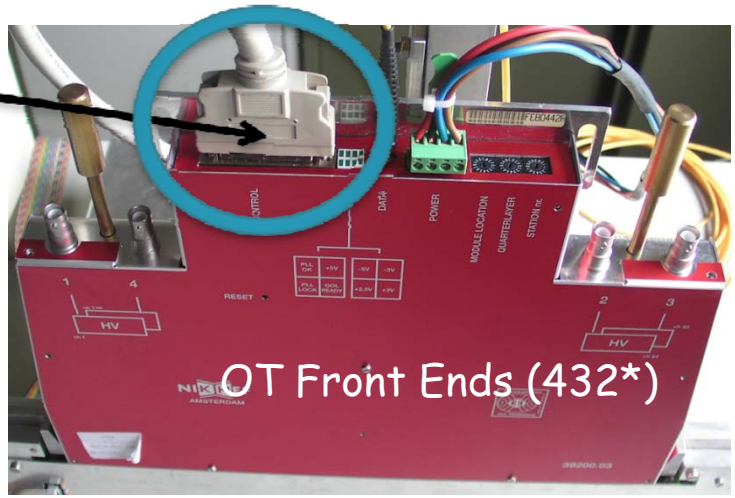
Outer Tracker wire chamber modules with Front Ends.

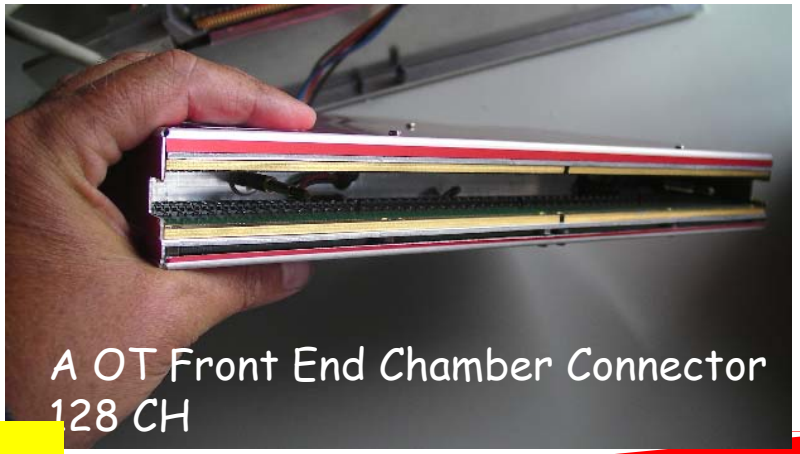
Present Situation Outer Tracker

At present we have
only few TFC fiber (24)
and ECS connections (24)
For 432 Front Ends.

We use 24 Control-Boxes
each for 18 times "fan-out"
to detector Front Ends

They fit in the very
tight C-frame space





Control-Box ECS and TFC
for 18 Front Ends
In : 1 TFC fiber and 1 SPECS cat5
Out: 25*LVDS for 18 FE's

1 Fiber(TFC) &
1 Cat5(ECS/SPECS)

Present Situation Outer Tracker

- 12 C-frames with each 36 Front Ends =
  Total 432 FE that need Control

- Each C-frame has 2 Control-Boxes
  for distribution of fast/slow control

  (Future will be 432 individual control dual-fibers
  needed for daq tx clock)

- Each Front end has 25 Control signals incl spare
  (Fast and Slow, ECS/ TFC)

What kind of signals go to a Front End?

Present Signals:

1 i2c master to slave (diff FE-input)
2 i2c slave to master (diff FE-output)
3 i2c clock (diff FE-input)
4 -
5 measurement1 +3V (diff FE-output)
6 measurement2 -3V (diff FE-output)
7 measurement3 +2.5V (diff FE-output)
8 measurement4 temp FE (diff FE-output)

9 GOL status (diff FE-output)
10 GOL OFF (diff FE-input)
11 2.5V inhibit (diff FE-input)
12 -
13 testpulse1 odd low (diff FE-input)
14 testpulse2 odd high (diff FE-input)
15 testpulse3 even low (diff FE-input)
16 testpulse4 even high (diff FE-input)
17 -
18 -
19 -
20 Pow up reset (diff input)
21 L0 Reset (diff fast input)
22 Ev count reset (diff fast input)
23 Bunch count reset (diff fast input)
24 L0 trig accept (diff fast input)
25 BX clock (diff fast input) **40 MHz**

ECS Slow Control
via Control Box distr.

Few DCU (ADC) chips so many analog signals measurement to multiplexors in Control Box

TFC Fast Control, 25ns

few circuits inside FE to make it radiation tolerant.
So 4 types of test pulses come directly from external Control box

ECS signals after the LHCb OT Electronics Uprgade

New Signals:

1 i2c master to slave
2 i2c slave to master
3 i2c clock
4 measurement1 +3V
5 measurement2 -3V
6 measurement3 +2.5V measurement
7 measurement4 temp FE

8 GOL status
9 QPLL status

10 FE Power on (procedure)

11 TESTPULSE 1 odd low
12 testpulse2 odd high
13 testpulse3 even low
14 testpulse4 even high

15 Bunch count reset
16 BX clock
17
18 FE reset
19
20
21
22
23
24

→ No new signals, we can skip a few (L0 accept and Ev count reset)

→ **ECS Slow Control**

Remarks:
- 432 Rad hard ADC needed (was inSPECS)
  future: DCU = 8ch ADC 12 bit inside

- 16ch DAC needed in FE (now in OTIS chip)

→ **TFC fast Control**

Remarks:
- clock passing from Control GBT to 8 DAQ-transmitter-GBT 's assumed 40MHz or 4.8Gb clock (2.4 MHz?)

Future Situation Outer Tracker ECS/TFC for Front Ends Question

Can the Data transmitters do with only 40MHz clock? (And I2C control)?

And still make a stable clock for the 4.8Gbps transmission?

So without the 4.8 Gb clock with < 40ps jitter

We assumed not

→ If so we can change the present OT-Distribution/ControlBox to have GBT dual fiber input , remove the TTC board and SPECS Slave, and keep the rest the same.
The 8 transmitter GBT's will still work

In this case we use only 24 control fibers (dual)

We could also keep the old TFC and ECS in the FE

Future Situation Outer Tracker

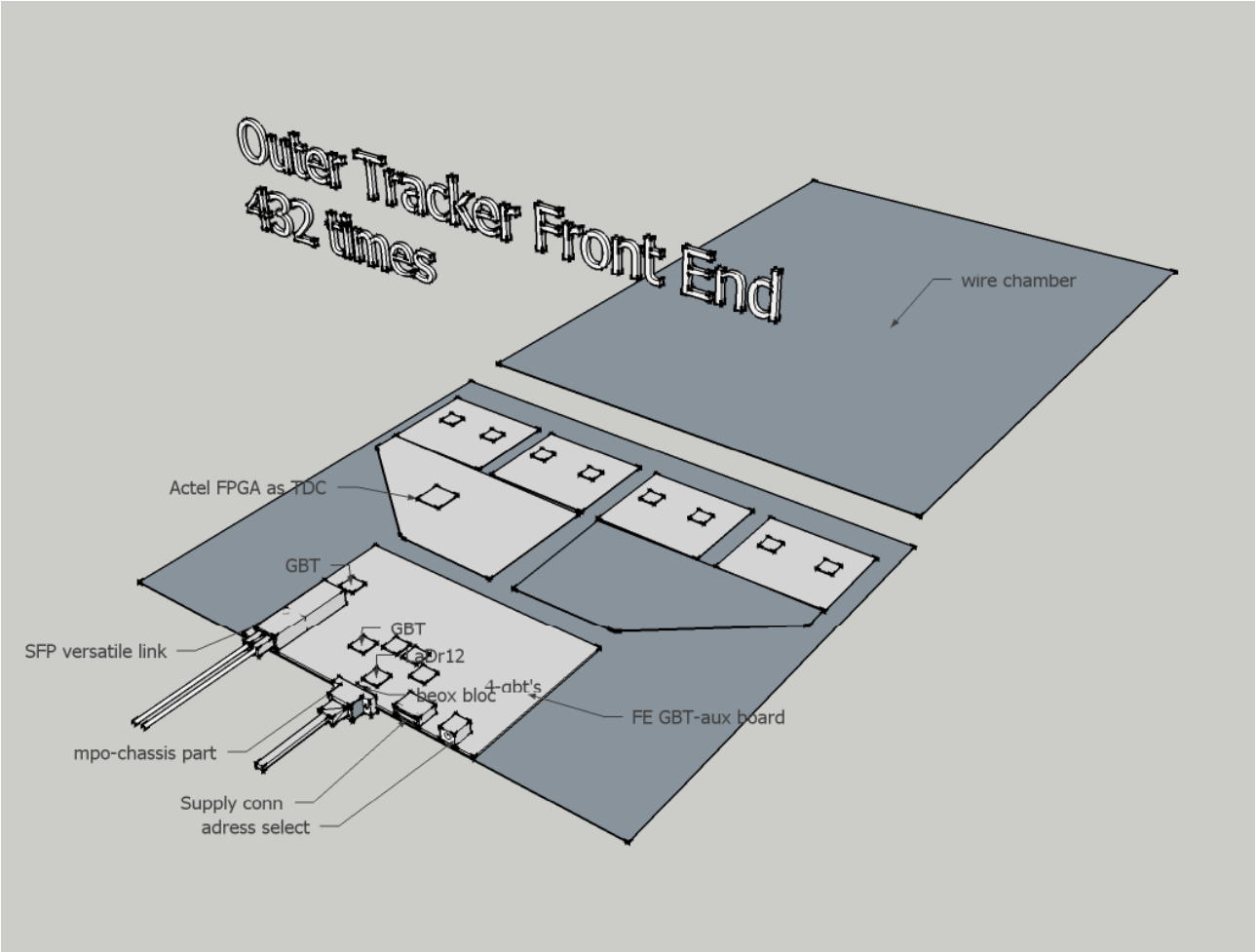
- Stable 4.8 Gbps Clock needed for FE 8tx's
  Each Front End needs TFC with very stable clock used for multiple GBT Data Fiber Outputs txclk (=200ps) Using the Control dual link

- Each FE needs 16 DAC channels for Threshold
  (now still in Otis Chip, not normally in FPGA)

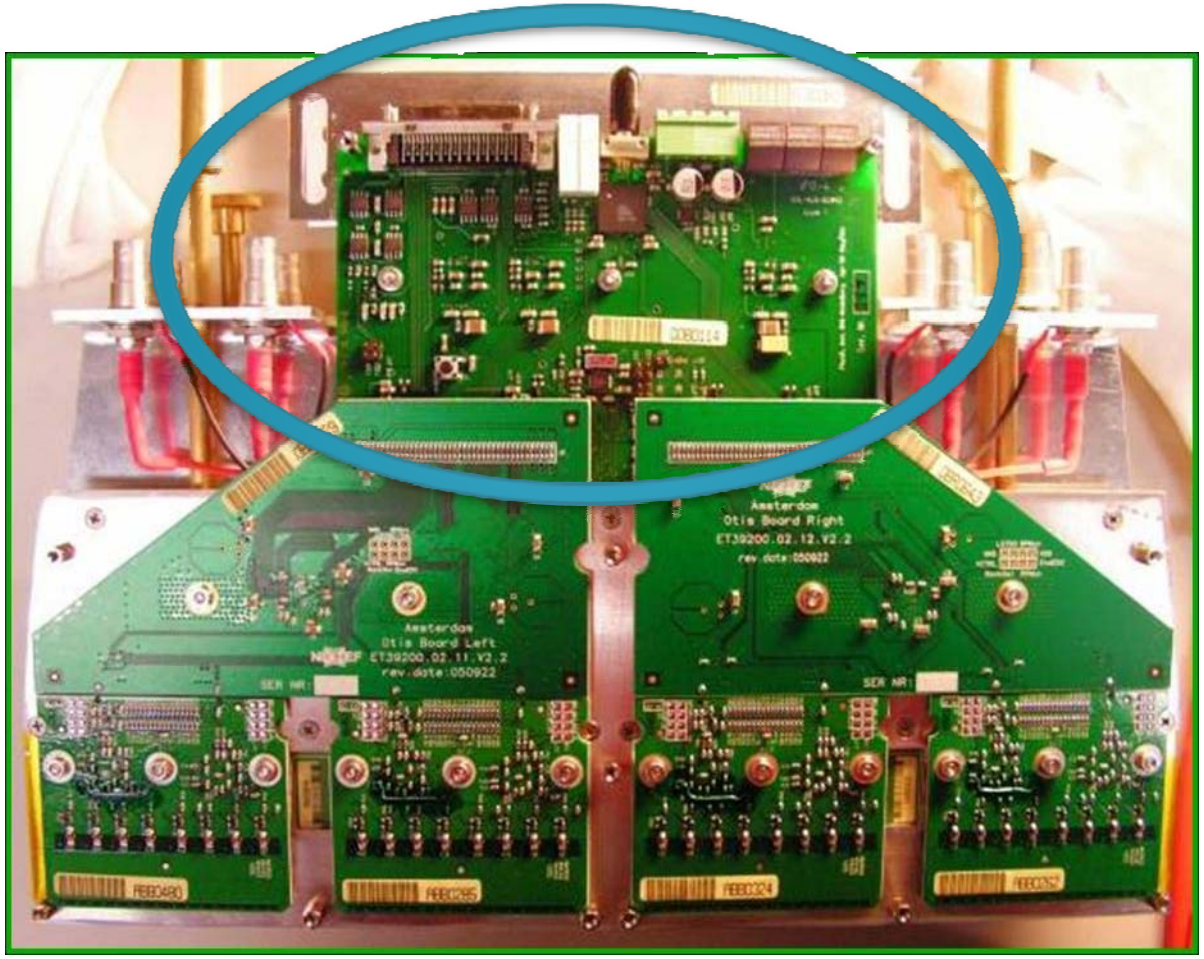
- Each FE needs >4 ADC channels Voltage for voltage and temperature monitor
  (now in Controlbox, SPECS-DCU chip from CMS dev. / CERN IC)

- Each FE needs I2C
- Each FE needs timed pulses (clock,tespulse, bx reset etc)

View of the future OT Front End

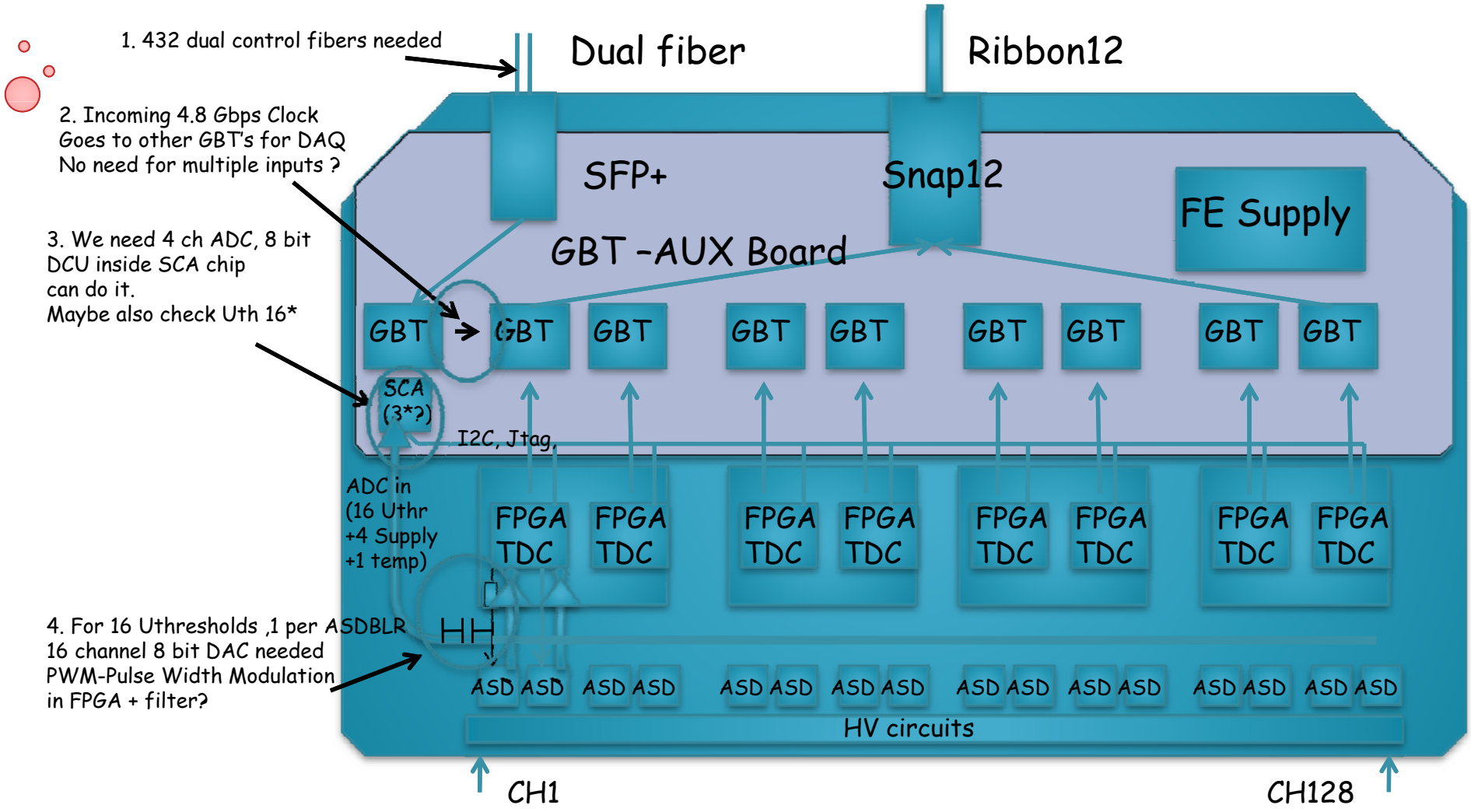


Old OT Front End PCB's

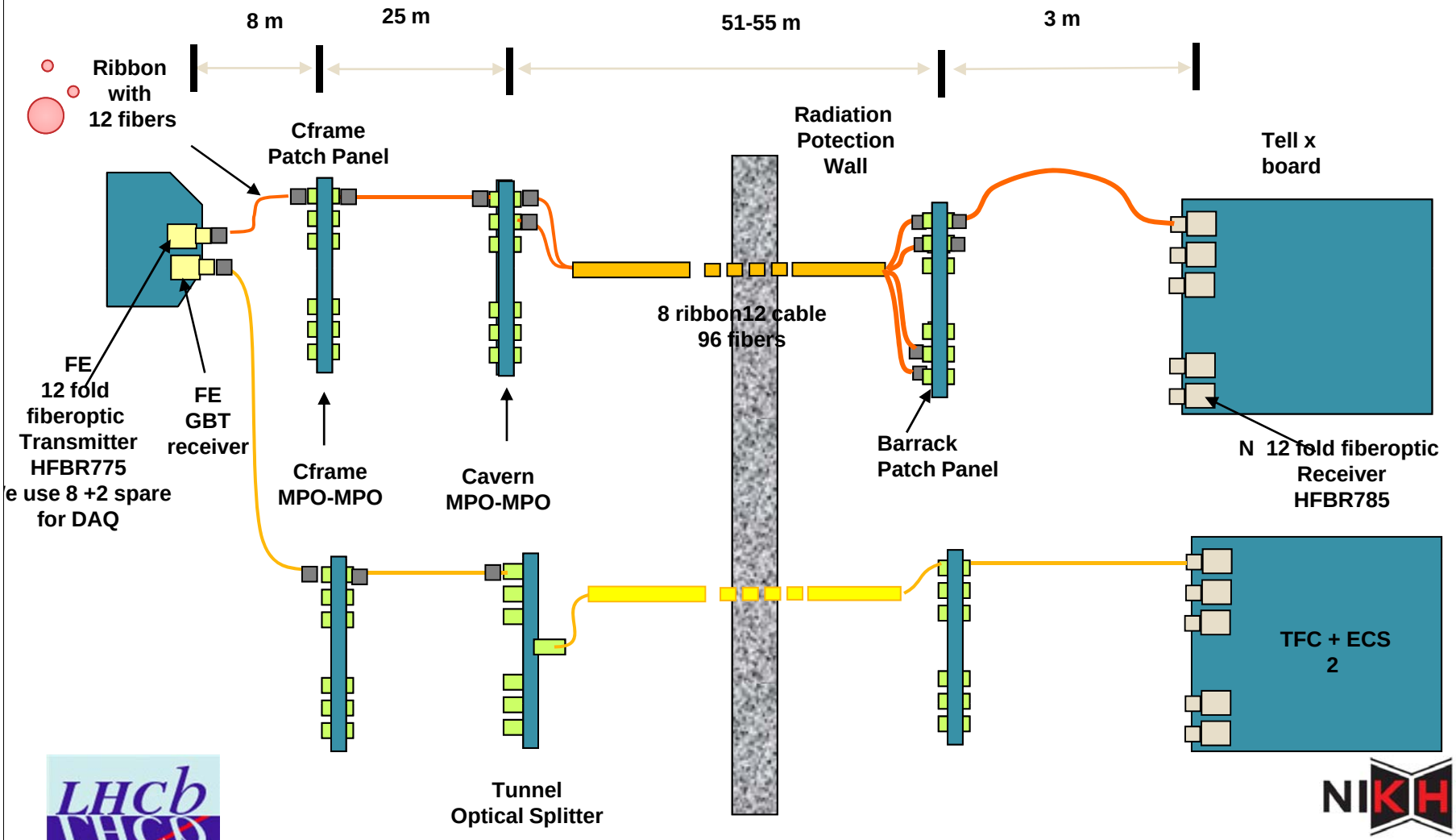


GOL/Aux
Board
to be changed
For 8 fiber outpu

Upgraded GBT AUX board in the 432 FE's



The “Ribbon +Duo per Front End” Solution -- With Separate TFC and ECS



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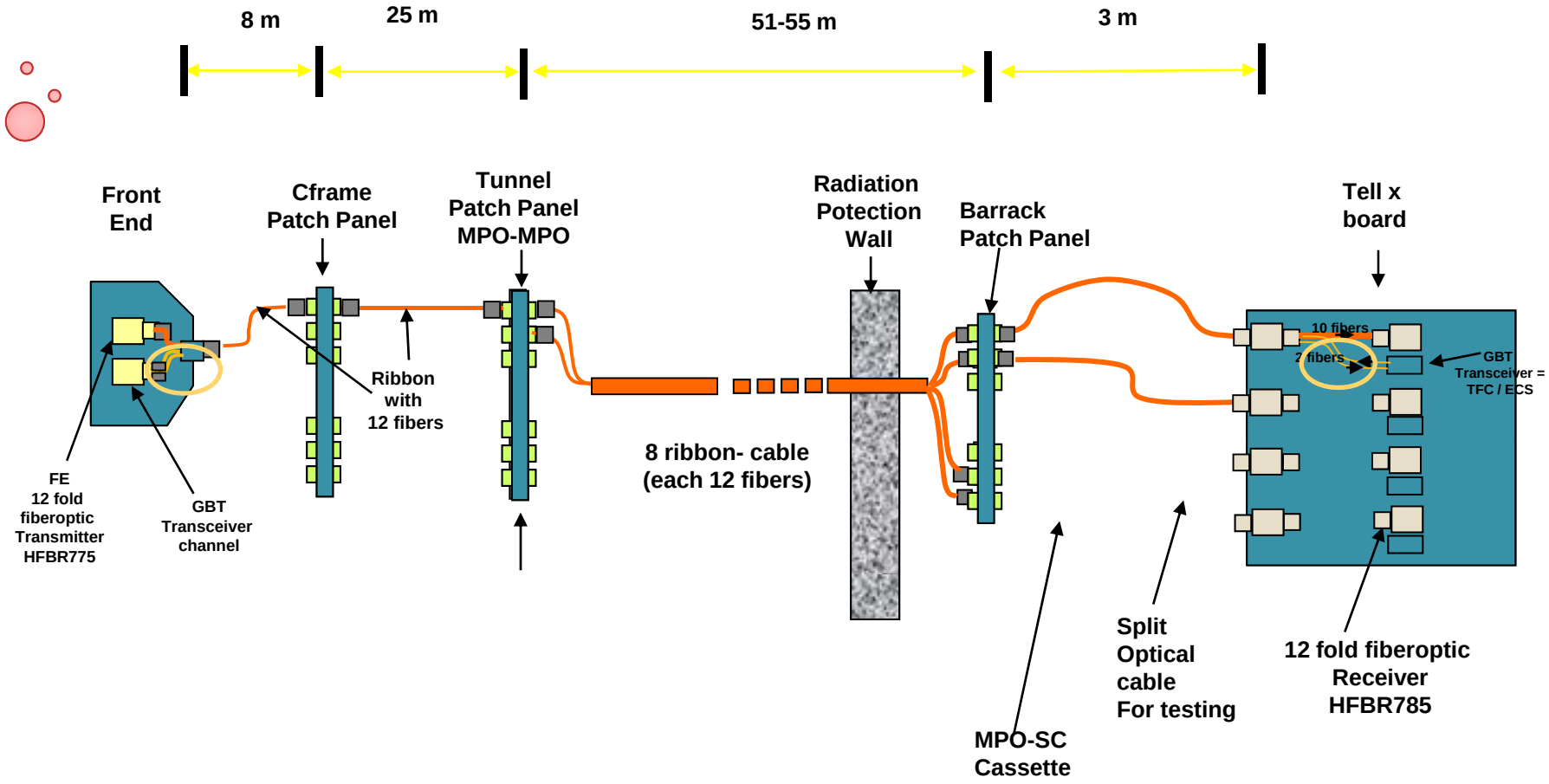
The “Single Ribbon per Front End” Solution – TFC and ECS on same Ribbon



TFC ECS Distribution

We need 432 dual fibers ex spare, for ECS/TFC is it too much ?

1. Can we make Optical Splitters in the FE-Rx fiber, since they can all listen to the same transmission?
(FE is addressable, DIL switches)

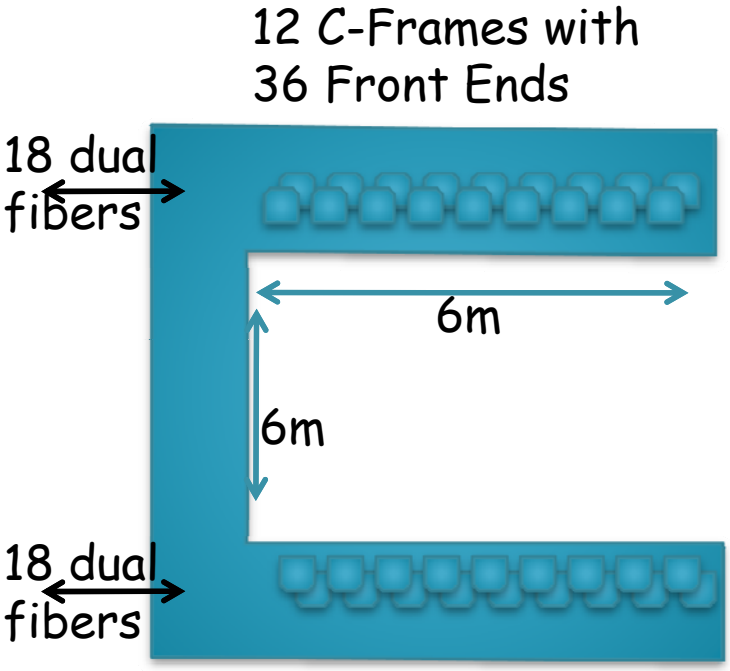
Problem: we would need high power outputs (8 fold splitters possible? 10dB)

2. Can we combine FE-Tx fibre's of several FE's? Since only the FE-addressed may talk

Problem: TX send idles the counting house stay in sync, combine fibers and there will be chaos

3. Can someone make electrical fan-out's/repeaters? (mix ok, if only 1 FE talks)

For now we need 432 dual control fibers from Counting House (and 3456 channels daq)



Questions TFC ECS Distribution

1. Can someone make fan-in/out for Control link (Dual fiber)
2. Will anybody produce multi channel DAC 8 bits res. ?
3. Can the GBT transmit without input fiber but only 40Mc clock

Wish list

1. We need 432 (ex spare) control fibers
   Maybe a fan-in/out can be made by Cern (GBT group)
2. We have to prove the GBT clock-sharing works, when the gbt arrives
3. We would welcome a multi (8,16) channel, Rad Tolerant DAC (>60Krad=600 Gray) ,
   ic2 controlled,
   otherwise we try a Pulse Width Modulator DAC (with filters)

Conclusion

Solutions to choose from, for the OT control:

1. Redesign Old controlboxes with
   new GBT fiber inputs,
   instead of tfc/ecs mezzanines
   (Only if gbt works on 40Mc)
   Advantage: Only 24 control dual fib

2. 432 Control links (dual)

3. Fan in/out near Cframes,
   rad tolerant.