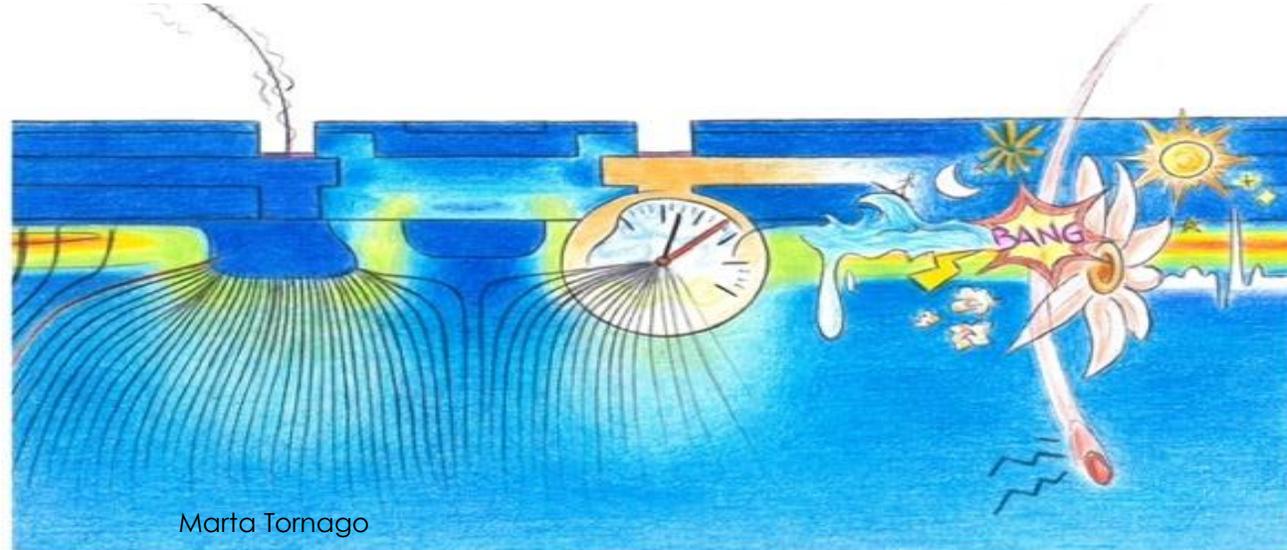


# Topics in LGAD design

- DC-RSD
- SEB-resistant (Single Event Burn-out) LGAD design



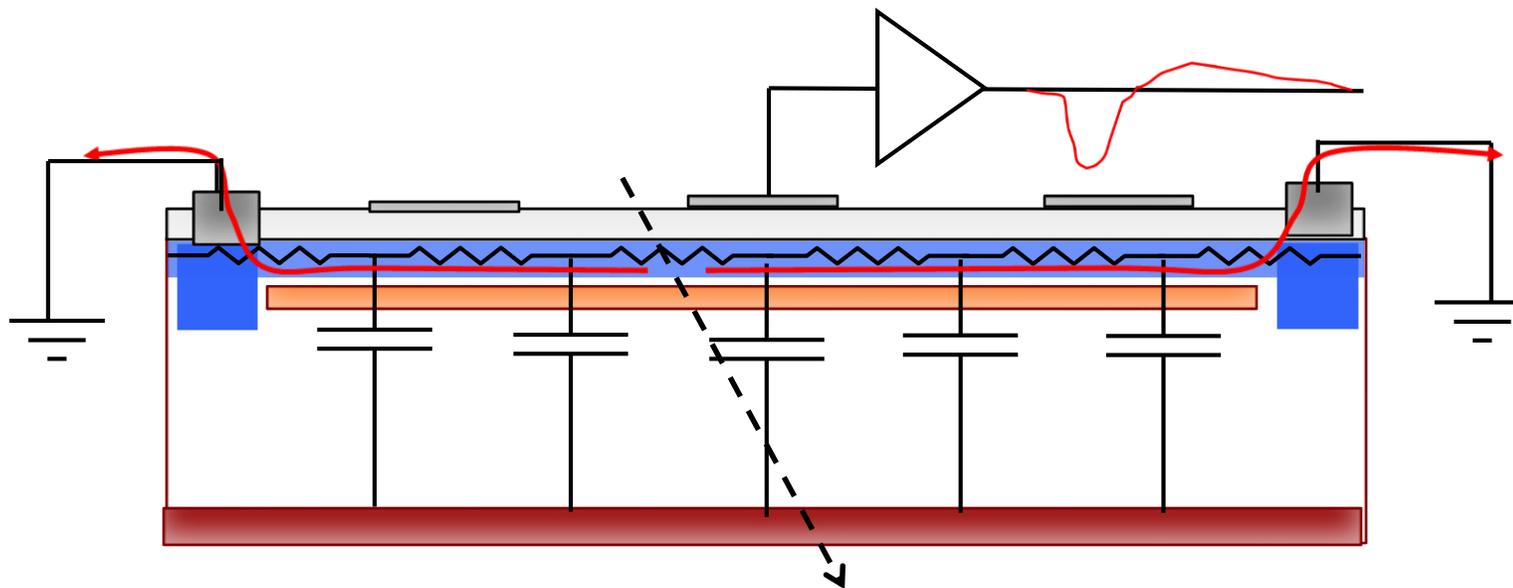
**N. Cartiglia**

4DInSiDe PRIN (INFN Torino & Genova, UniTo, UniPO, Univ. of Perugia, CNR-Perugia)  
FBK, Univ. of Trento, UCSC

# Part I: Resistive readout

In [1], the idea of resistive read-out has been introduced.

The realization exploited a resistive layer AC-coupled to the read-out pads



In this design, there is only 1 contact to the n<sup>++</sup>: the charges collected on the n<sup>++</sup> flow to the edge of the sensor.

[1] TREDI 2015

[https://indico.cern.ch/event/351695/contributions/828366/attachments/695875/955507/TREDI\\_Cartiglia.pdf](https://indico.cern.ch/event/351695/contributions/828366/attachments/695875/955507/TREDI_Cartiglia.pdf)

# AC-RSD

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## **AC-RSD have been proven to work quite well:**

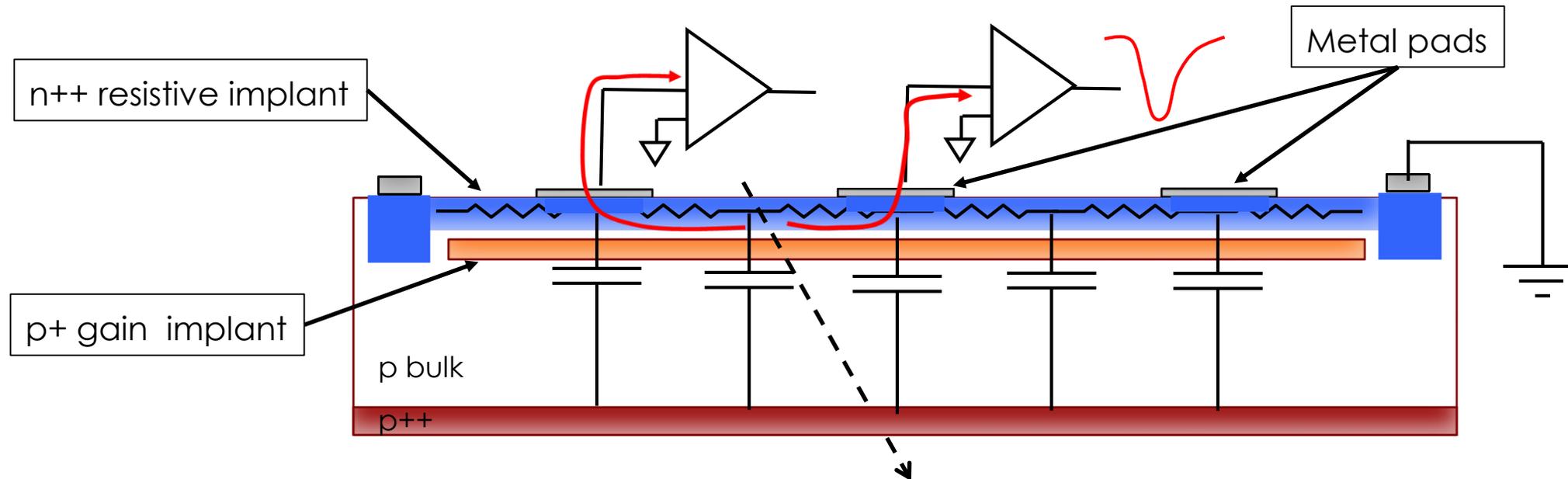
- Temporal resolution similar to the other “LGAD” designs
- Excellent position resolution using large pixels
- 100% fill factor

## **A few known problems with the AC-RSD design:**

- The signal is bipolar, with a long tail ( $\sim 100$  ns)
- The number of pads seeing a signal depends upon the hit position: it might be 3,4, 5, 6
  - Studies to minimize these effects are on-going, see FBK RSD2 production
- Normally, 3 or 4 pads collect most of the signal but several more pads see “something”
- The leakage current is collected at the edge of the sensor
- Not yet proven that AC-RSD can be made large, for example  $10 \times 10$  cm<sup>2</sup>

# Design evolution: DC-RSD

What would be the consequences of a DC read-out in resistive read-out ?



In this design, the charges collected on the n++ flow to the electronics as in standard sensors  
The read-out pads are embedded into a resistive n++ sheet that assures pad isolation

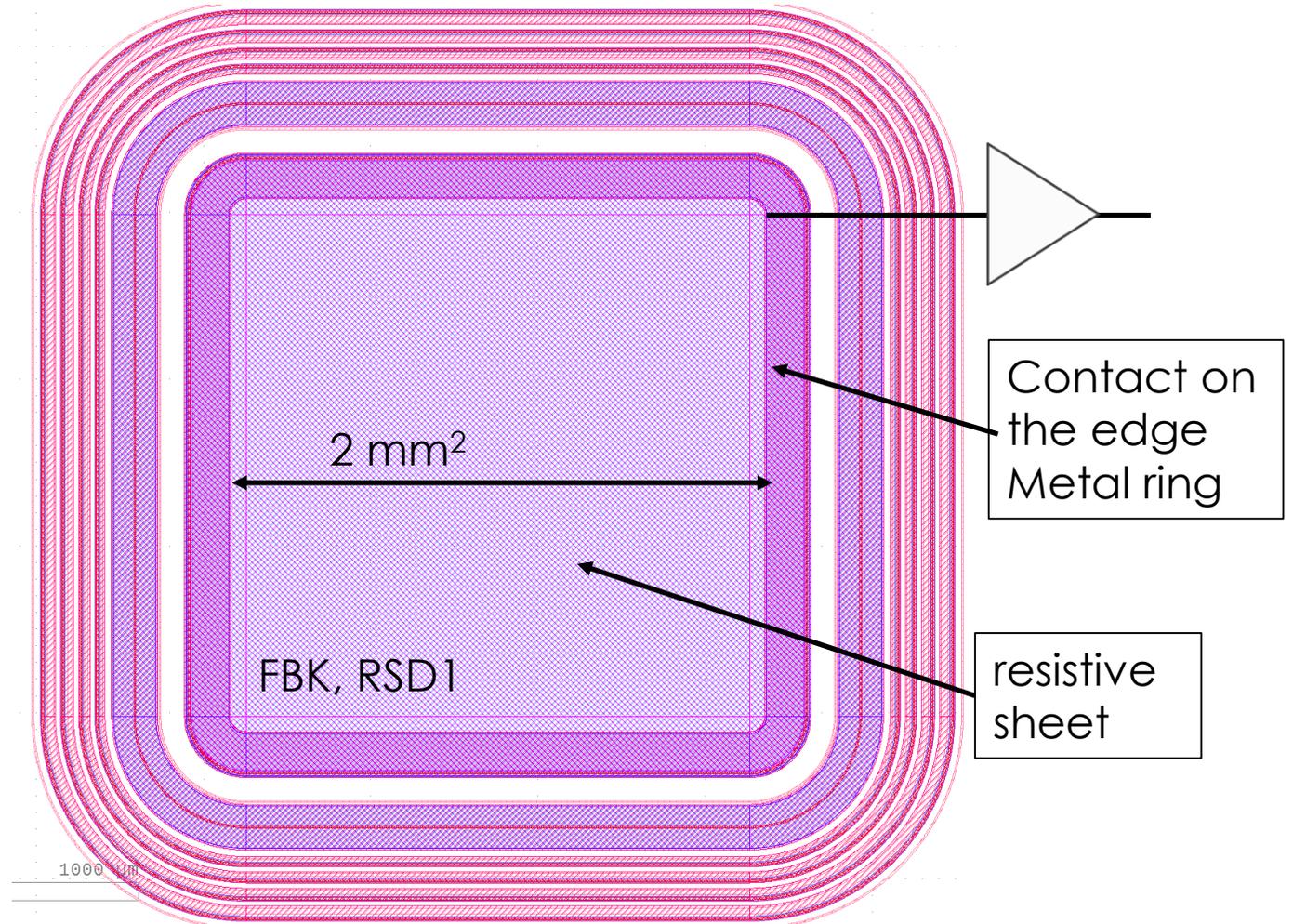
- Signal propagation on the n++ ?
- Signal sharing?

# Signal propagation on a resistive sheet

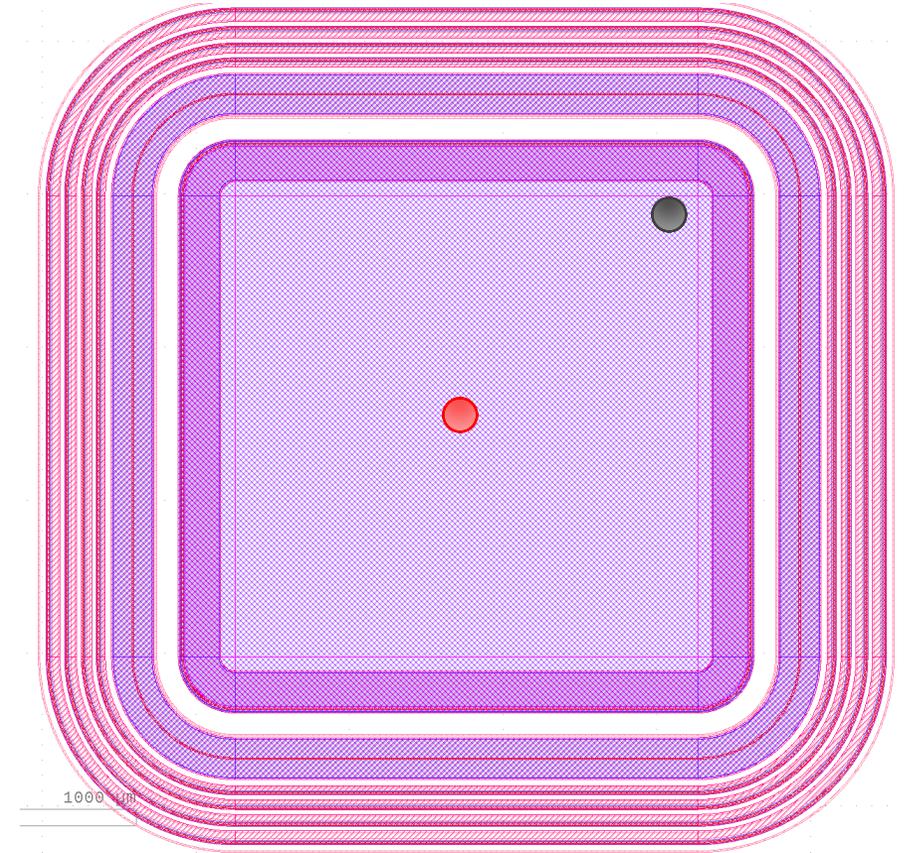
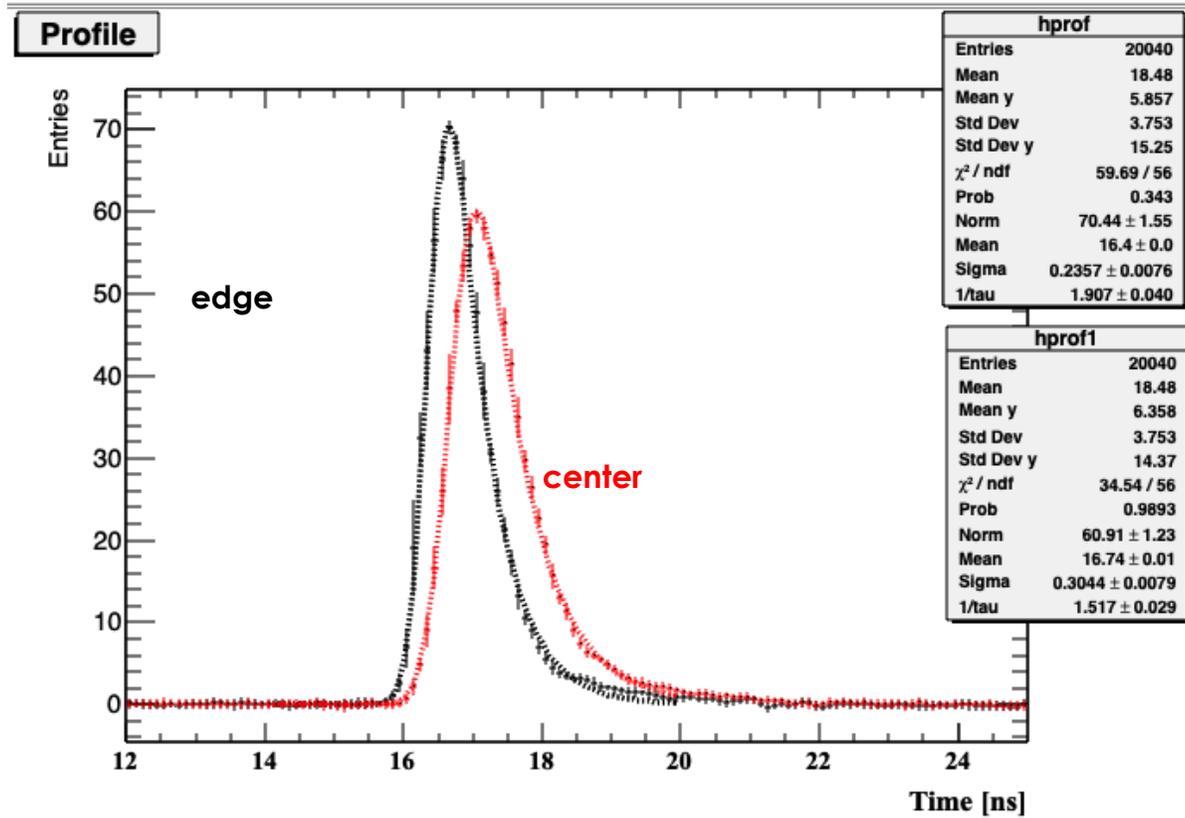
The first step is to understand how a signal spreads on a resistive sheet  
=> manufacture a resistive sheet and study signal propagation

In RSD1 production we have:

- single pads:  $2 \times 2 \text{ mm}^2$  resistive sheet
- Contact at the periphery to read-out of the  $n^{++}$
- Various doping levels of the resistive sheet

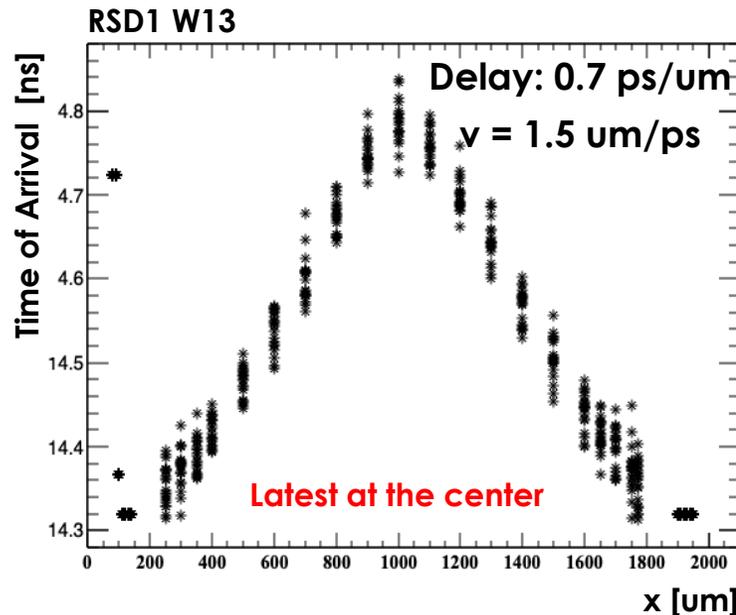
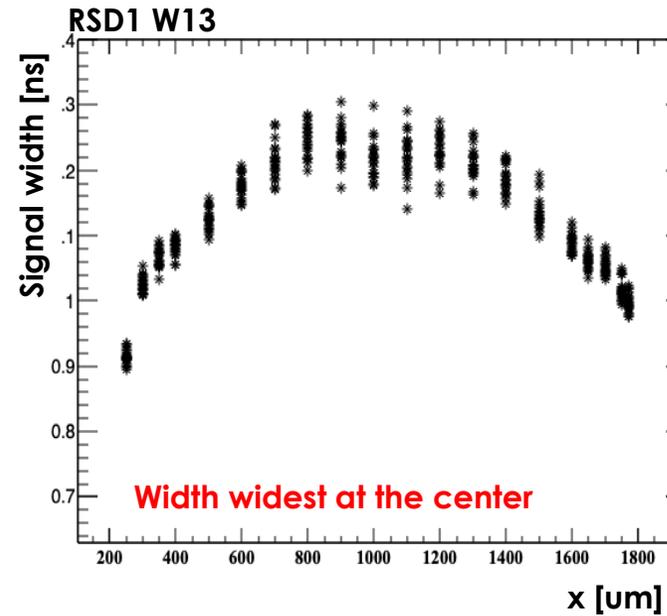
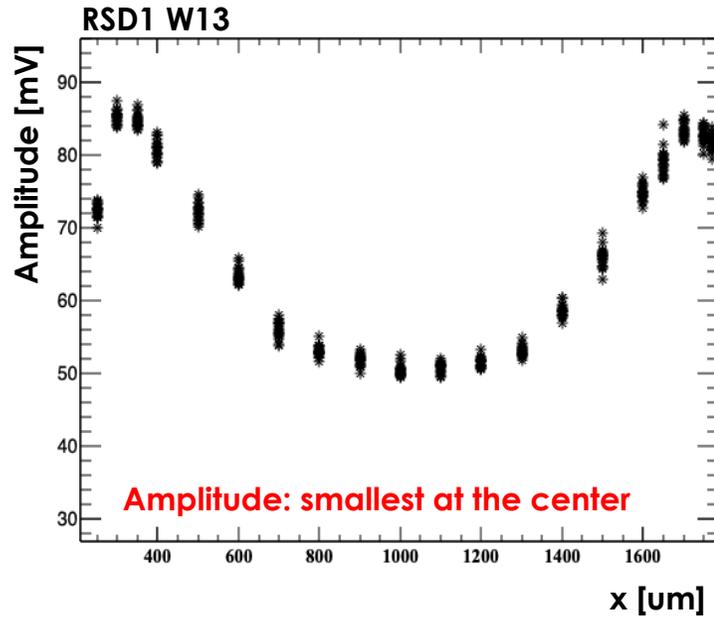


# Signal shape of hits near the edge or in the center



Even after a sizable distance,  $\sim 1$  mm, the rising edge is still quite sharp  
The signal shape is that of an exponentially modified gaussian

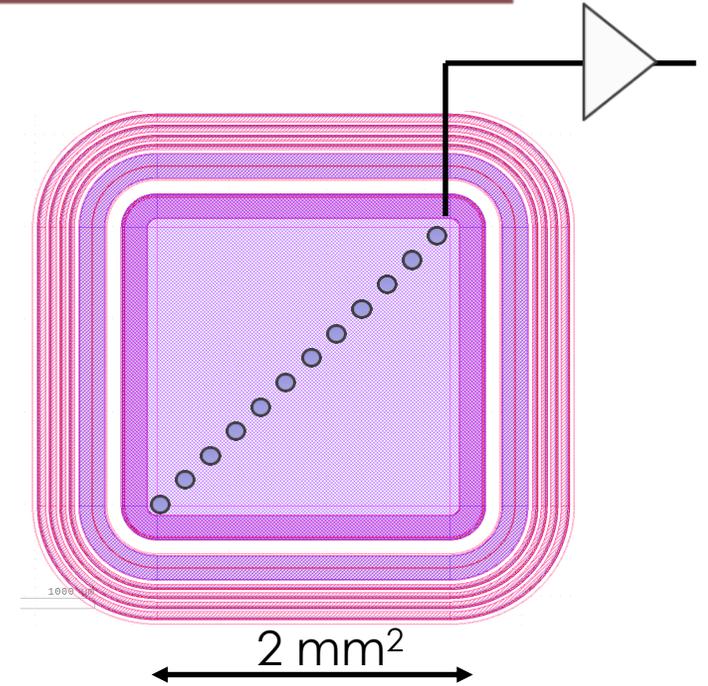
# Shooting along the diagonal and reading out the signal at the edge



At lower sheet resistivity:  
lower attenuation,  
faster propagation

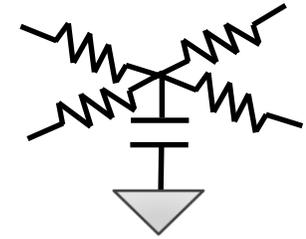
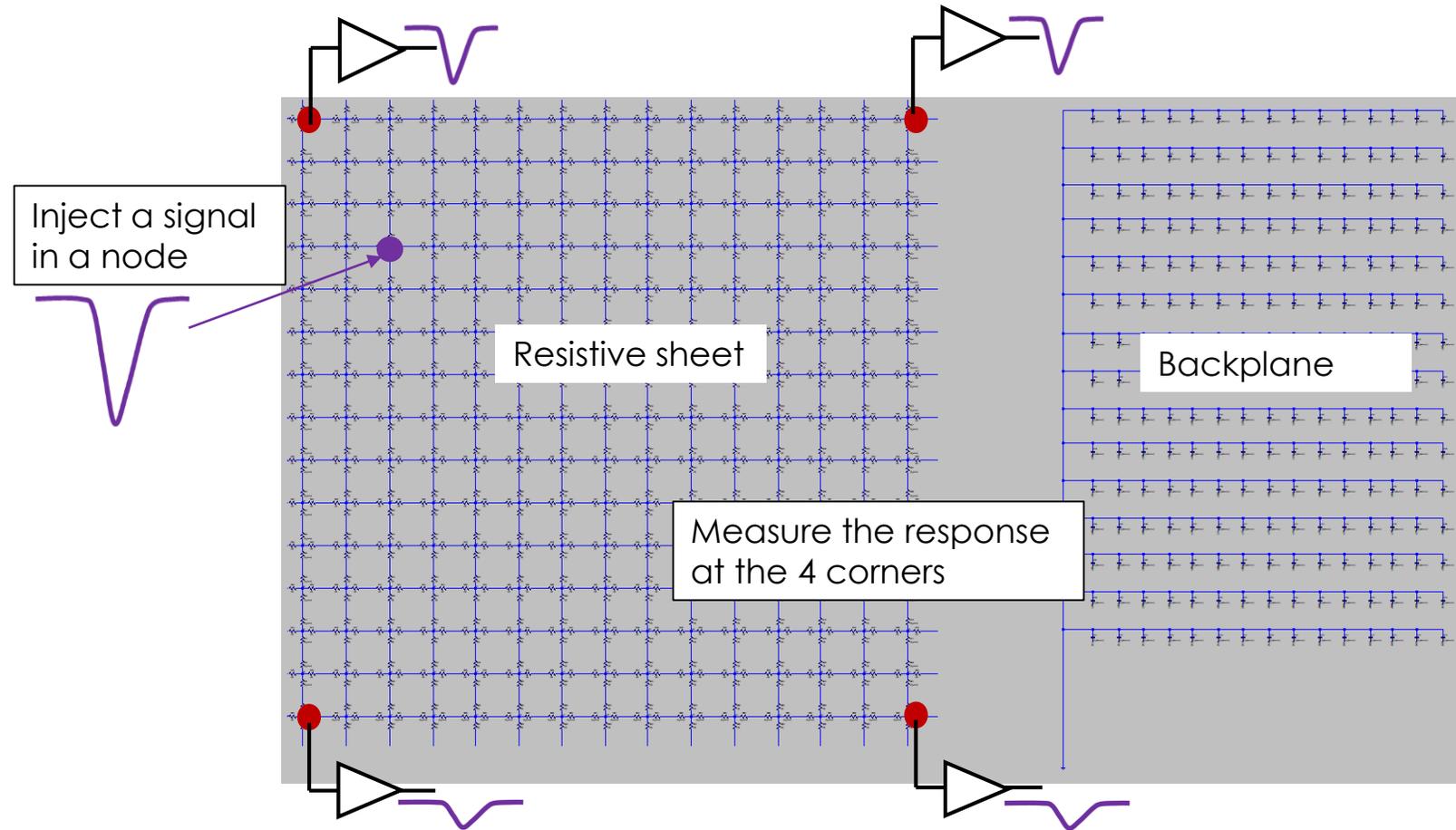
## Summary:

Propagation does not ruin the signal shape,  
the shape changes as expected: it becomes shorter and wider  
with distance



# DC-LGAD LTSpice simulation

The resistive sheet is simulated with a grid of resistors.  
The bulk as capacitors attached to each node [2].

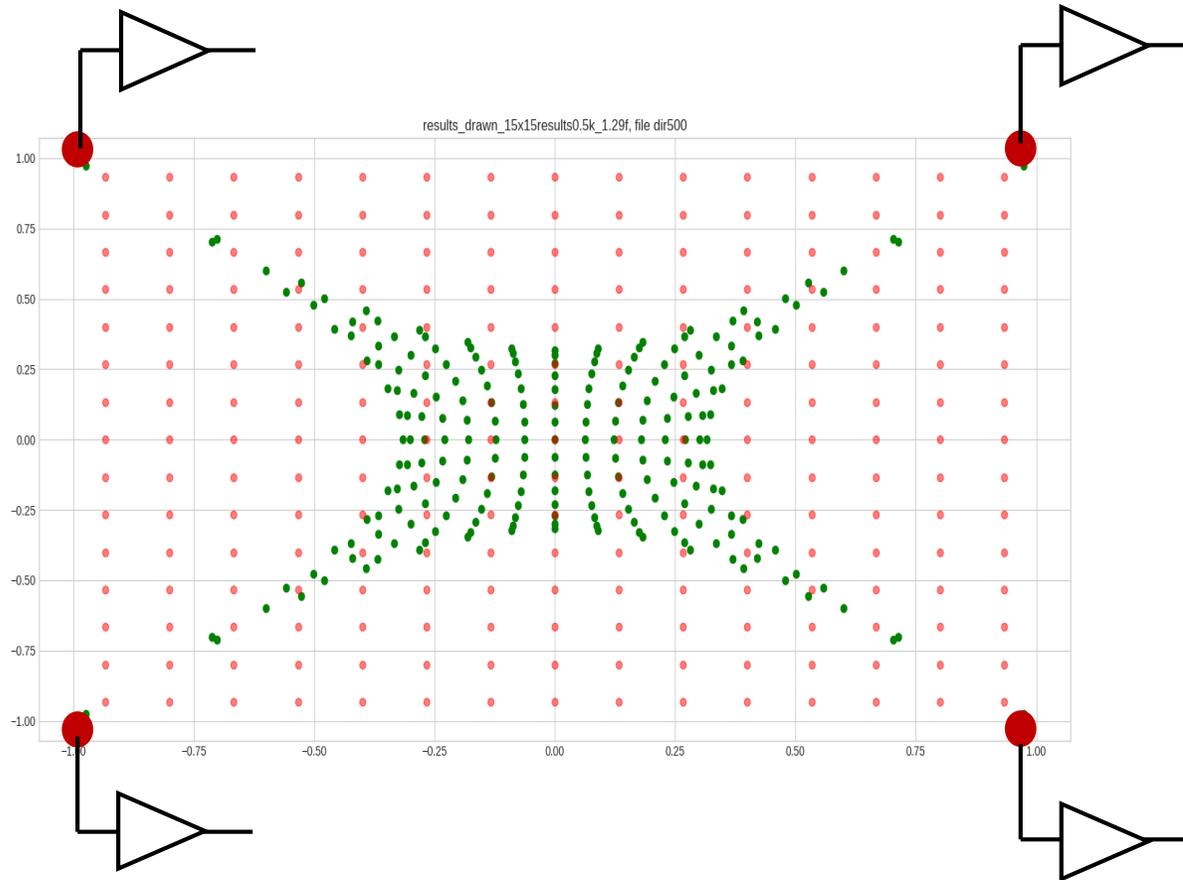


[2] For additional details on this study, ask the author, [luca.menzio@to.infn.it](mailto:luca.menzio@to.infn.it), more details soon

# Position reconstruction using charge imbalance

Simplest algorithms for position reconstruction:

$$x_i = \frac{Q_{top\ right} + Q_{bottom\ right} - Q_{top\ left} - Q_{bottom\ left}}{Q_{tot}}$$
$$y_i = \frac{Q_{top\ right} + Q_{top\ left} - Q_{bottom\ left} - Q_{bottom\ right}}{Q_{tot}}$$



Shoot in a grid of points, and see where the position is reconstructed:

**Red:** points where the signals are injected

**Green:** reconstructed points

**Very large distortion.**

This is a known problem in resistive read-out (for example, in grid of SiPM)

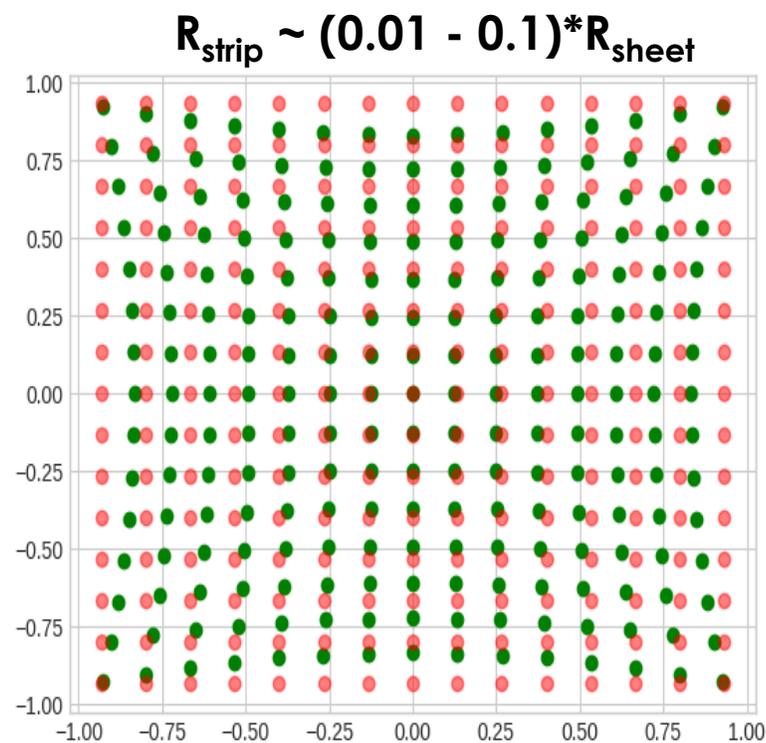
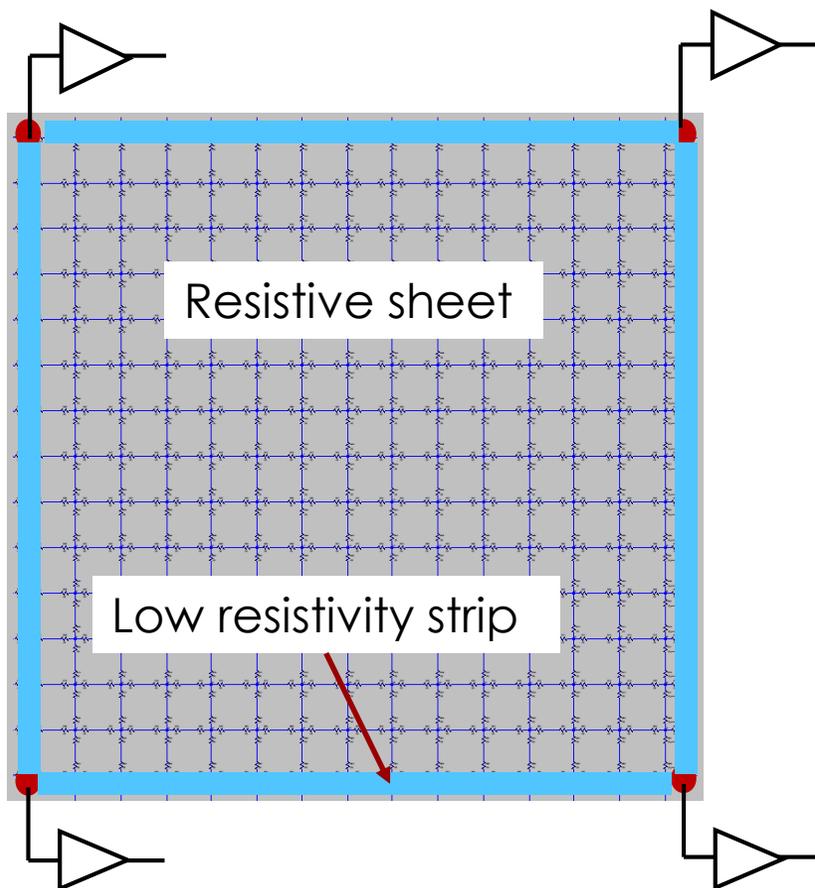
Often corrected using homography [3]

[3] Su-Jin Jeon et al, "Position error Correction Using Homography in discretized positioning circuit...", IEEE Vol 64 No.2 feb 2017

# Mitigation: add low resistivity strips between read-out points

There is a hardware solution [4][5] to this distortion: add a low-resistivity strip between each pair of points

Important benefit: in this design, **the signal is contained in a square**, firing always the 4 corners.



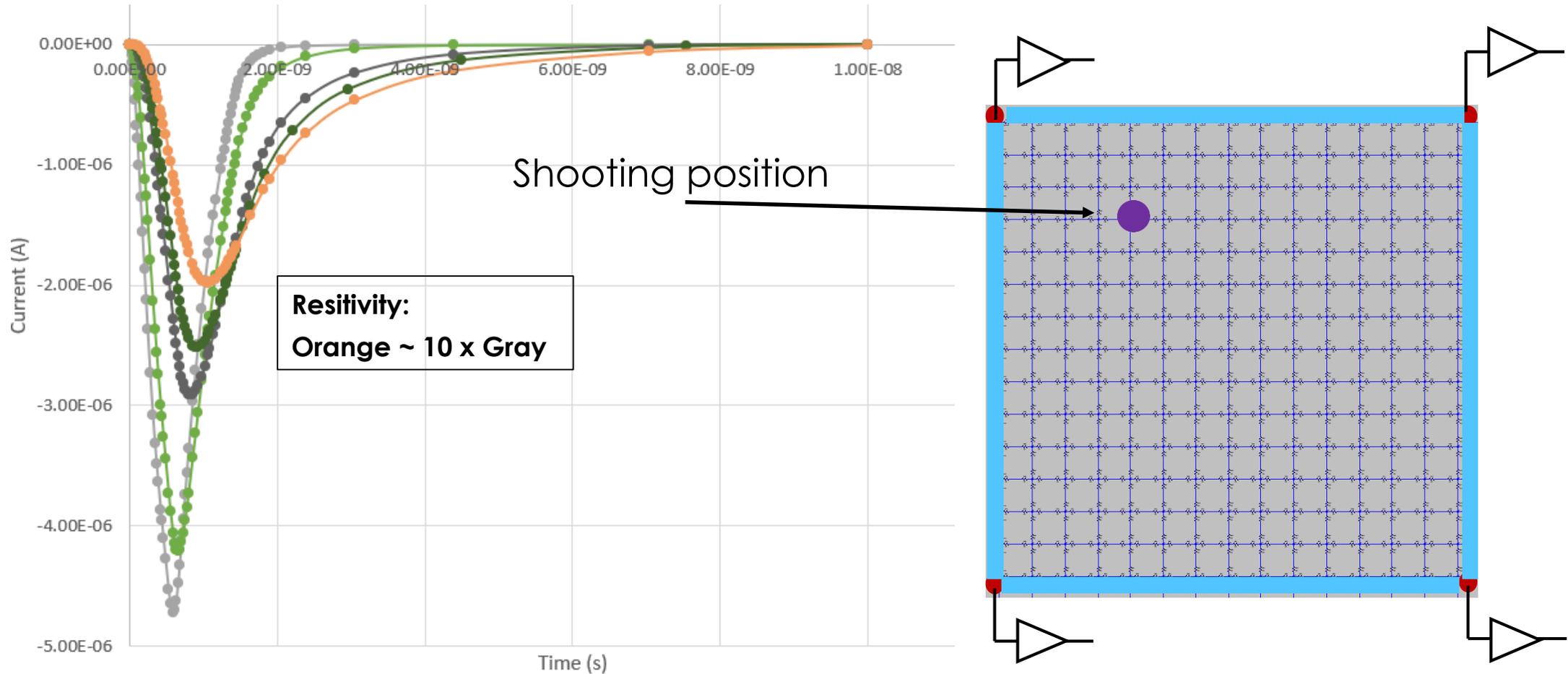
Red: points where the signals are injected

Green reconstructed points

[4] H. Wagner et al, *On the dynamic two-dimensional charge diffusion of the interpolating readout structure employed in the MicroCAT detector*, NIM A 482 (2002) 334–346.

[5] Many thanks to W. Riegler for pointing-out this paper to us

# Signal shape vs sheet resistivity

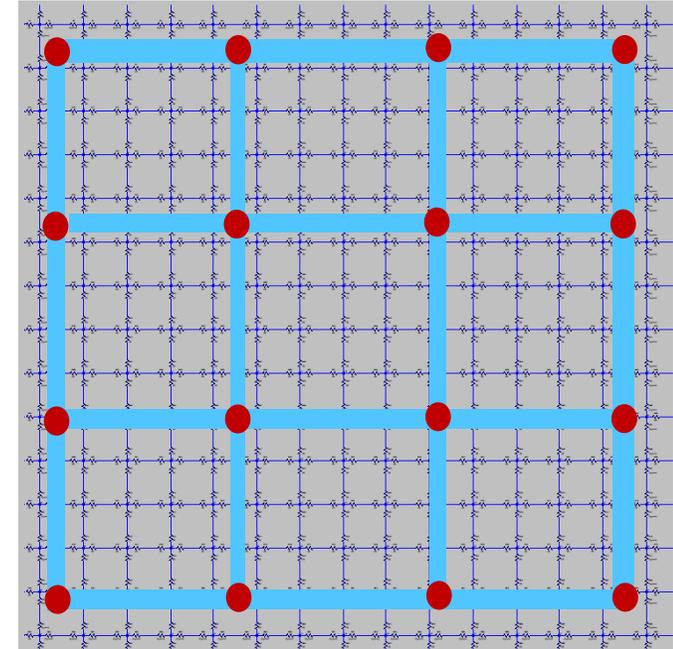
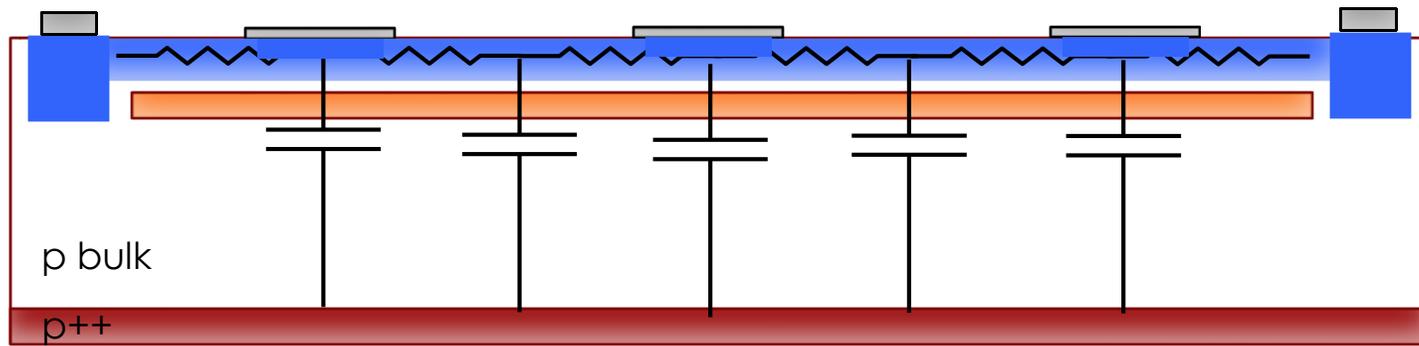


As the n++ resistivity increases, the simulation predicts shorter and wider signals

# Wrap-up DC-RSD

## DC-RSD:

- Use DC read-out on a resistive sheet
- Link the read-out pads with a lower resistivity strip



## Benefits:

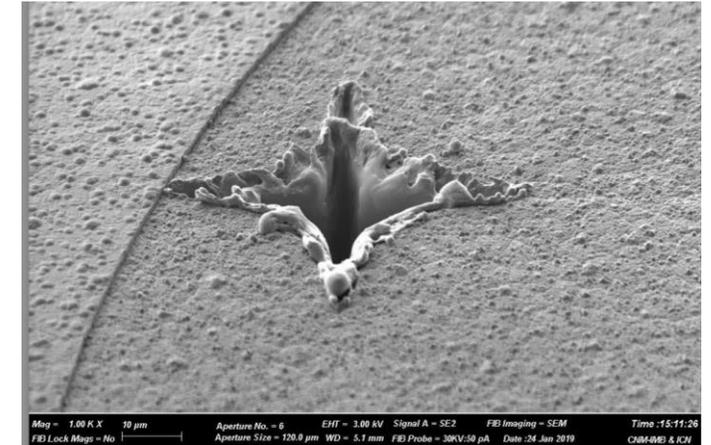
- Fast signal
- Large pixels (200-300  $\mu\text{m}$ ): still sharp rising edge even after a propagation of 1 mm.
- Excellent position resolution
- DC connection to the read-out
- Well-defined sharing among 4 pads

## Futures:

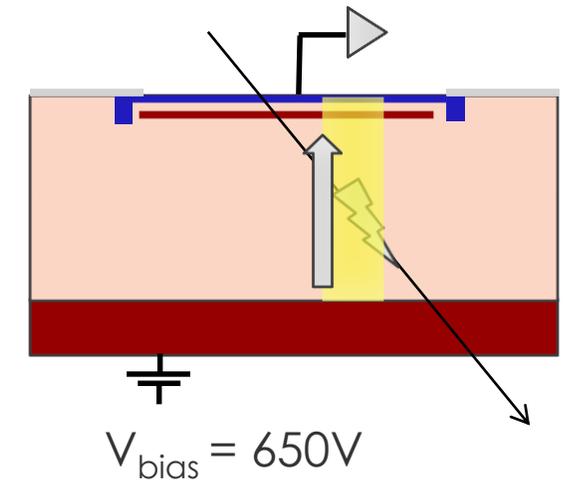
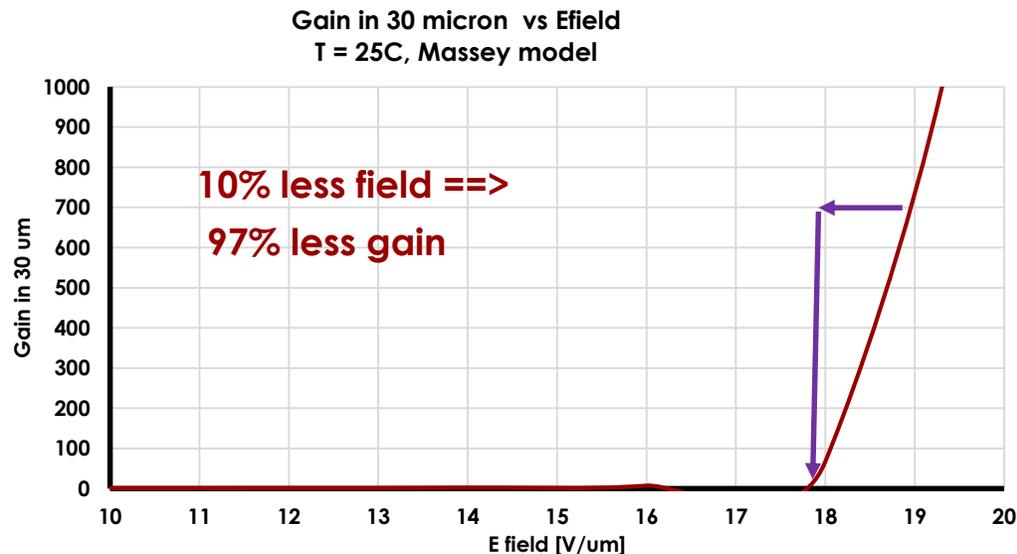
- Simulation studies on-going
- Detailed presentation soon (VCI, TREDI...)
- FBK production in 2022

# Part II: SEB-resistant LGAD design

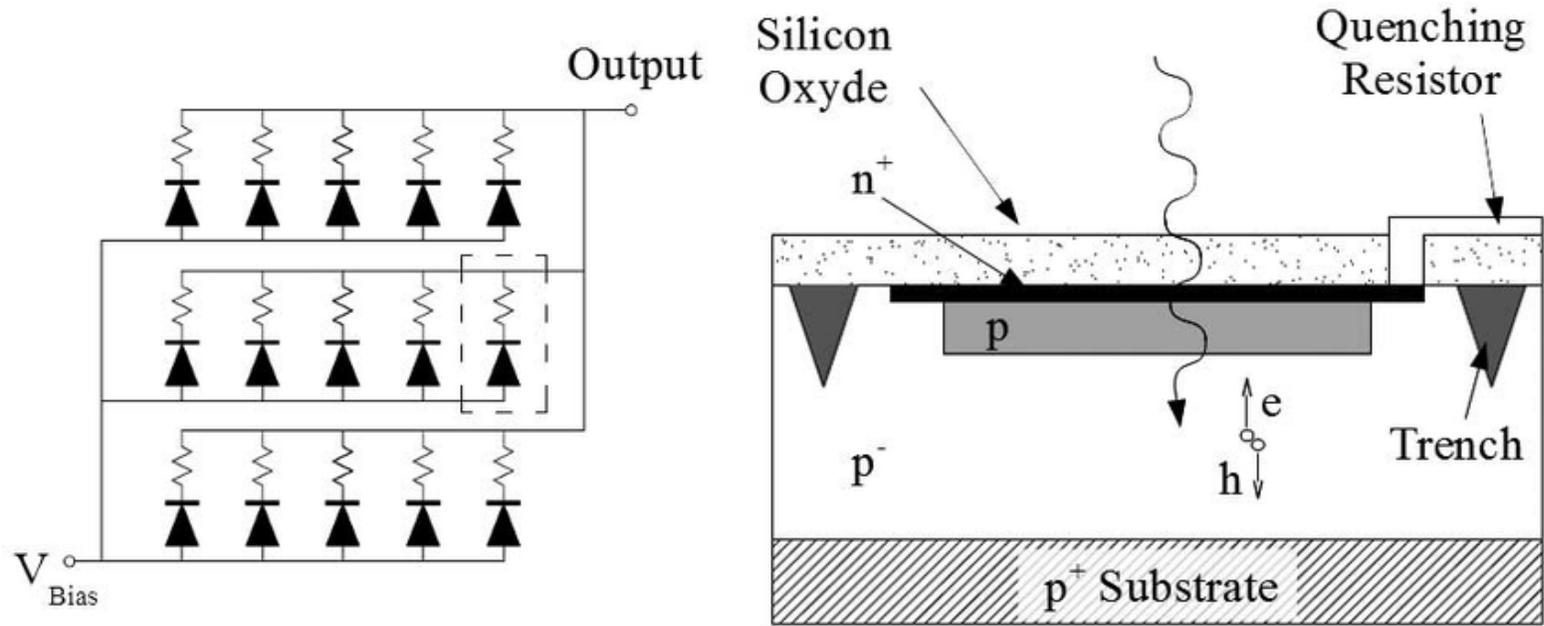
- **50  $\mu\text{m}$  thick LGAD** sensors exposed to 120 GeV/c protons, when biased at 625V or higher (**12.5V/ $\mu\text{m}$** ), break down permanently.
- **45  $\mu\text{m}$  thick LGAD** broke down at 550V (**12.2V/ $\mu\text{m}$** )
- 50  $\mu\text{m}$  thick LGAD sensors, biased at 575V or less (**11.5V/ $\mu\text{m}$** ), did not break.
- **55  $\mu\text{m}$  thick LGAD** survived many hours at 600V (**10.9V/ $\mu\text{m}$** ).



**Threshold effect: SEBs happen quickly if the Electric field is high enough**



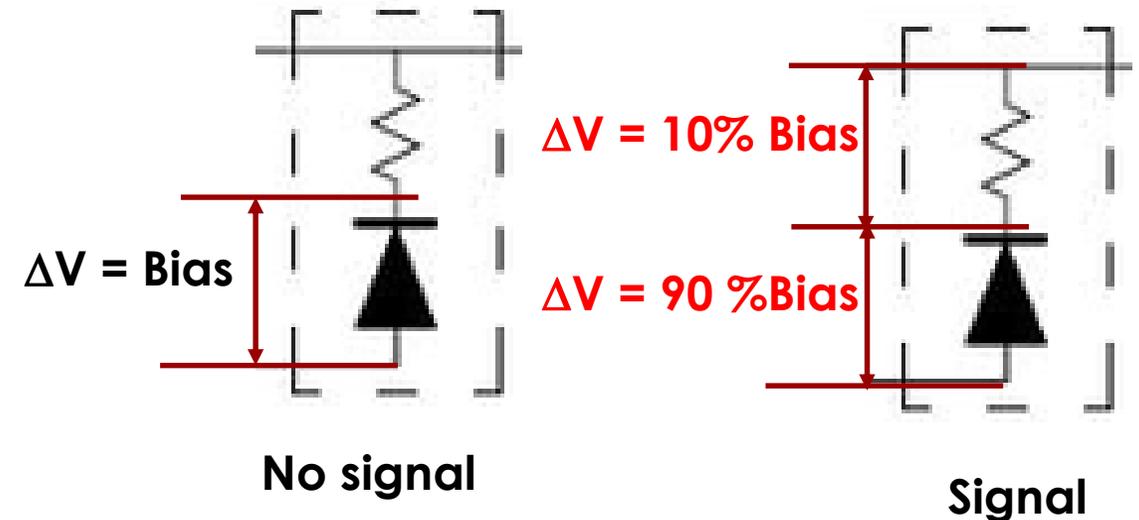
# SiPM: aide mémoire



SiPM: one single bias, working in avalanche mode

## SiPMs do not burnout. Why?

- 1) A SiPM goes into avalanche
- 2) A large current flows
- 3) A fraction of  $\Delta V$  shifts from the capacitor to the resistor,  $\Delta V = V_{bias} - V_{BD}$
- 4) The voltage on the silicon bulk drops,
- 5) The avalanche is quenched
- 6) The capacitor does not discharge,  $\Delta V$  is preserved



# SEB-resistant LGAD design

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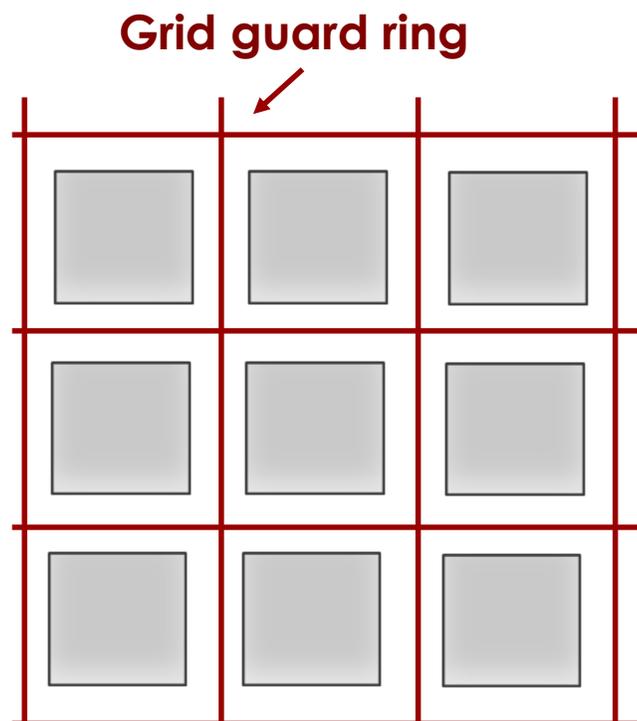
Can we add a quenching resistor in LGAD?

What are the consequences?

- **Where do we connect the resistors to ground?**
- **Do we spoil the signal shape?**
- **Do we increase dramatically the fill factor?**
- **How do we do this study?**

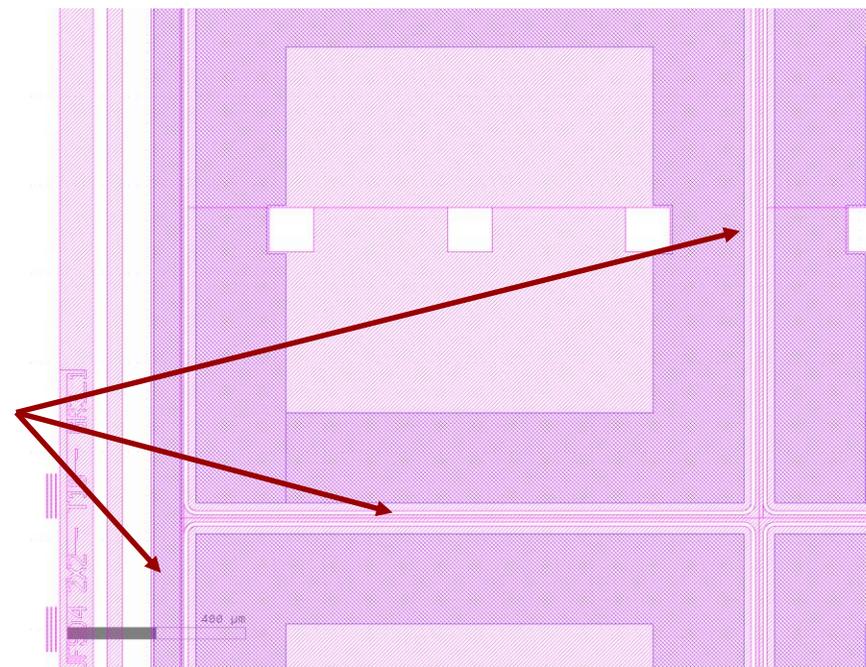
# LGAD matrix with grid guard-ring

Independently from the SEB issue, FBK has developed LGAD matrices with a grid guard-ring, i.e., there is a ground grid among the pads (the so-called FBK UFSD Type10)



No-gain region ~ 70  $\mu\text{m}$

Grid guard ring



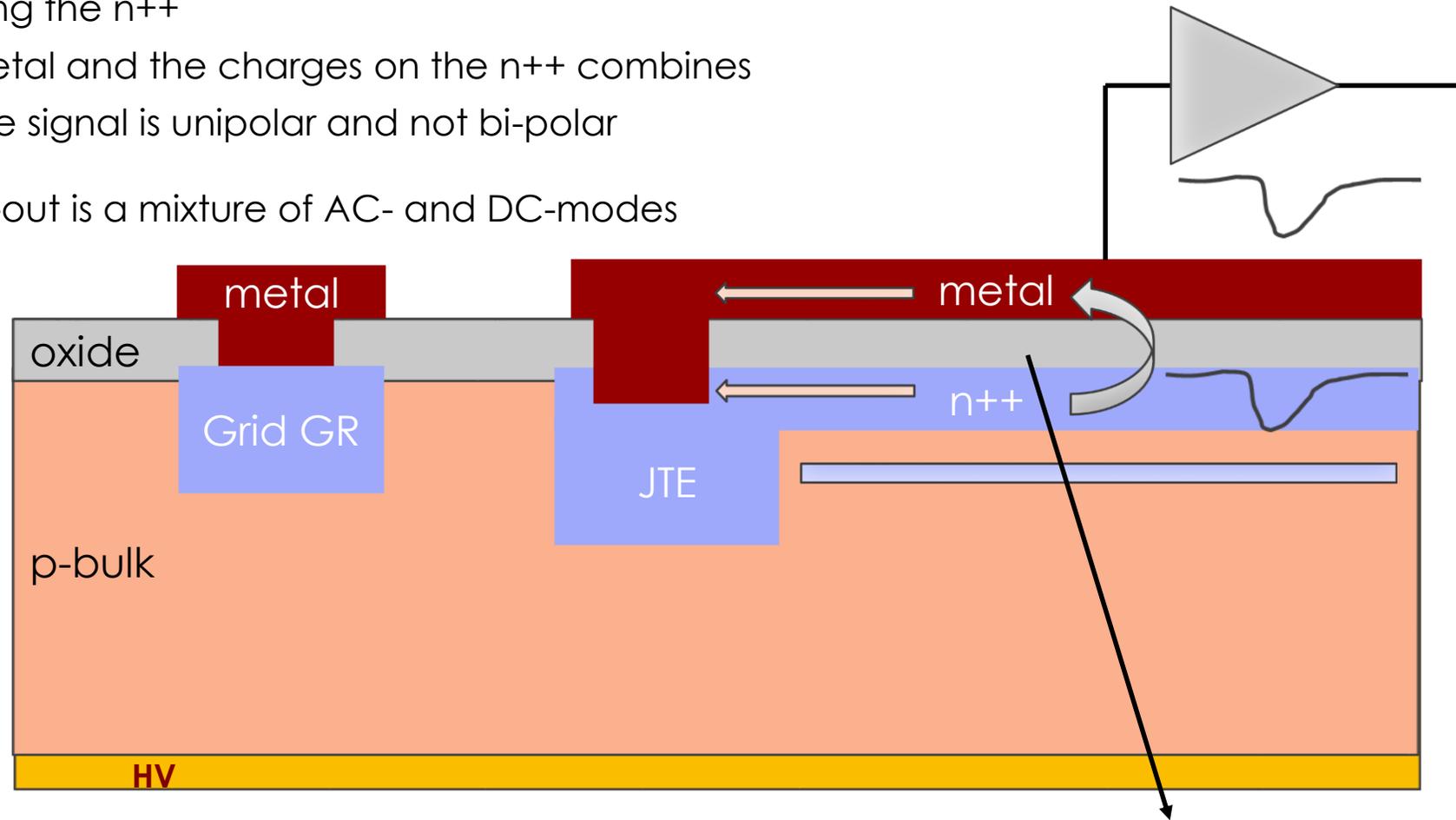
We have a design where each pad has a near-by ground. Can we use it?

# LGAD: aide mémoire

## Signal formation:

- The signal is formed on the n++
- It is AC-coupled to the metal
  - ==> that is why the timing is not "position dependent" as it is in "not metallized" LGADs.
- Charges travels along the n++
- The signal on the metal and the charges on the n++ combines
  - ==> that is why the signal is unipolar and not bi-polar

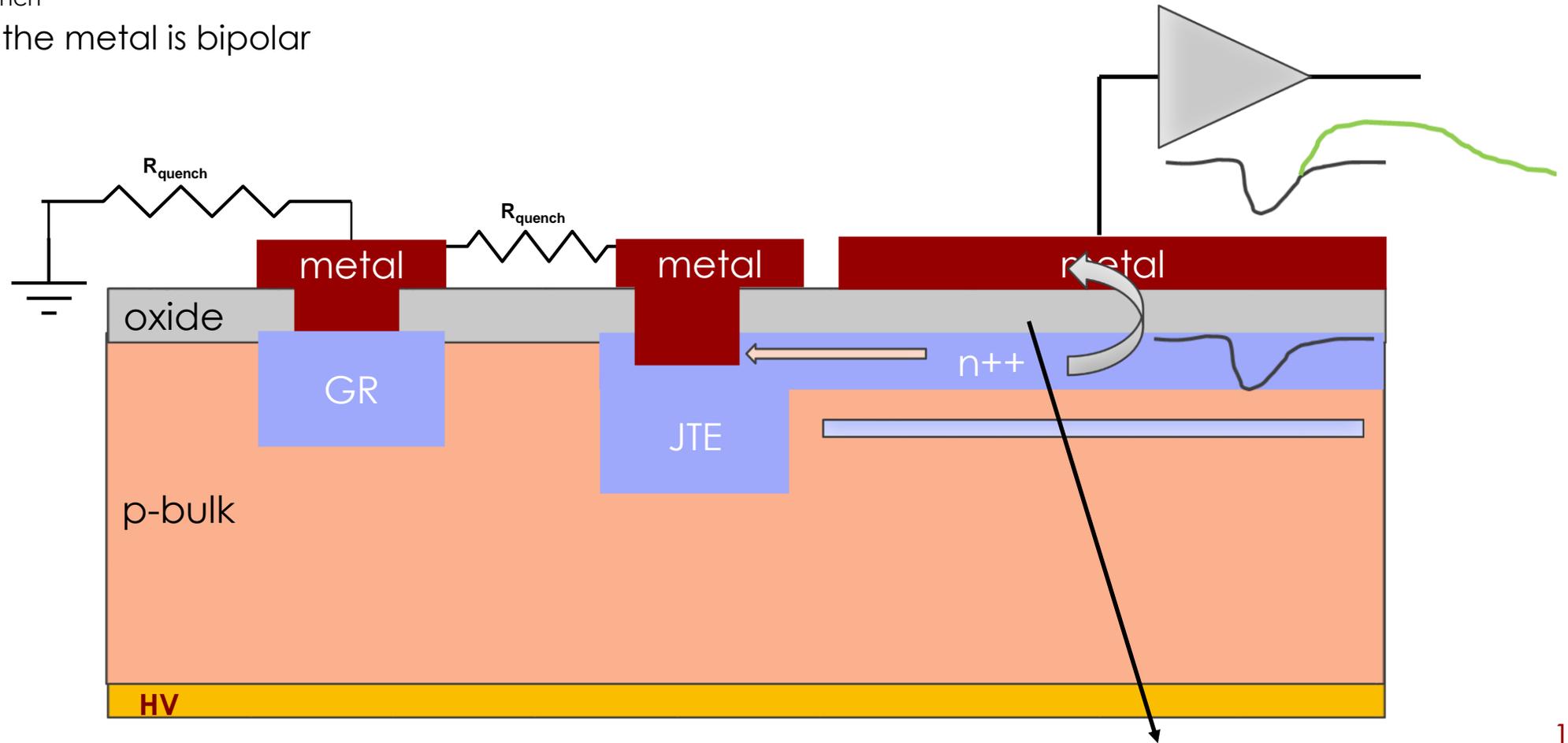
Oddly, the LGAD read-out is a mixture of AC- and DC-modes



# LGAD with quench resistor

## Let's imagine a new design:

- The signal is formed on the n++ and it is AC-coupled to the metal
- Charges travels along the n++
- Goes via  $R_{\text{quench}}$
- The signal on the metal is bipolar



# Note: every diode needs to have a resistor

Beam-tests demonstrated that not only the pads but also the guardrings are suffering from SEB

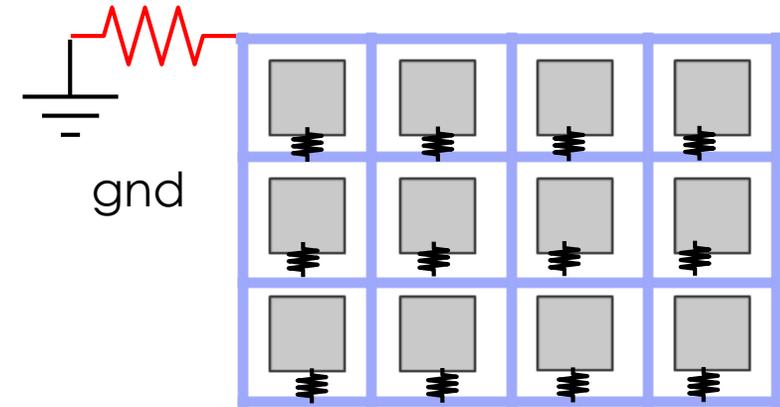
Resistors need to be placed in:

- 1) Pads to grid guard-ring  
(necessary for AC read-out and pad isolation)
- 2) Grid guard-ring to gnd
- 3) Your ideas here....

$R_{\text{quench}}$  needs to:

- Limit the current in case of a quench
- Be high resistive to limit the signal loss
- Small enough for a fast recovery  $\tau = RC$
- Generate enough  $\Delta V$  to quench the avalanche

**Position of  $R_{\text{quench}}$** : the closer to the diode, the smaller the amount of charge flowing  $Q = \Delta V * C_{\text{total}}$



## Example:

- $R_{\text{quench}} = 100 \text{ k}\Omega$
- $\Delta V = V_{\text{bias}} - V_{\text{breakdown}} \sim 100 \text{ V}$
- Max current =  $100 \text{ V} / 100 \text{ k}\Omega \sim 1 \text{ mA}$

Performances:

- Signal loss minimal  $\sim 50 \text{ }\Omega / 100 \text{ k}\Omega$
- $RC = 100 \text{ k}\Omega * 5 \text{ pF} = 500 \text{ ns}$

# Wrap-up SEB-resistant LGAD design

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Can we add a quenching resistor in LGAD?

What are the consequences?

- **Where do we connect the resistors to ground?**
  - To the grid guard-ring and at the periphery of the grid
- **Do we spoil the signal shape?**
  - The fast part won't change, it will not affect the timing performance
- **Do we increase dramatically the fill factor?**
  - Probably it won't change with respect of UFSD Type10 (~ 70 micron no-gain distance)
- **How do we do this study?**
  - FBK will propose an RD50 project in the near future

# Acknowledgements

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We kindly acknowledge the following funding agencies, collaborations:

- ▷ RD50, CERN
- ▷ MIUR, Dipartimenti di Eccellenza (ex L. 232/2016, art. 1, cc. 314, 337)
- ▷ Ministero della Ricerca, Italia, PRIN 2017, progetto 2017L2XKTJ – 4DinSiDe
- ▷ Ministero della Ricerca, Italia, FARE, R165xr8frt\_fare
- ▷ INFN CSN5