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Guard-ring optimisation for sensors in LFoundry 150nm CMOS technology for the RD50-MPW3 submission

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In high energy physics, the silicon pixel sensors manufactured in commercial CMOS chip fabrication lines have been proven to have a good radiation hardness and spatial resolution. Along with the mature manufacturing techniques and the potential of large throughput provided by the foundries, the so called "passive CMOS" sensor has become an interesting alternative to standard planer sensors.
High and predictable breakdown behaviour is a major design goal for sensors and the guard-ring structure is one factor to optimise. This is especially important for the applications that require higher voltages.

We present a concept of the guard-ring design which can be realised in the LFoundry 150nm CMOS technology. Indicated by TCAD simulations, such design can lead to a higher breakdown voltage by modifying the potential and electric field distribution in the guard-ring area. A number of test-structures have been designed for the RD50-MPW3 submission for verifications and further studies.

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