The Silicon Electron Multiplier

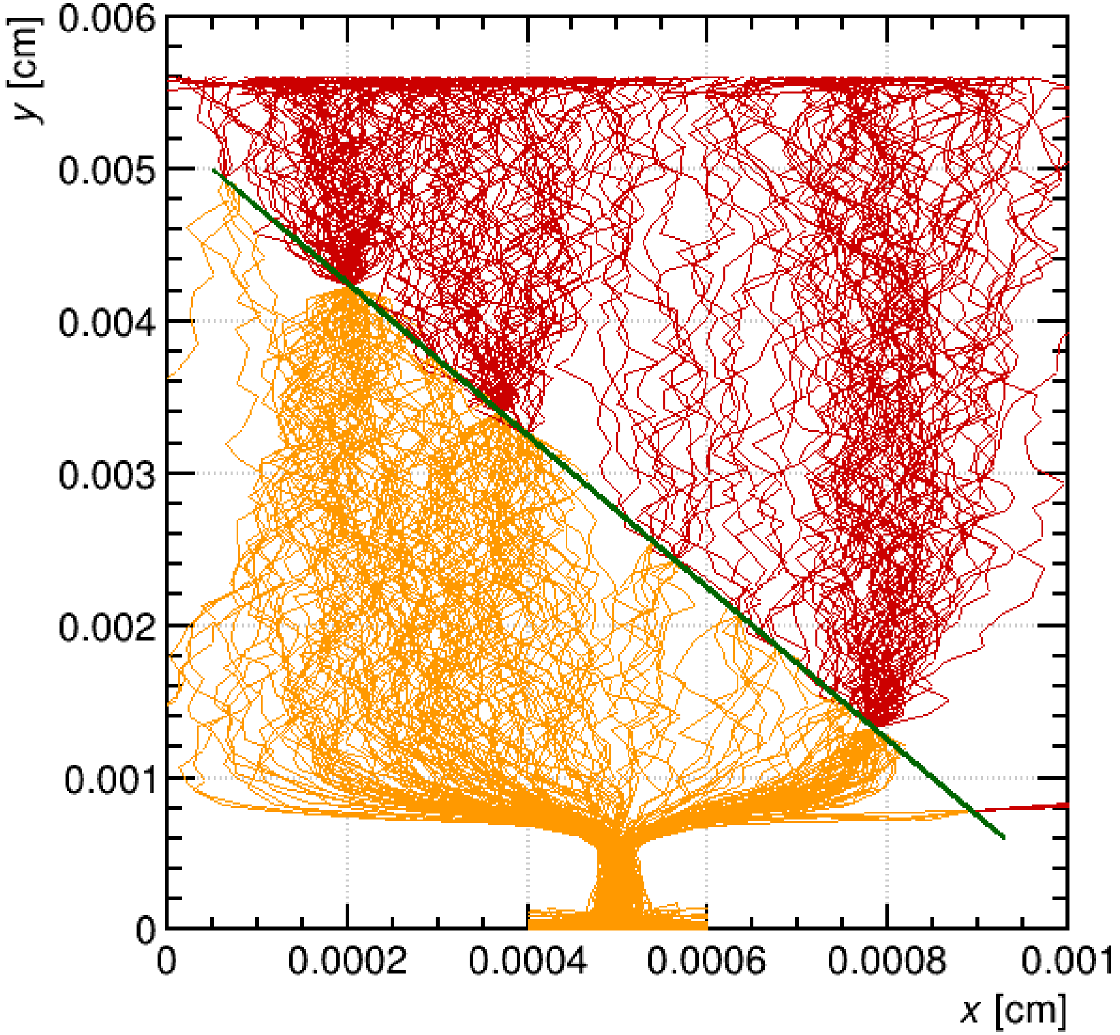
Victor Coco[1], Vagelis Gkougkousis[1], Marius Mæhlum Halvorsen[1,2]

The 39th RD50, Valencia, November 19th 2021

[1]CERN, [2]University of Oslo

Overview

- Motivation, framework and introduction
- Working principles
- Plans of fabrication
- Outlook



Motivation

from the CERN Strategic R&D Programme on Technologies for Future Experiments [CERN-OPEN-2018-006]

[fineprint in CERN-OPEN-2018-006]	HL-LHC	SPS	FCC-ee	FCC-hh
Fluence [$n_{eq}/cm^2/y$]	5×10^{16}	10^{17}	10^{10}	10^{17}
Max Hit rate [$cm^{-2}\ s^{-1}$]	2-4G	8G	20M	20G
Material budget per layer [X_0]	0.1-2%	2%	0.3%	1%
Pixel size [μm^2] inner trackers	50x50	50x50	25x25	25x25
Temporal hit resolution [ps] inner trackers	~50	~40	-	~10

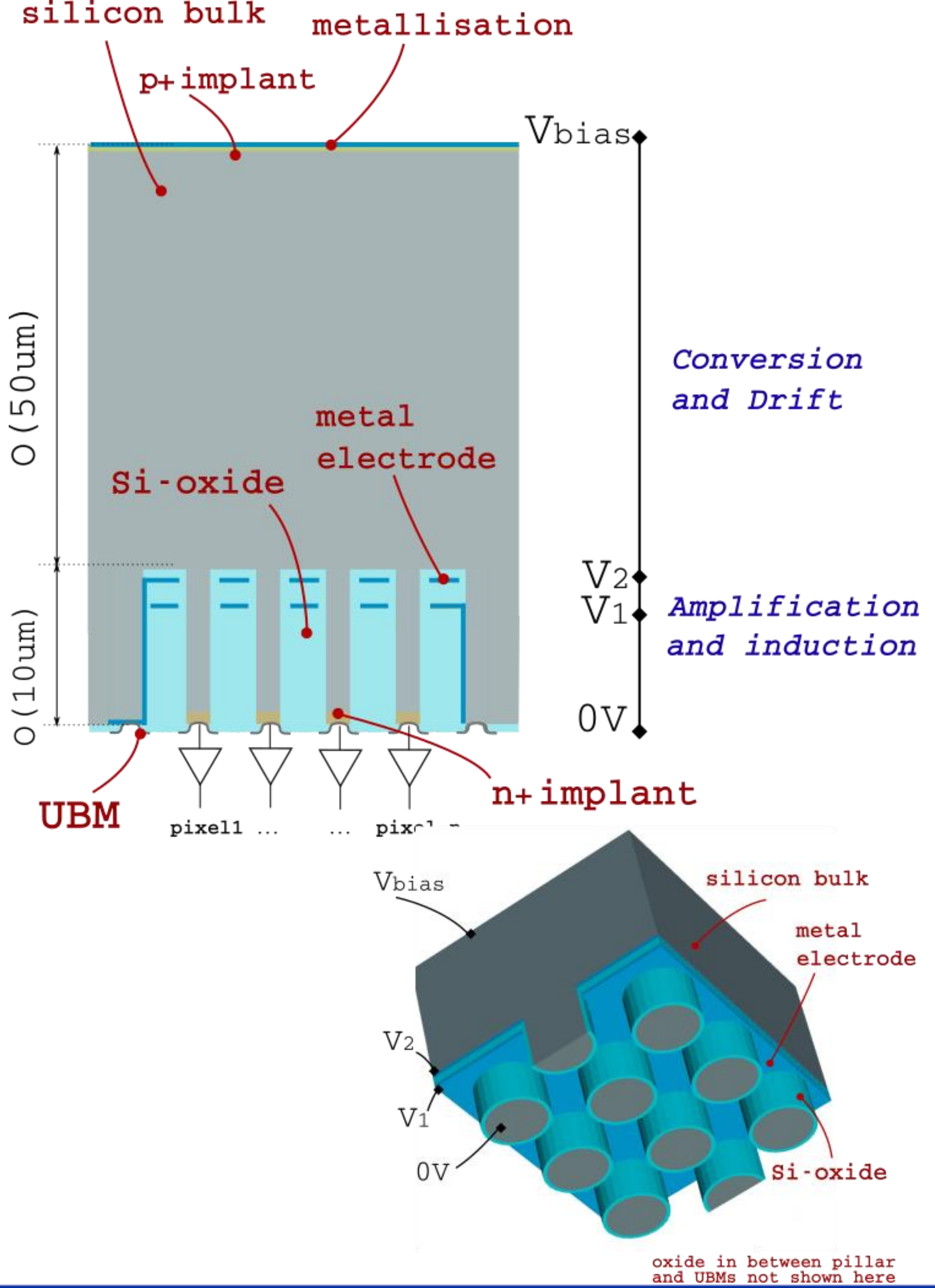
- Future inner tracker detectors will requite
  - Time resolution between 10 and 50ps
  - Pixel pitch down to 25µm
  - Radiation hardness up to $10^{17}n_{eq}$

Our approach

- Gain
- Small thickness, doping independent gain

Motivation

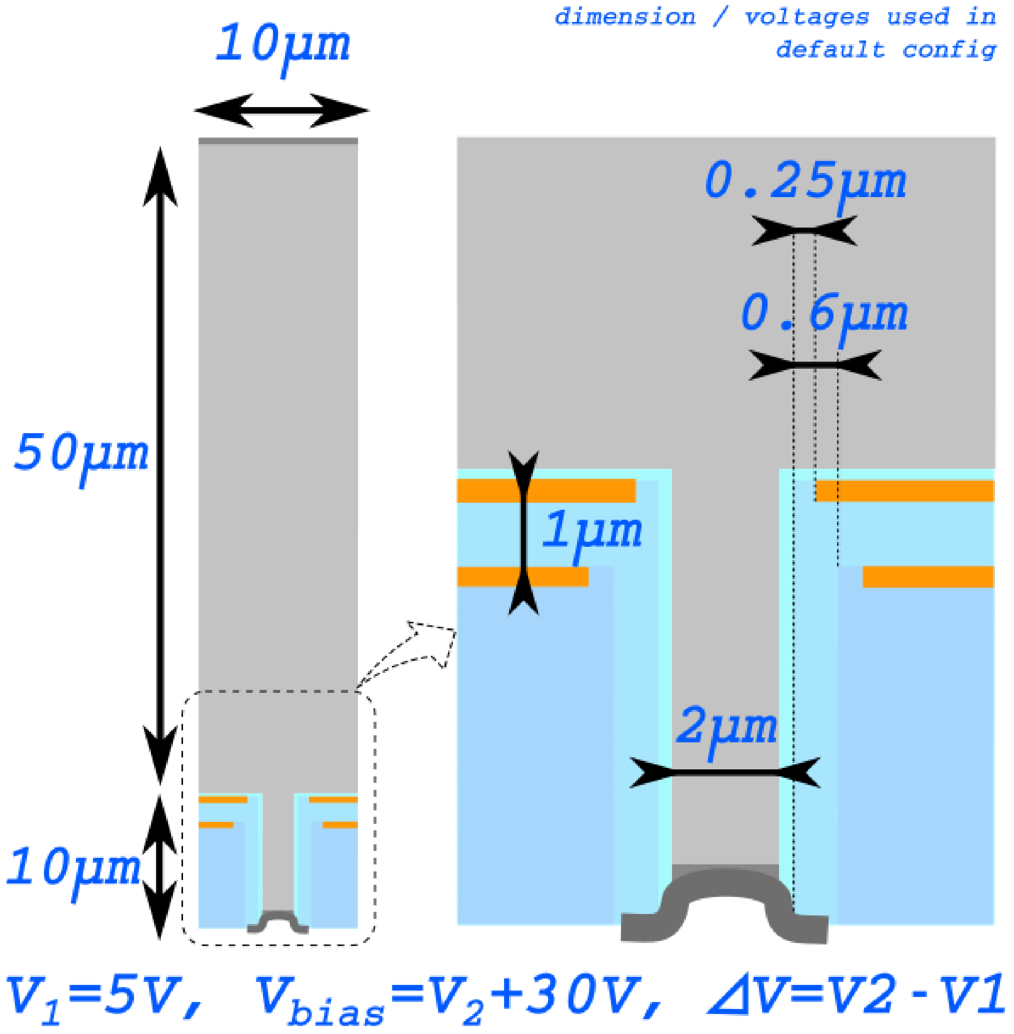
- Make a radiation hard sensor with internal gain
  - Avoid doping dependent gain regions'
- Idea: Generate high electric field regions by applying a potential difference to a set of electrodes
- Inversely etch (or grow) pillar structures
  - Silicon, diamond, SiC …
  - One or more layer of electrode grids
- Electrons drifting in the "amplification and induction" region multiply and enhance the signal



Geometry

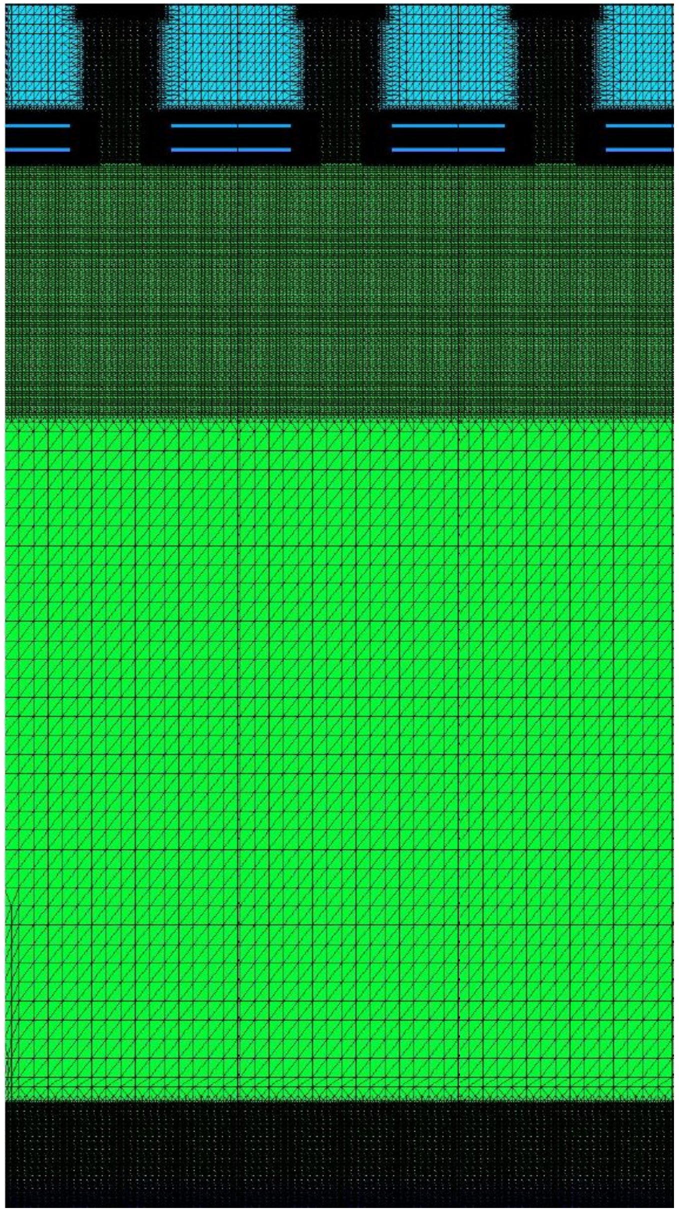
- First consider DRIE process
  - Etching of pillars and consecutive deposition of metal and oxide
- Process related constraints:
  - Guard and height of pillar
  - Sufficient guard around pillars to not get metal on pillar walls
- Impact on geometry
  - Pillar height 4-15μm,
  - Pillar width 1-4μm
  - Inter pillar distance more than 6μm

- Other fabrication techniques have different geometrical constraints

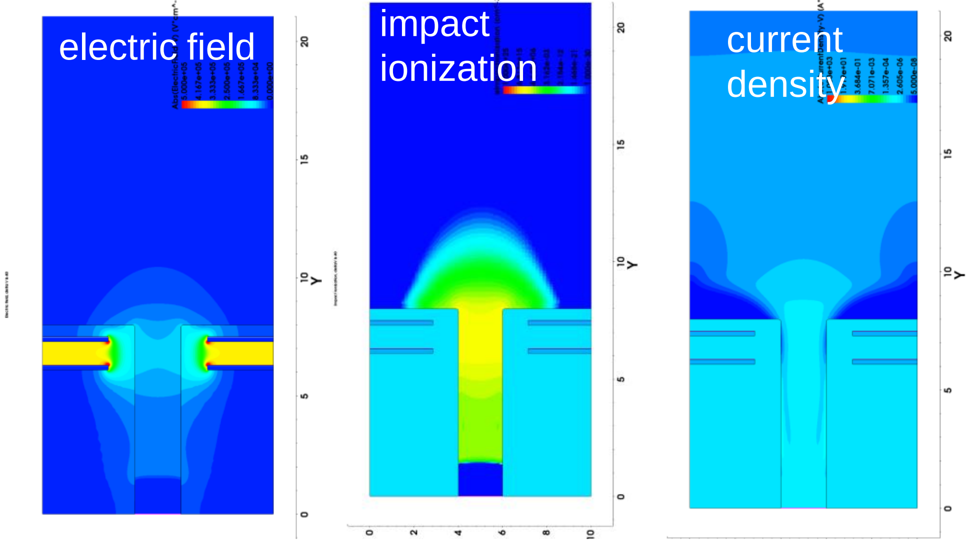


Synopsys TCAD simulations

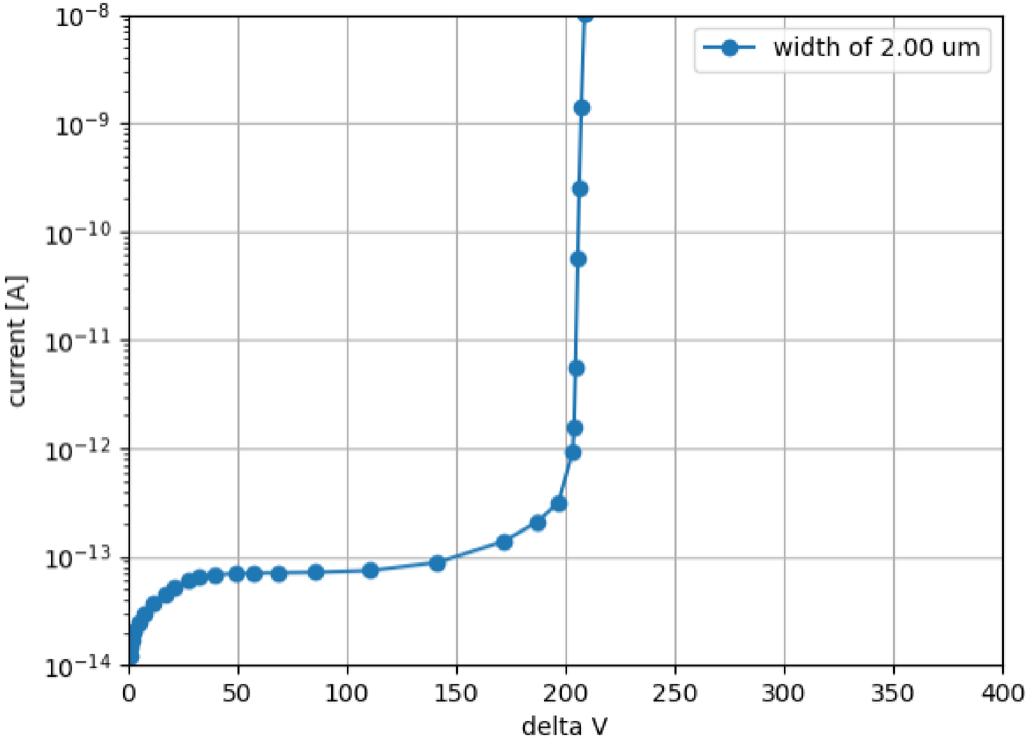
- Synopsys TCAD
  - Version Q-2019.12
  - Version Q-2021.06
- Impact ionization model: vanOverstraeten
  - Tested university of Bologna model
- Mobility model: Canali
- Solver: PARDISO
- Recombination: Shockley-Read-Hall
- Transient model: HeavyIon
- Band gap model: Slotboom



Quasi-stationary simulations

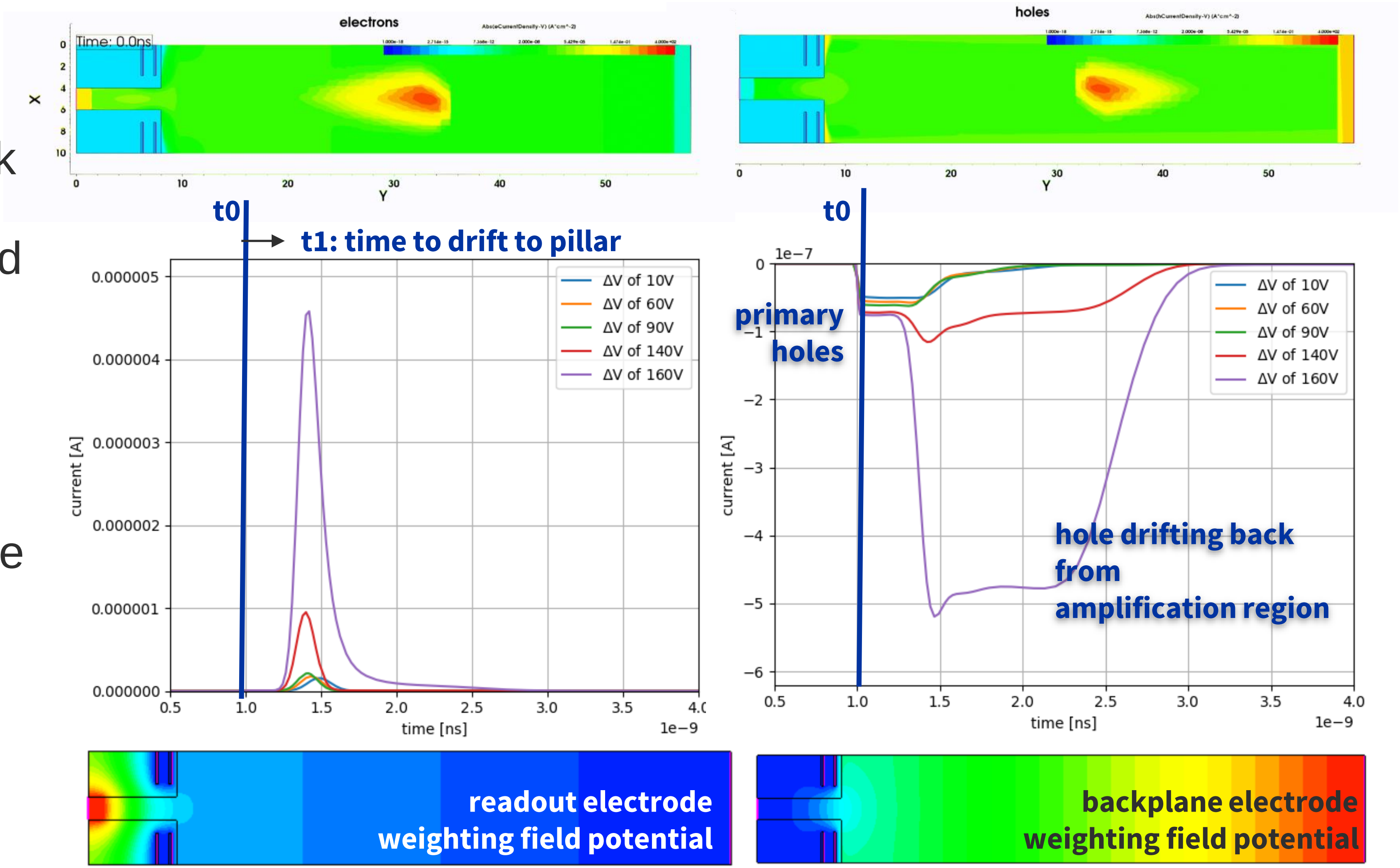


- Evaluate electric field and leakage current
  - Breakdown position depends on biasing configuration
- Pillar and bulk depletes
  - Pillar density
- High electric field in the pillars can be reached
  - Above 15V/µm



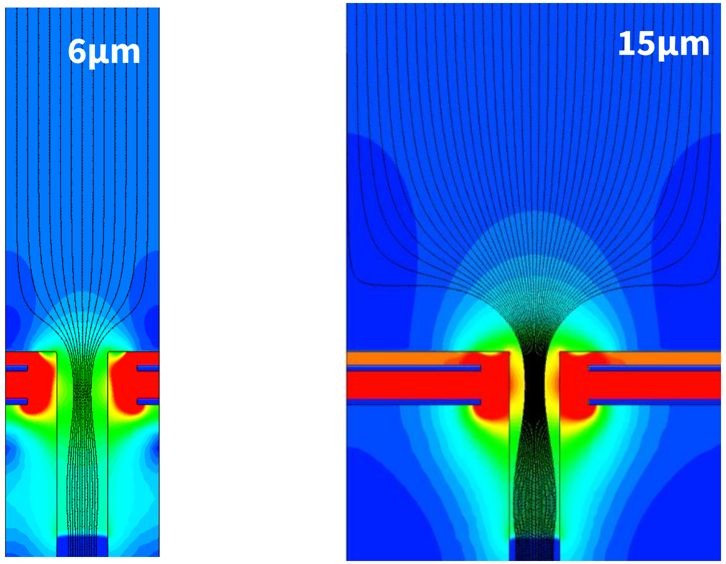
Signal simulations and charge multiplication

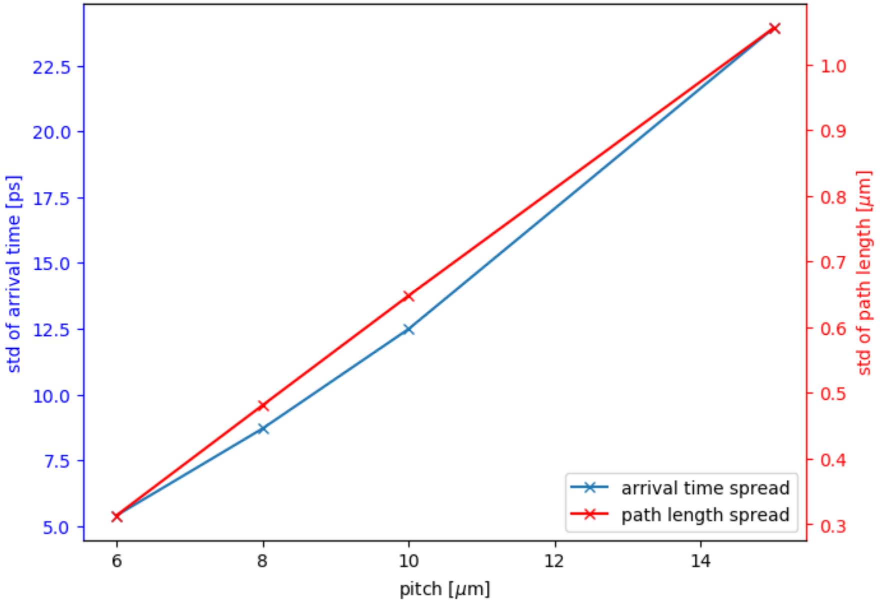
- Charge cloud deposited in bulk center
- Charges drift and get multiplied in pillars.
  - Gain= $Q_{collected}/Q_{injected}$
- Gain achieved for ΔV>100V
  - above 10 has been simulated
- Weighting field of readout electrode is concentrated in the pillar
  - Shielded by multiplication electrode
- Weighting field of backside electrode
  - “Pad like”



Optimisation
Pillar pitch and timing performances

- Arrival time distribution at the gain layer will play a large role on the final time resolution
  - See [Riegler,Windischhofer; NIM A (2021) 165265]
- Inhomogeneity in path
  - Can be reduced by reducing the inter-pillar distance
  - Down to 5ps for 6um
- Can expect similar time resolution as LGADs, to be confirmed with full MIP simulations

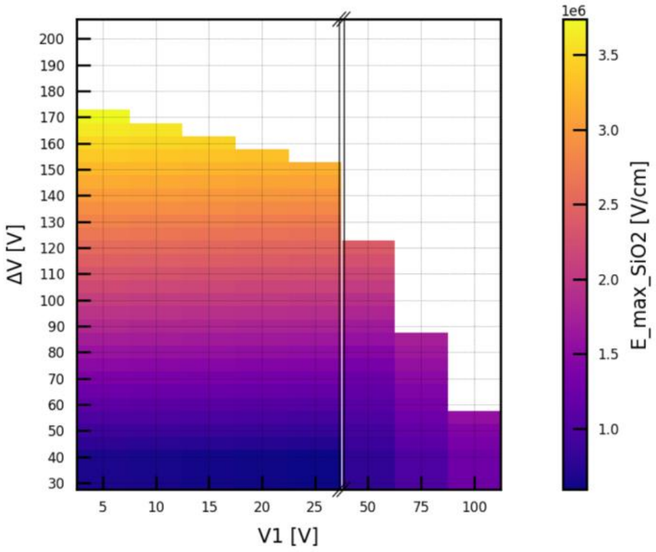




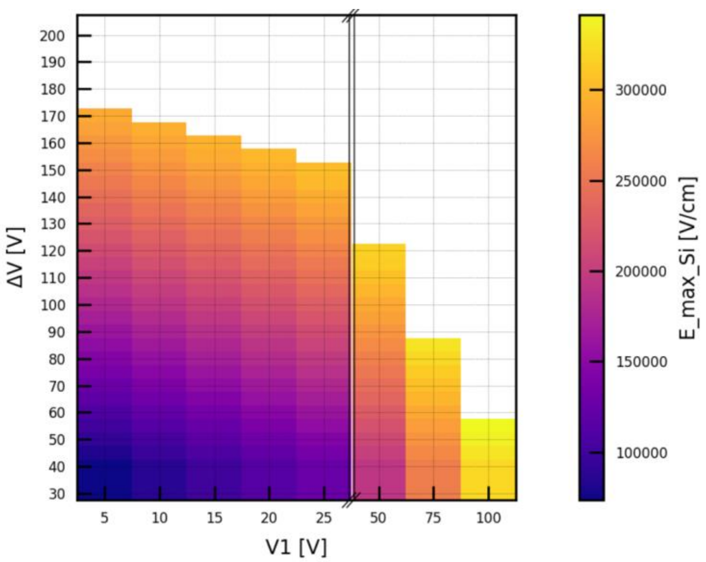
Optimisation

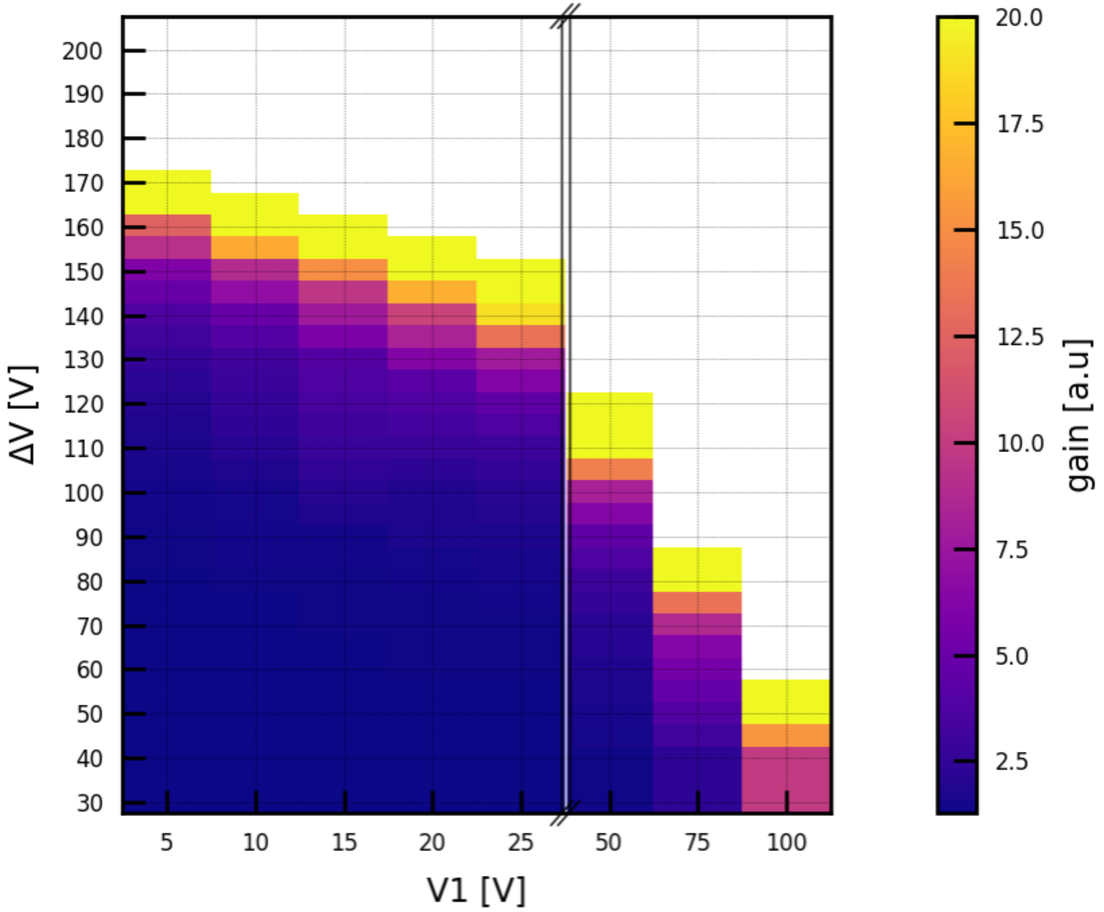
- Interplay between V_1 and ΔV can be optimised
  - freedom in choice of operation settings
- High V_1 leaves high field in silicon
- High ΔV leaves high field in the oxide

Max field in SiO_2



Max field in Si

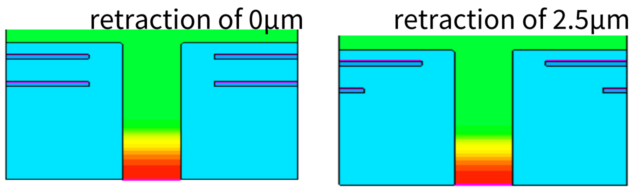


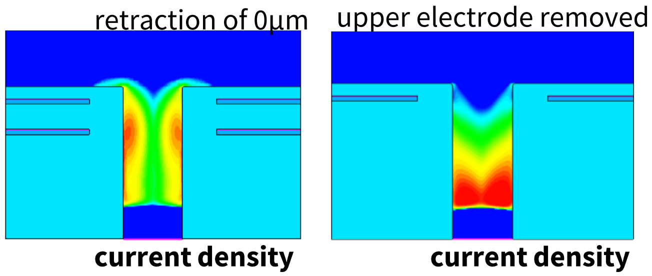


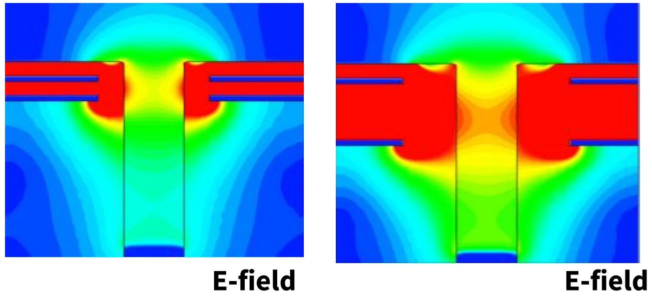
Optimisation
Electrode geometry

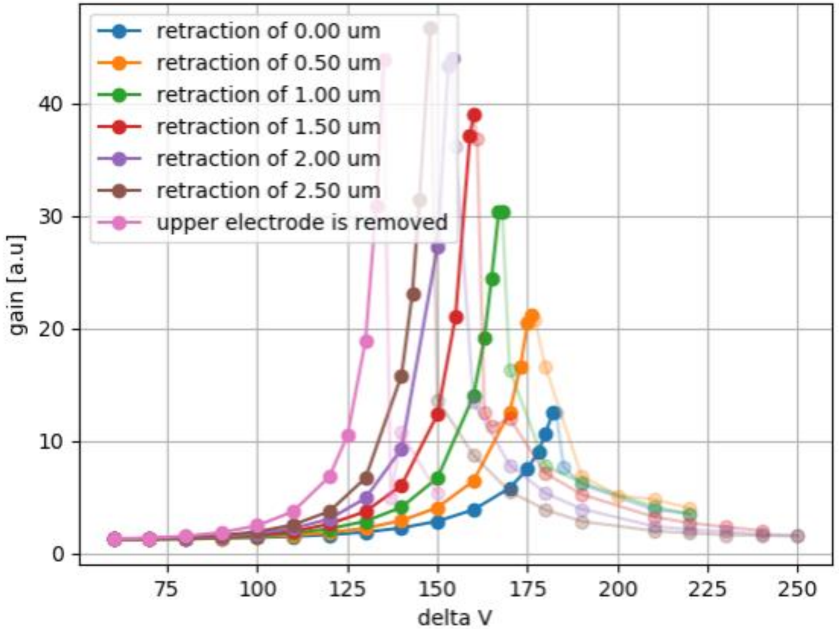
- Electrode geometries and pillar height
  - Retraction of the shallower electrode allow to better fill the pillar with high field
  - Similar effect to rising V_1
- Single electrode configuration
  - Simpler but higher field in the silicon
  - Different breakdown location
- Larger inter-electrode distance
  - Better spreading of the field
  - Less localised high field values

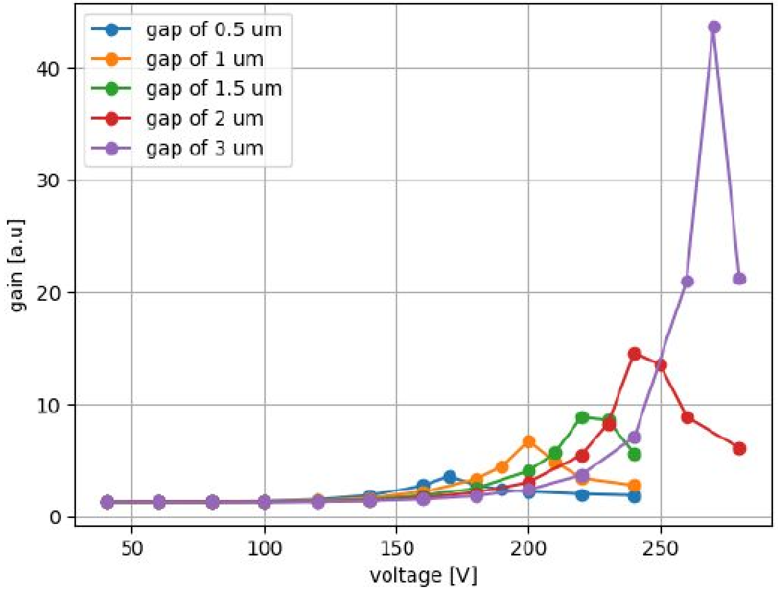
Several degrees of freedom to cope with production process constraints





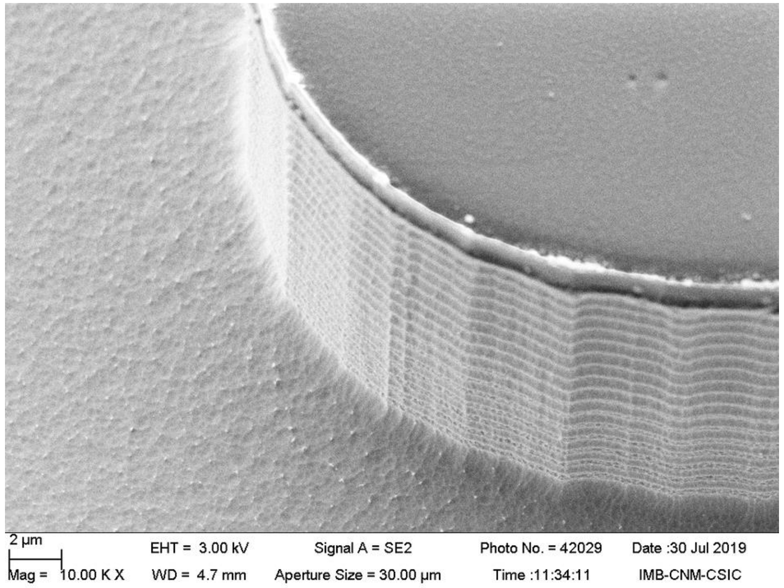






Possible production processes

[courtesy of CNM]



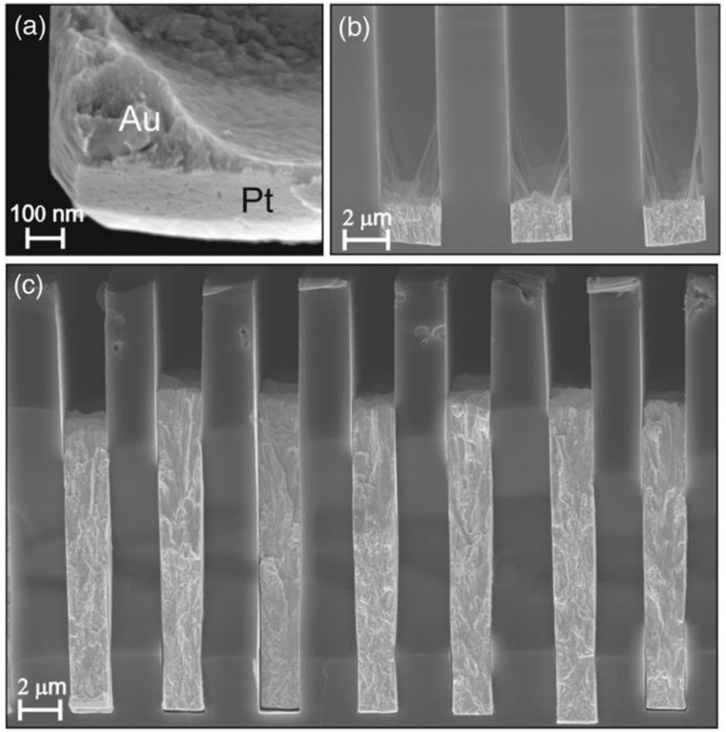
DRIE based

- Discussions about the process and its constraints with LeTI and CNM
- Now: evaluate what topology that can really be achieved
  - Electrode/wall guard, thickness of oxide, corner shapes…
- Next: electrical properties?
  - SiO_2/Si interface, scalloping, ...
- Homogeneity of the production?
- Performances

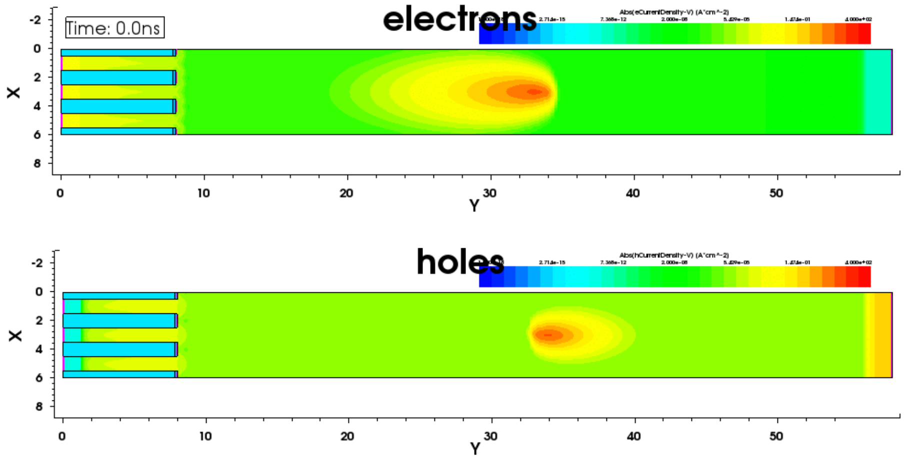
To be investigated in 2022

Metal Assisted Chemical Etching

[L. Romano *et al*; AdEM 22 (2020) 2000258]



- Discussions with PSI
- MacEtch Process
  - Metal mask used as a catalyst for etching.
  - Electroplating with gold
  - Electrode directly on silicon
- Less “production ready”
- More appropriate for single electrode structure
- Denser pillars
- No more constraints on the guard
- Could be a simpler processing technique
- Simulations started

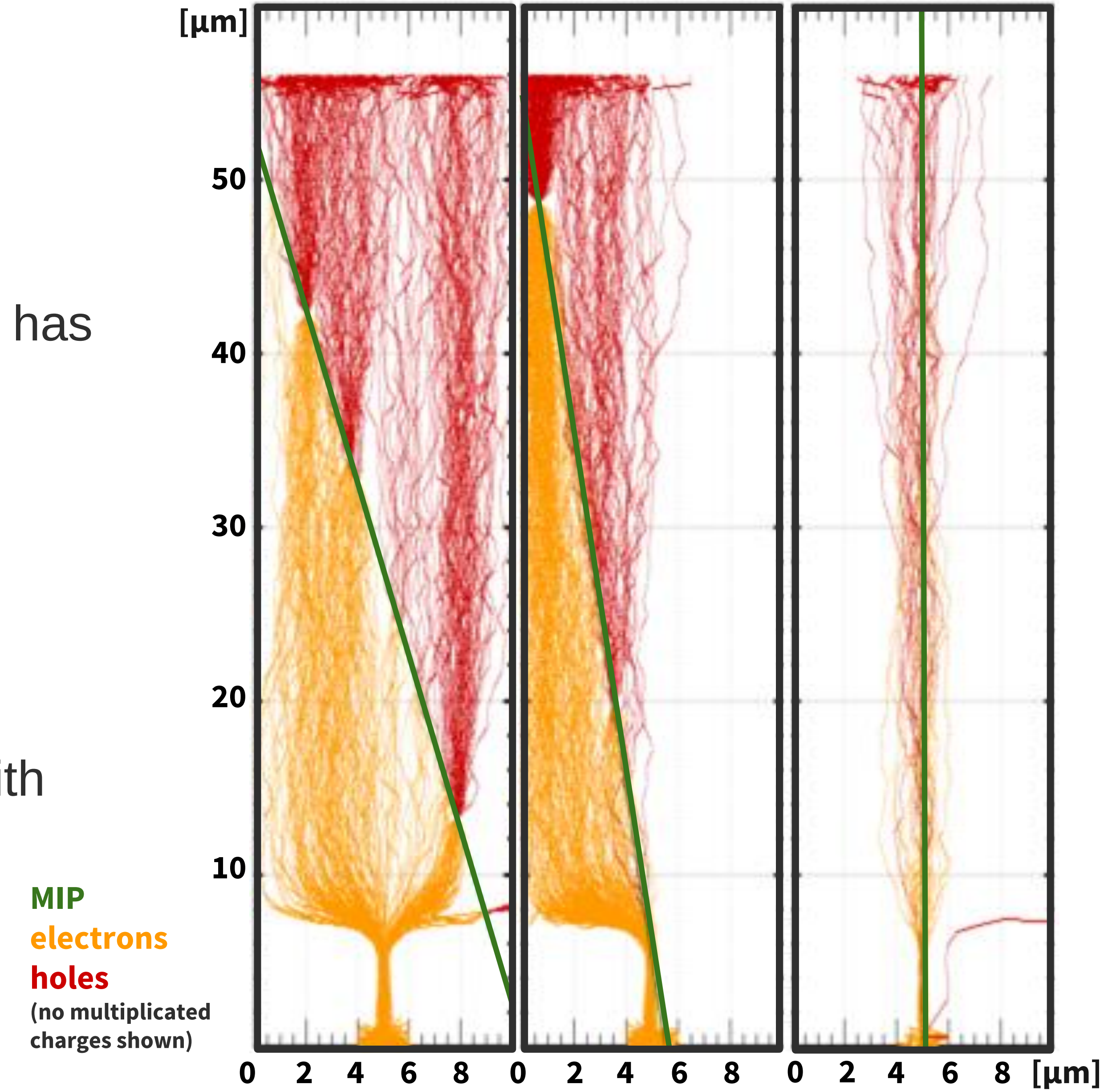


Summary and Outlook

- A new solid state radiation detector concept has been presented.
    - Small pitch
    - Expected time resolution similar to LGADs
    - Gain is not doping dependent

- Next steps
    - finish simulations full MIP simulations with Garfield++
    - preparation to produce a demonstrator

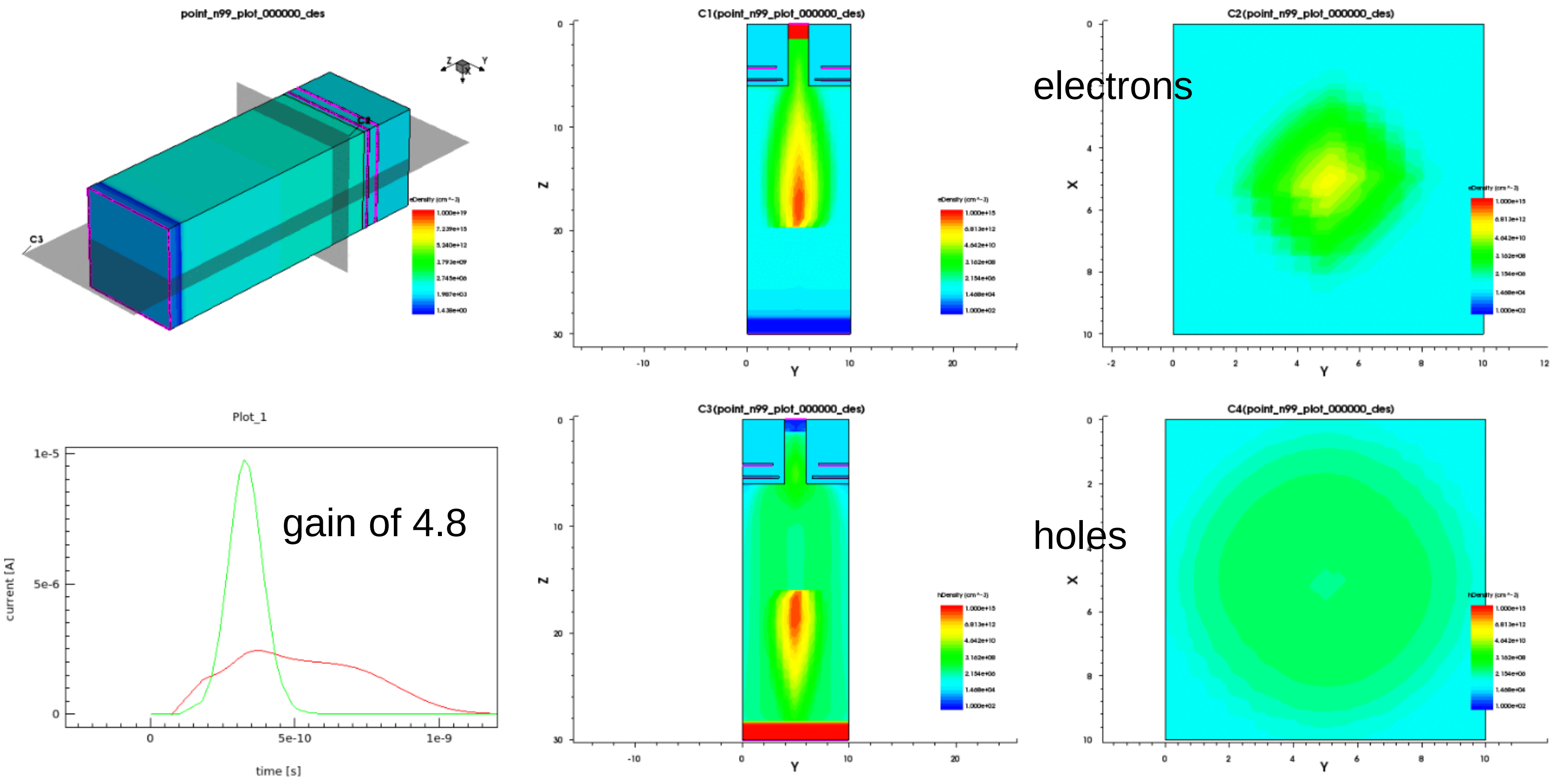
MIP simulation with Garfield++



home.cern

Backup

3D simulations



CV curves

- **Simulation of one unit cell (no inter-pixel capacitance)**