Radiation damage investigation of epitaxial p-type silicon using Schottky and pn-junction diodes

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39TH RD50 Workshop, 17-19 November 2021

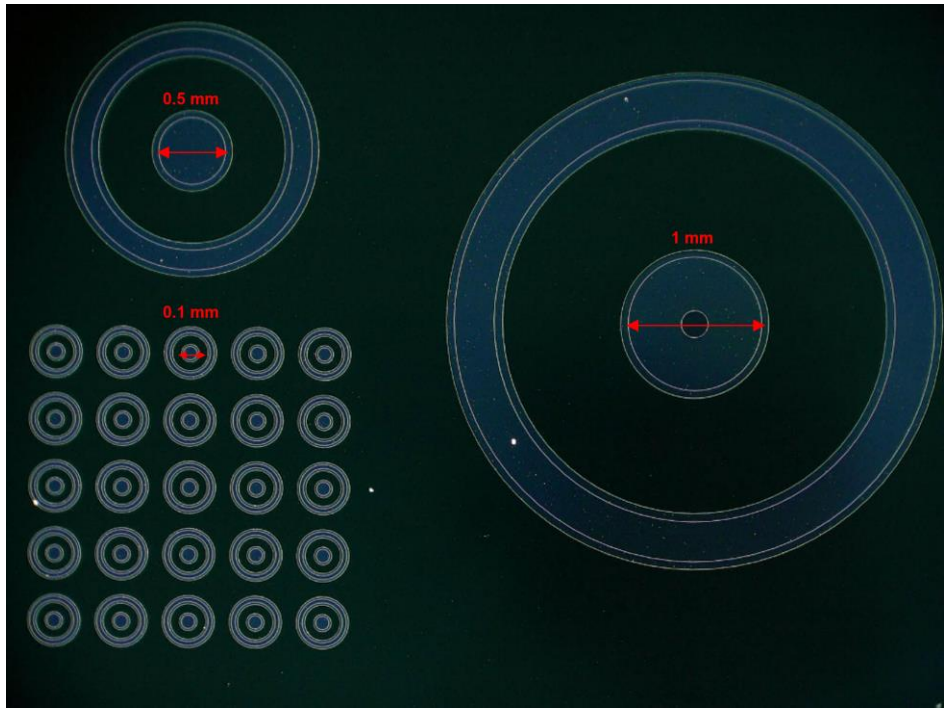
Schottky Project description and goals

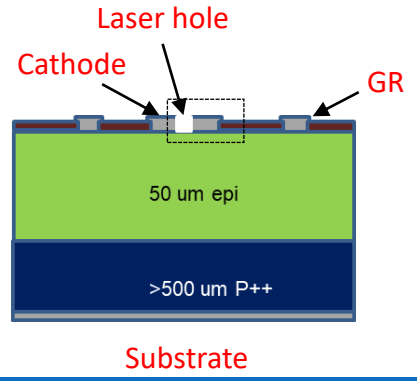
- **What:**
  - fabricate Schottky and n^+p diodes on p-type epitaxial (50µm thick) silicon wafers
  - doping concentrations as they are normally found in CMOS MAPS devices
- **Why:**
  - investigate and gain a deeper understanding of radiation bulk damage in CMOS sensors.
  - develop reliable damage models that can be implemented in TCAD device simulators (Synopsys or Silvaco)
- **How:**
  - purchase of 6-inch wafers at five B-doped epitaxial levels (10^{13}, 10^{14}, 10^{15}, 10^{16} and 10^{17} cm^{-3}) 25x each, total **125 wafers**
  - fabrication process has started both at ITAC (RAL) and Carleton University Microfabrication Facility (CUMFF).
  - tests will be carried out at RAL, Carleton, Birmingham, JSI, IHEP

Design and layout of devices

5 type of devices proposed:

- #1: 2 mm Ø cathode with 0.4 mm Ø central hole, 10 x 10 mm^2 area
- #2: 1 mm Ø cathode, 0.2 mm Ø central hole, 5 x 5 mm^2
- #3: 0.5 mm Ø cathode, no central hole, 2.5 x 2.5 mm^2
- #4: 0.1 mm Ø cathode, no central hole, 0.5 x 0.5 mm^2
- ‘cell’ with the previous 3 flavors (2,3,4) grouped together, to exploit wafer uniformity on small area
- #5: 6 TLM points for contact and epi resistance
- 2 masks only (metal and oxide)
- detailed description during the 35th RD50 workshop





Fabrication details & comparison

RAL-ITAC

- Schottky fabrication process only, optimised on test wafers
- oxide deposition @150°C
- Al sputtering immediately after etching (no thin SiO2 layer)
- Al lift off in Acetone ultrasonic tank

CUMFF

- pn-junction and Schottky processes, optimised on test wafers
- 6” substrate wafers laser cut into 4” or 6” wafer pieces
- high temperature thermal oxidation
- Al front metal thermal deposition, back Al via e-beam evaporation
- front metal patterning + etching

full details of fabrication processes in E.G. Villani’s talk from the 36th RD50 Workshop

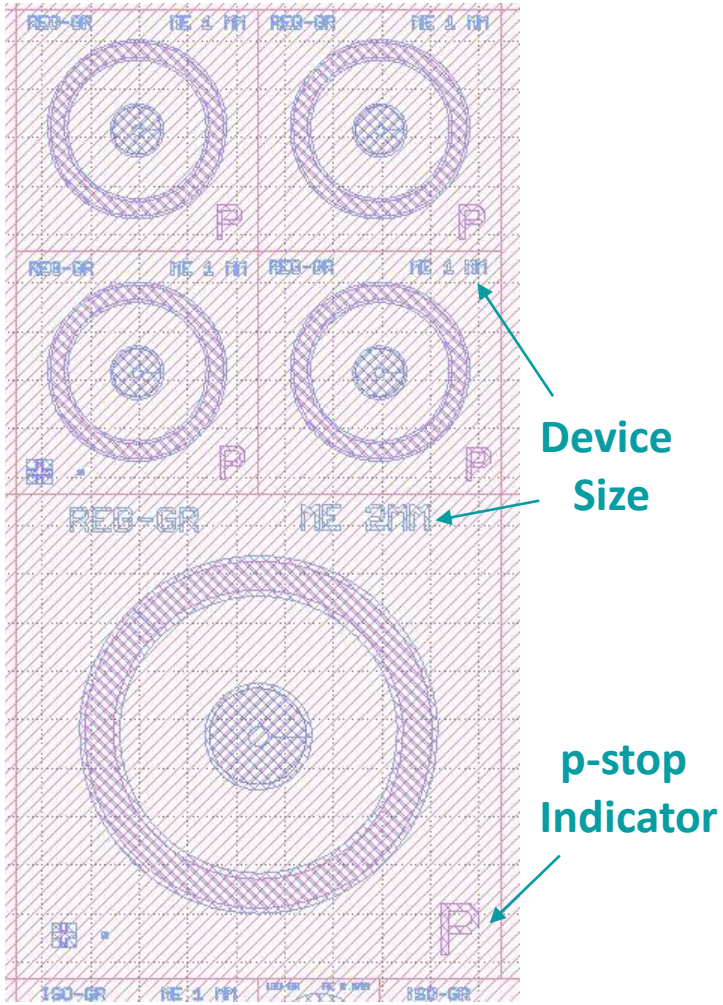
Fabrication status update (since last workshop)

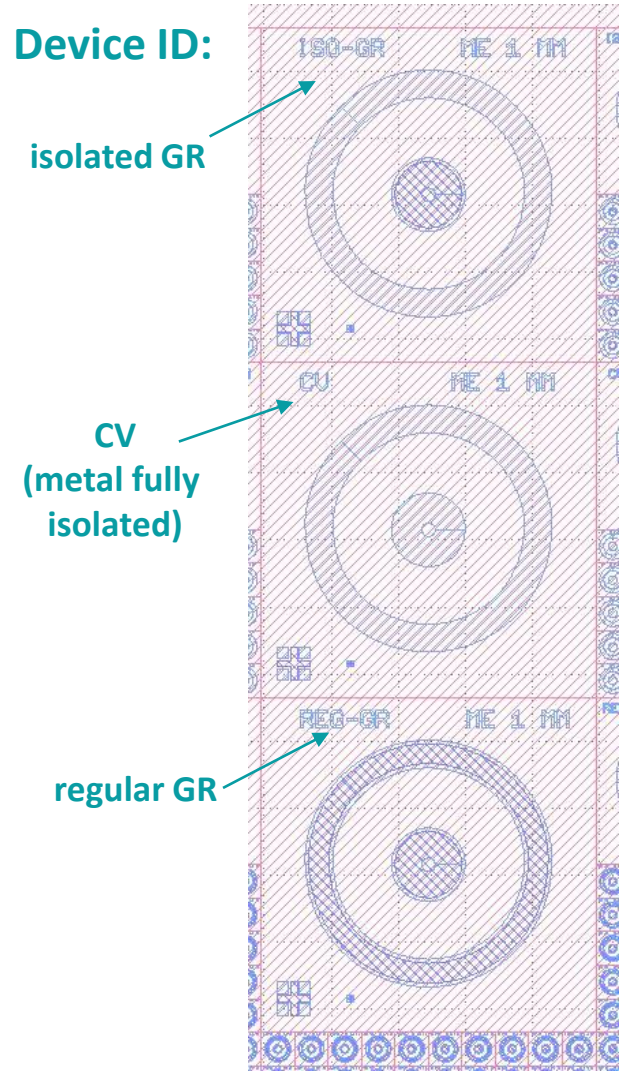
CUMFF

- new masks made, including isolated MOS gate GR variation for all device types + optional p-stop
  - after initial success in reducing leakage current in high-resistivity wafers (see last workshop)
- 2x ¼ 1e16 wafers + 2x full 4” 1e13 wafers; one for each doping concentration as standard pn-junctions or pn + additional p-stop

RAL

- 5x full 6” Schottky wafers (3x 1e13; 1x 1e14, 1x 1e15)





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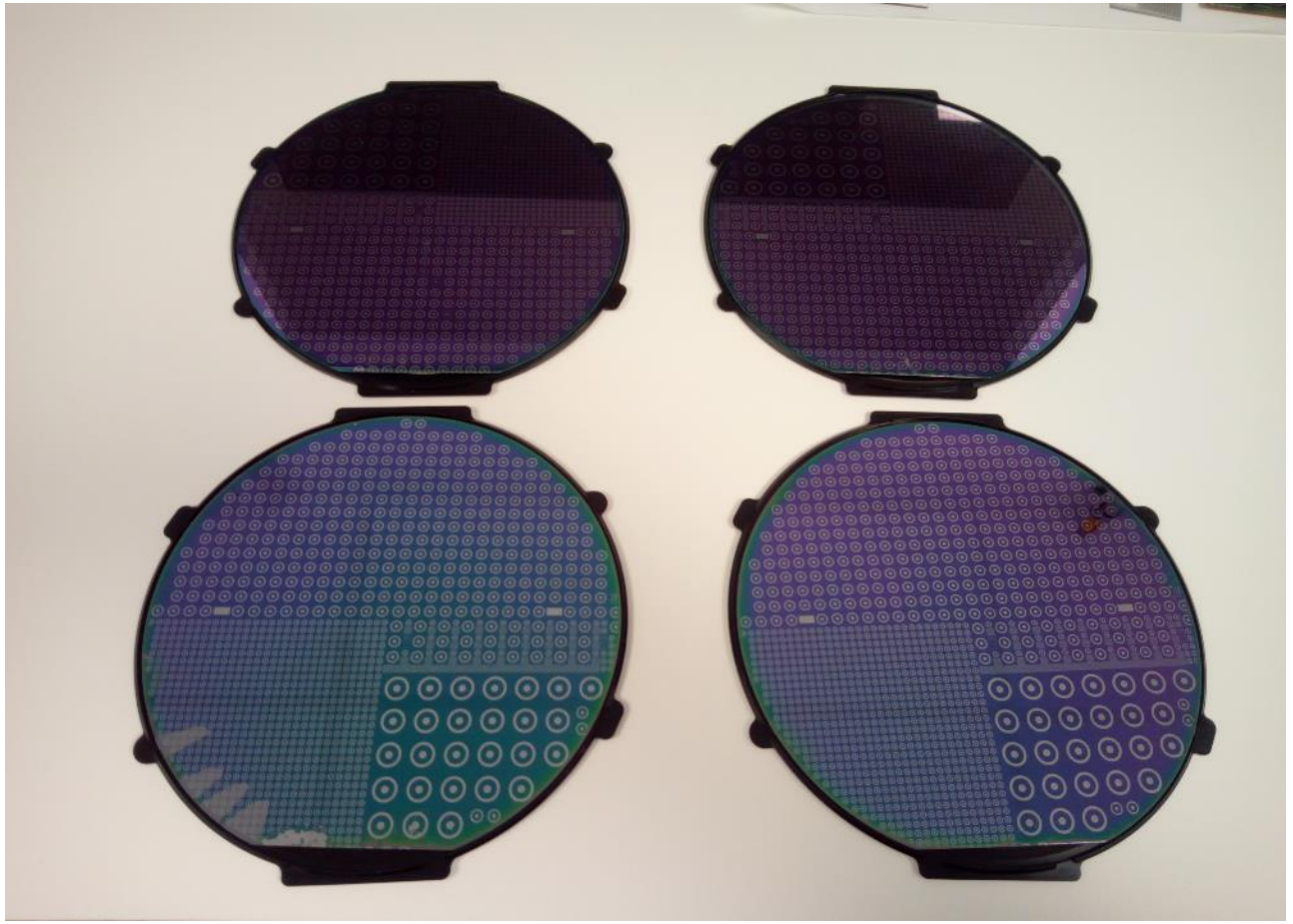
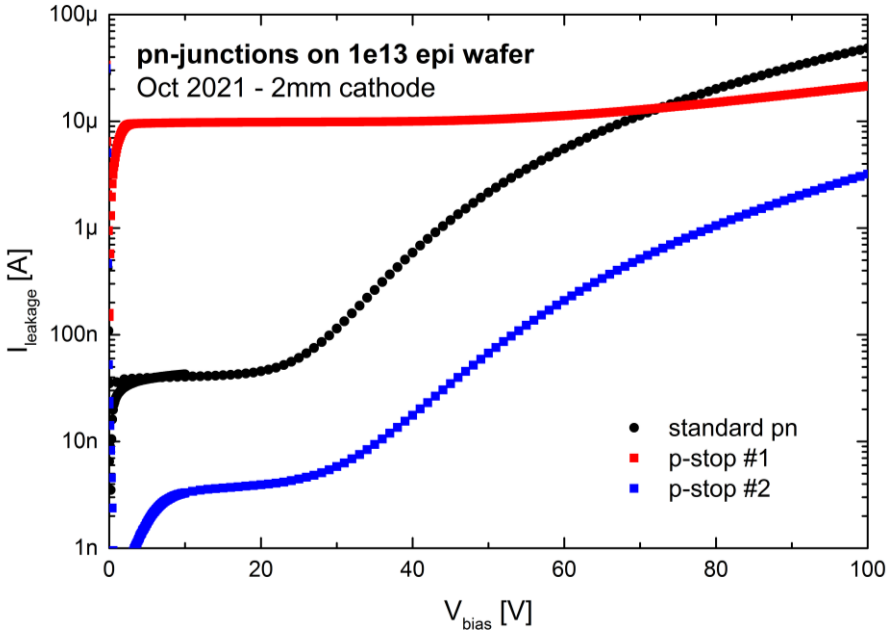
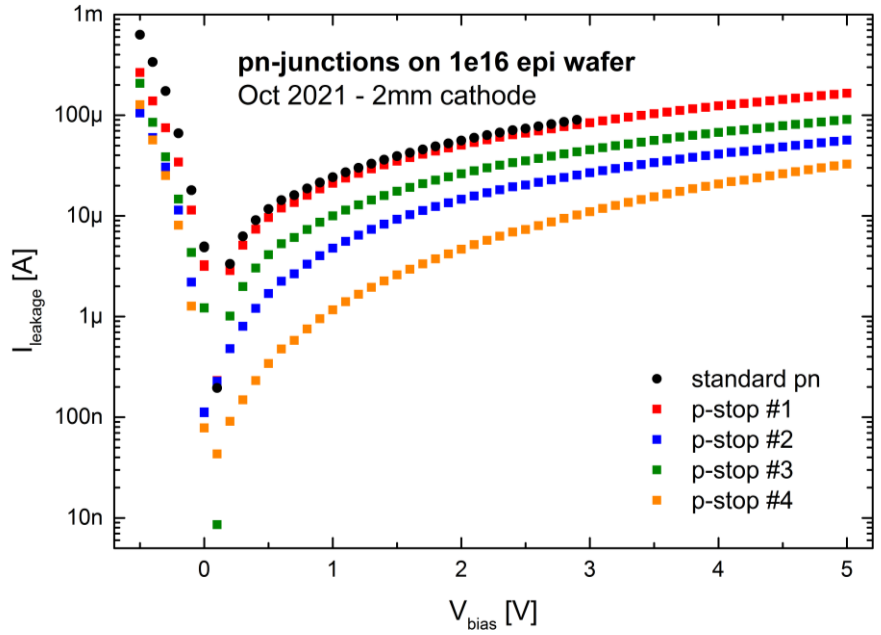


T = 21°C

IV measurements: CUMFF pn-junctions (regular GR, floating)



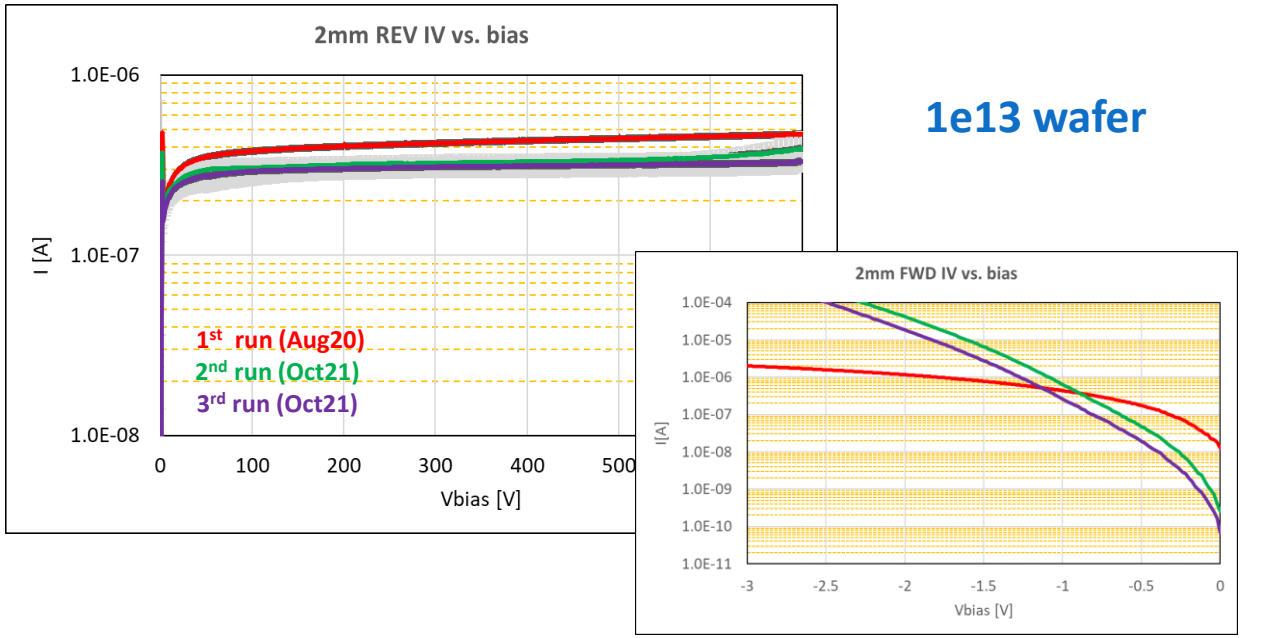


- current can vary by large margin on same wafer
- very low initial current often seen
- no hard breakdowns observed; gradual increase in current
- ➢ leakage current at much lower levels compared to first iterations
- ➢ effect of different GR flavours and p-stop will be investigated in coming weeks

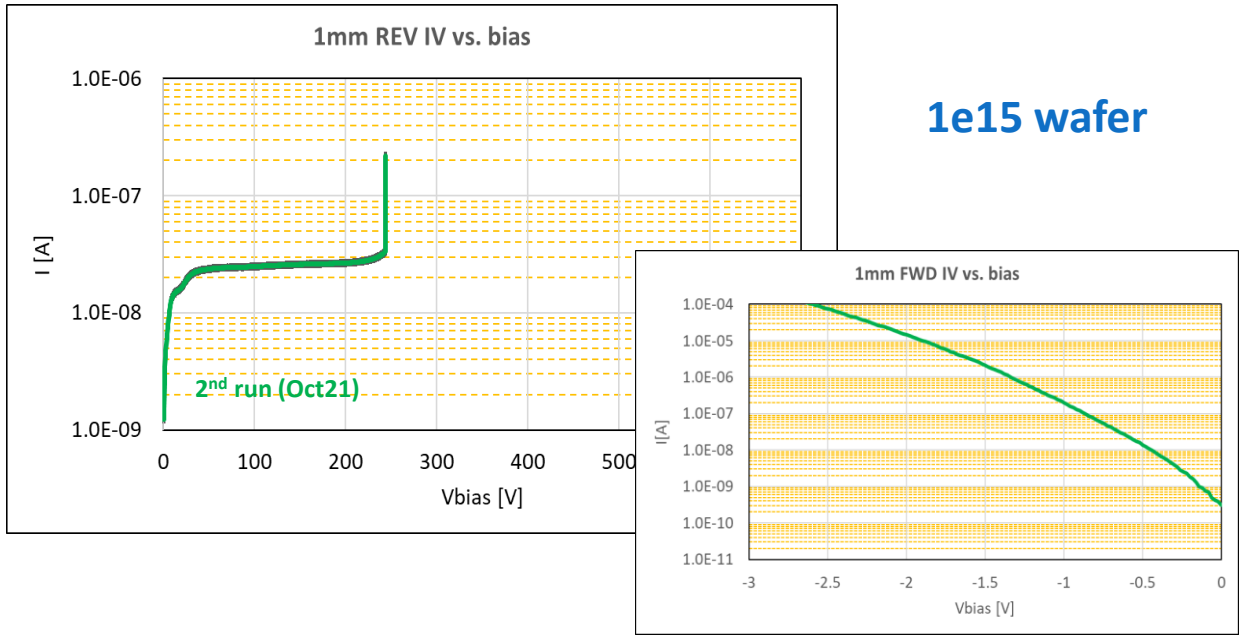
- high leakage current even at low bias voltages
  - no ‘plateau’, current keeps increasing
- smaller structures often have inconsistent IV curves
- ➢ first fabrication on low-resistivity wafer, improvements in future iterations

T = 21°C

IV measurements: RAL Schottky 1e13 vs. 1e15



1e13 wafer



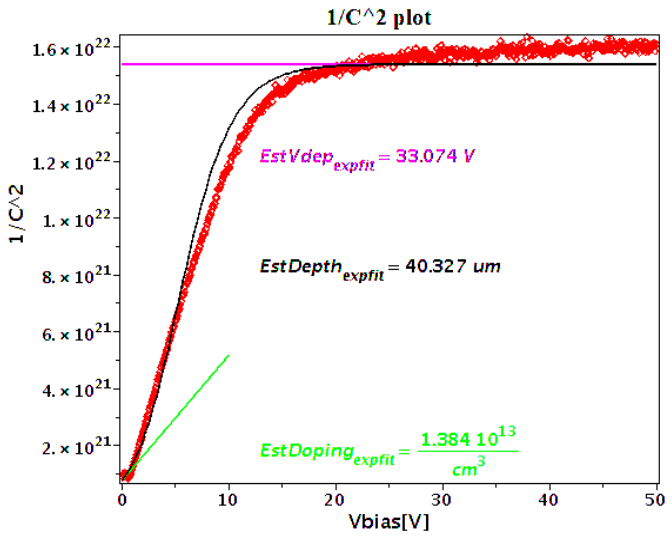
1e15 wafer

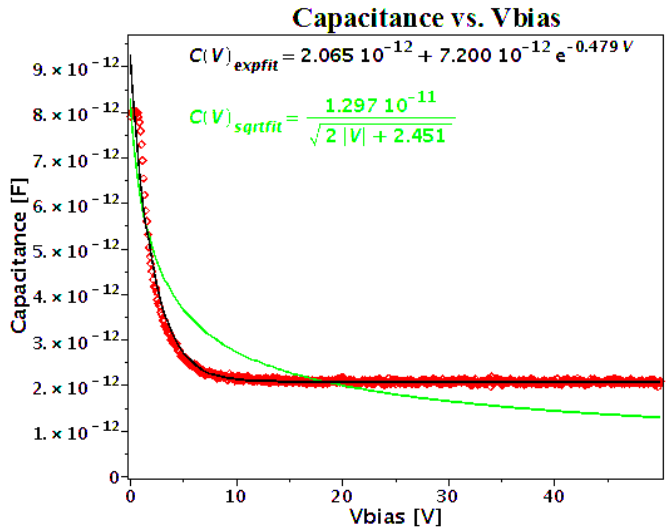
- reverse bias IV similar in all runs, slightly lower leakage in the two latest runs
  - breakdown voltage > 700V
- forward bias shows very different characteristics

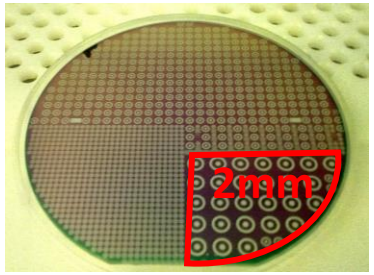
- expected lower leakage in reverse bias, with lower BV
- measured BV is high for this doping
- forward bias ~linear

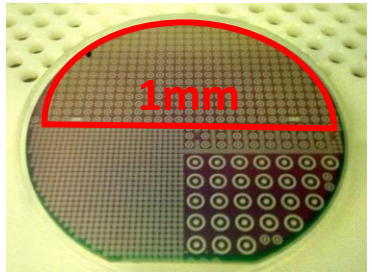
CV measurements: RAL 1e13 Schottky

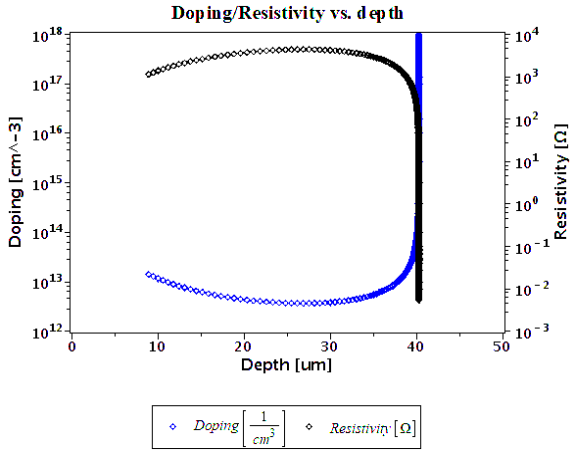
T = 21°C
f = 100kHz
V_{AC} = 30mV











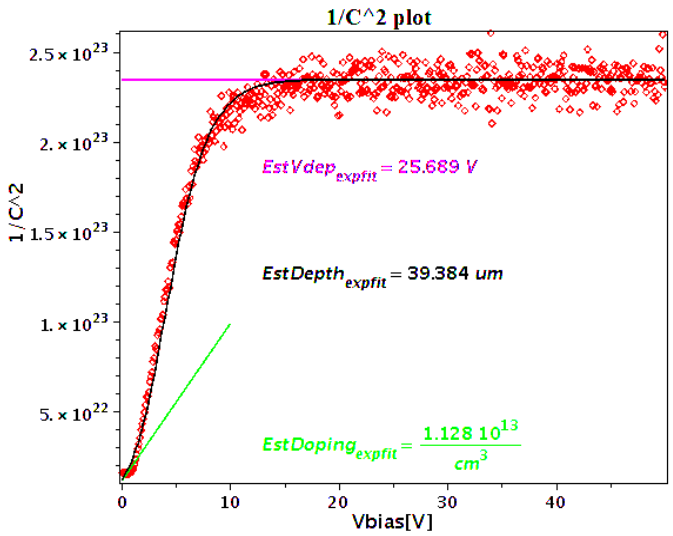
V_d	1.716
φ_b	2.134 (?)

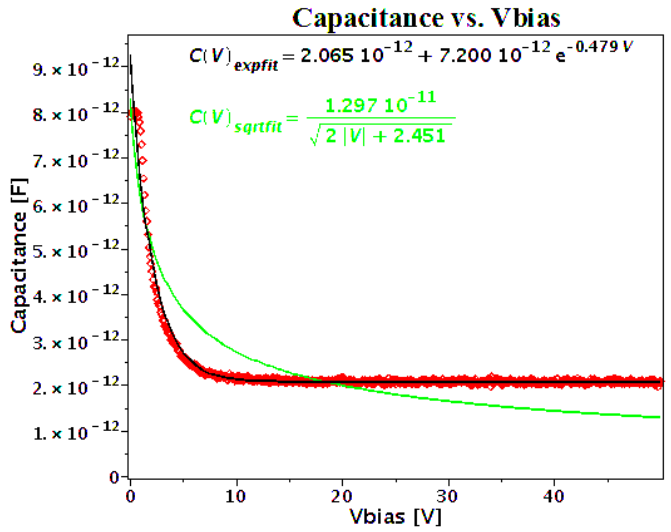
V_d	1.343
φ_b	1.739 (?)

Φ(Al) = 4.1 [eV]
χ(Si) = 4.05 [eV]

φ_b = 1.16 - (4.1 - 4.05)
= 1.11 (ideal case)

φ_b from CV too high – needs further investigation (TCAD)

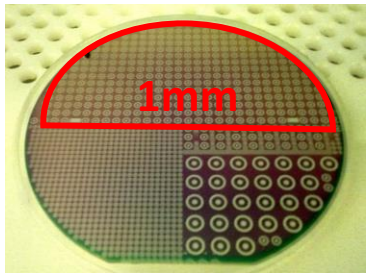


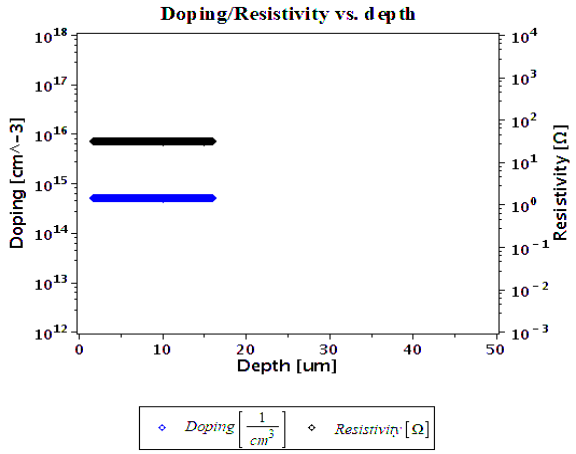


CV measurements: RAL 1e15 Schottky

T = 21°C
f = 100kHz
V_{AC} = 30mV

- 2 HR wafers show doping as expected
  - CV plot not really well described by 1/√V fit
  - barrier height estimate from CV too high
  - estimate from IV in progress
- devices on 1e15 wafer so far show very good 1/√V Cap dependence
  - doping as expected
  - barrier height clearly too high





Φ(Al) = 4.1 [eV]
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φ_b = 1.16 - (4.1 - 4.05)
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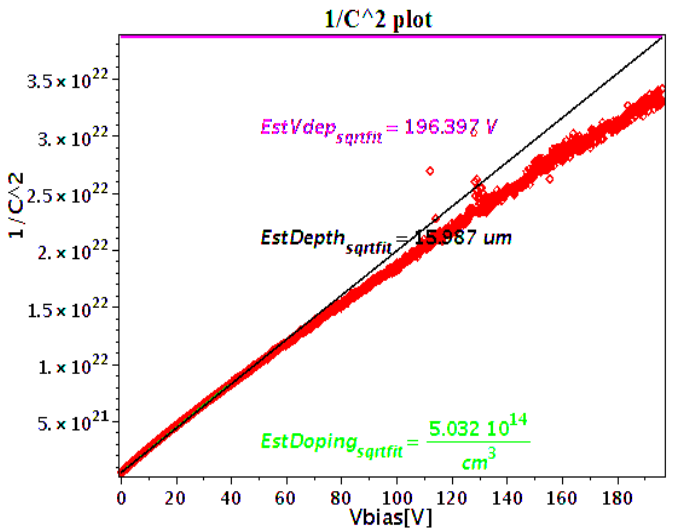
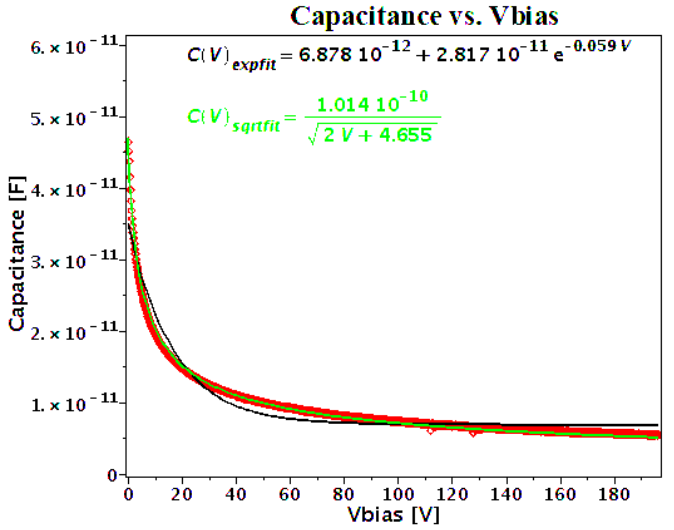


V_d	2.328
φ_b	2.646 (?)



Summary & outlook

- testing has proceeded successfully after shutdown periods last year
- TCAD simulations of Schottky diodes ongoing
  - need to improve breakdown voltage simulation
- fabrication efforts at RAL and CUMFF has ramped up
  - new mask design at CUMFF proves adaptability of fabrication process to findings

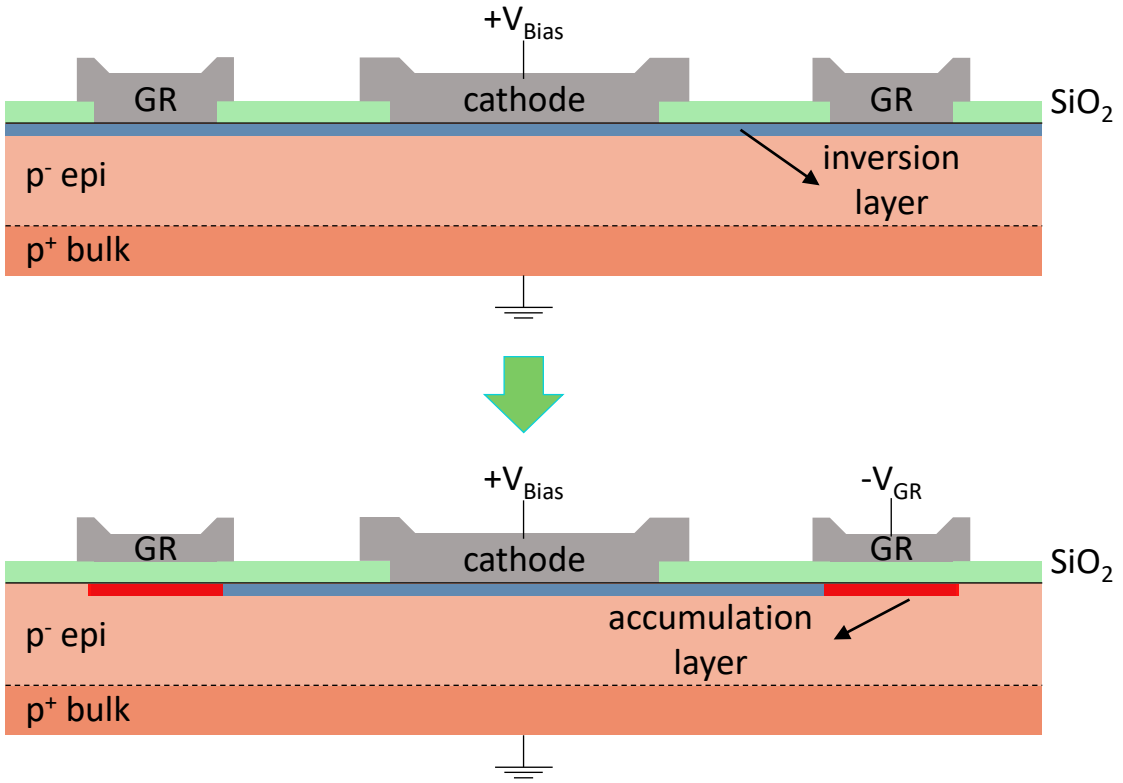
Outlook:

- charge collection measurements at RAL
- DLTS + TAS measurements at Carleton
- proton irradiations at Birmingham, neutron irradiations at Ljubljana

Backup

Reducing leakage current: MOS gate guard ring structure

- some diode runs on 1e13 cm^{-3} wafer had high leakage currents
- tests showed that cause was formation of electron inversion layer
- expected typical behaviour after radiation damage in oxide
  - outlook to actual behaviour after irradiation
- mitigate by modifying the masks to isolate GR on oxide
- apply low negative V to gated GR
  - accumulation layer formation in interface
  - limit inversion layer



solve this issue **now**

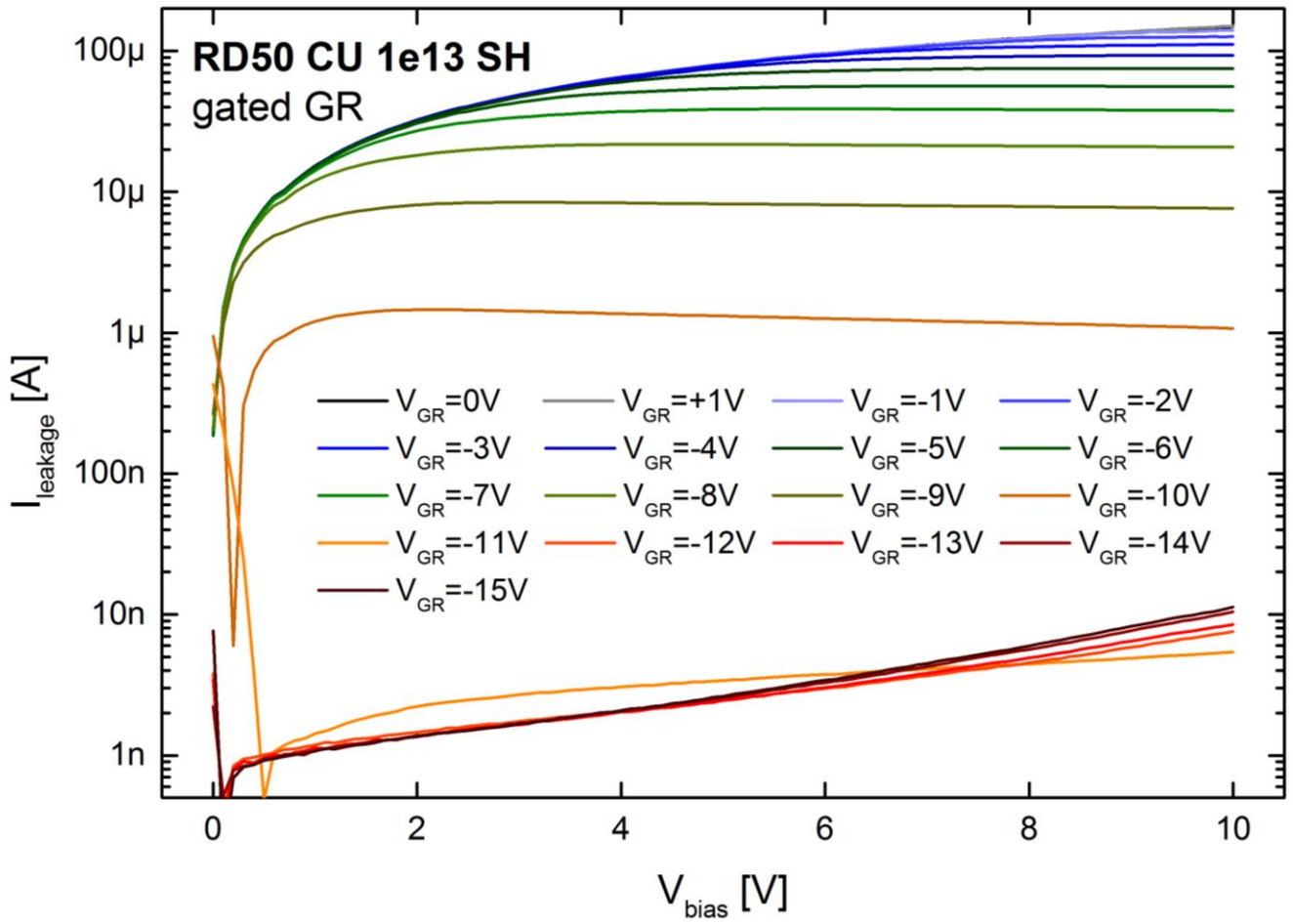
⇒ improve performance of irradiated devices **later**

Reducing leakage current: MOS gate guard ring structure

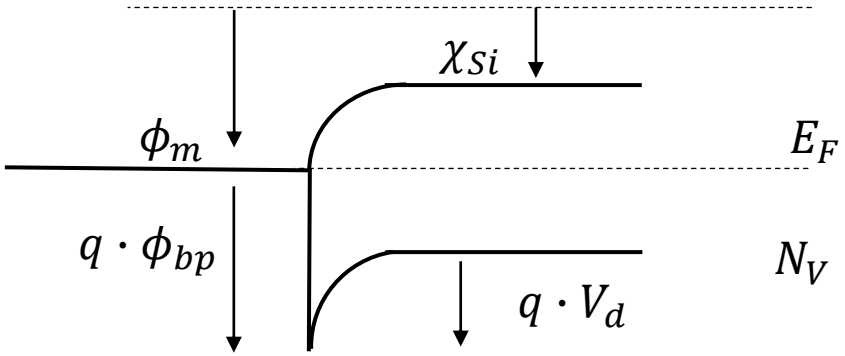
- gated GR yielded expected results
- high leakage fully mitigated for V_{GR} <-10V
  - depending on oxide thickness
- devices even showed ‘memory effect’
  - stable-ish charge traps in interface
  - further improvements during repeated scans

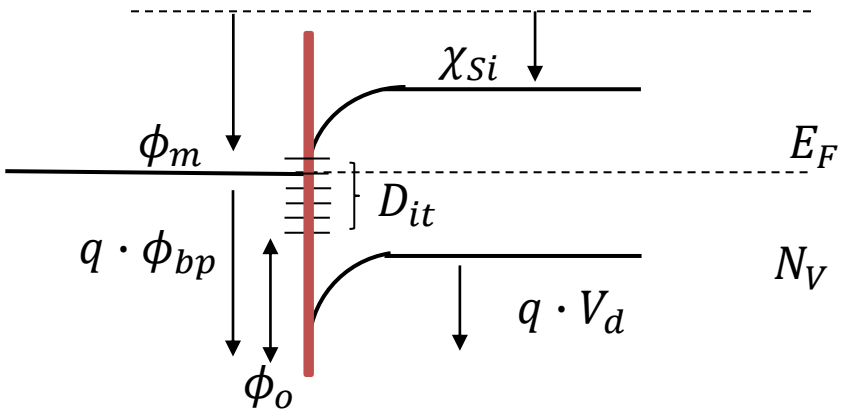
➢ try p-stop for comparison and more consistent (?) performance

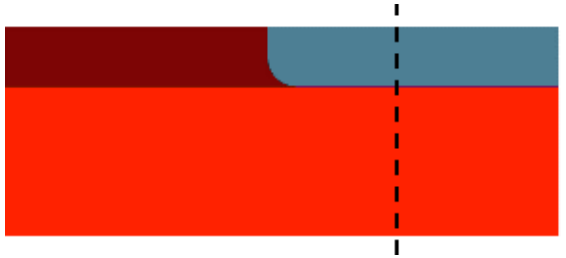
➢ looking forward to effects on irradiated devices



Schottky barrier – Theory







$$\phi_b = V_d + \frac{K \cdot T}{e} \cdot \left(ln\left(\frac{N_V}{N_A}\right) + 1 \right) - \Delta\varphi$$

$$* \phi_b = \gamma \cdot \left(E_g + \chi_{si} - \phi_m\right) + (1 - \gamma) \cdot \phi_o$$

$$\gamma = \frac{\varepsilon}{\varepsilon + q^2 \cdot \delta \cdot D_{it}}$$

Metal	Si
Al	0.58
Ag	0.54
Au	0.34
Ti	0.61
Hf	0.54
Ni	0.51
Pt	0.20

[1]

Table 1. Experimental barrier height data for p-type silicon Schottky diodes

Metal	ϕ_m (eV)	ϕ_{bn} (eV) From $\frac{1}{C^2}-V$	From $I-V$	ϕ_{bn} (eV) avg.	ϕ_{bn} (eV) (Ref. 3)	$\phi_{bn}+\phi_{bn}$ (eV)
Ag	4.31	0.53	0.55	0.54	0.56	1.10
Al	4.20	0.57	0.58	0.58	0.50	1.08
Au	4.70	0.34 (210°K)	0.34 (210°K) 0.35 (250°K)	0.34	0.81	1.15
Cu	4.52	0.46 (280°K)	0.46	0.46	0.69	1.15
Ni	4.74	0.50	0.51	0.51	0.67	1.18
Pb	4.20	0.54	0.56	0.55	0.41	0.96

ϕ_m = metal work-function; ϕ_{bn} = barrier height on p-type silicon; ϕ_{bn} = barrier height on n-type silicon (Ref. 3).

ε = permittivity of interface layer ~ ε_o
δ = thickness of interface layer hp: 1-2 [nm][2]
D_{it} = interface states density → [1.3-2.6]e13 [cm^{-2} eV^{-1}]

estimate of ϕ_o~ 0.38eV for neutrality level above BV edge

The presence of metal-Si interface states affects the barrier height ϕ_b and diffusion potential V_d

* Cowley-Sze model with thin oxide insulating layer between Si-Metal

[1] *R.W. Bene'et al.; J.Vac.Sci.Technol.* 14.925 (1977)
[2] ITAC measurements & http://dx.doi.org/10.1063/1.347181

Schottky barrier height

- Schottky barrier derived from CV measurement
- measured depletion voltage + depth:

	Layout #1 (2mm)	Layout #2 (1mm)
V_{dep}	7.715 V	4.03 V
D_{dep}	40.77 um	36.17 um

- diffusion potential inferred from the intercept of C^{-2} with the V axis using V_{dep}

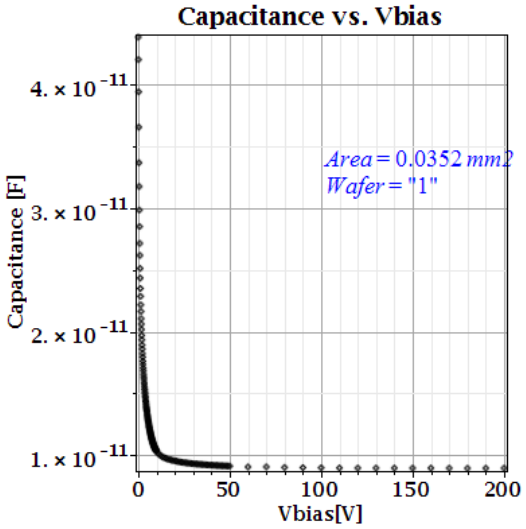
$$V_d^{2mm} = 0.3343\ V$$
$$V_d^{1mm} = 0.3719\ V$$

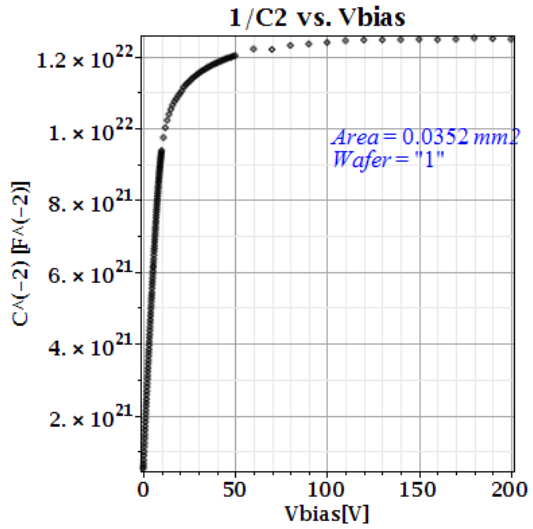
- barrier height calculated from:

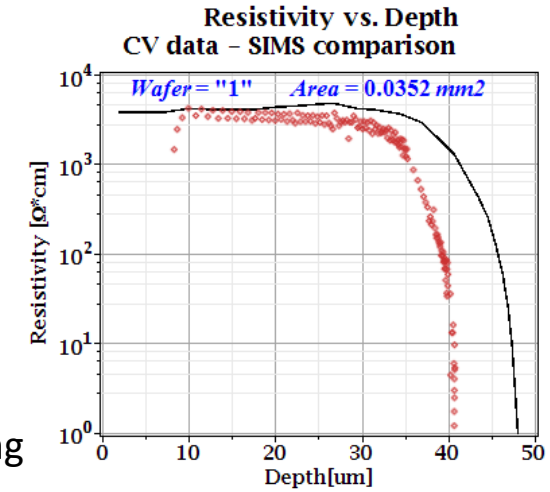
$$\phi_{bp}^{2mm} = 0.719\ V$$
$$\phi_{bp}^{1mm} = 0.756\ V$$

$$\phi_b = V_d + \frac{K \cdot T}{e} \cdot \left(ln\left(\frac{N_V}{N_A}\right) + 1 \right) - \Delta\phi$$

V_d: from $1/C^2$ intercept; $\frac{N_V}{N_A}$: from C-V; $\Delta\phi$: barrier lowering (fwd only)







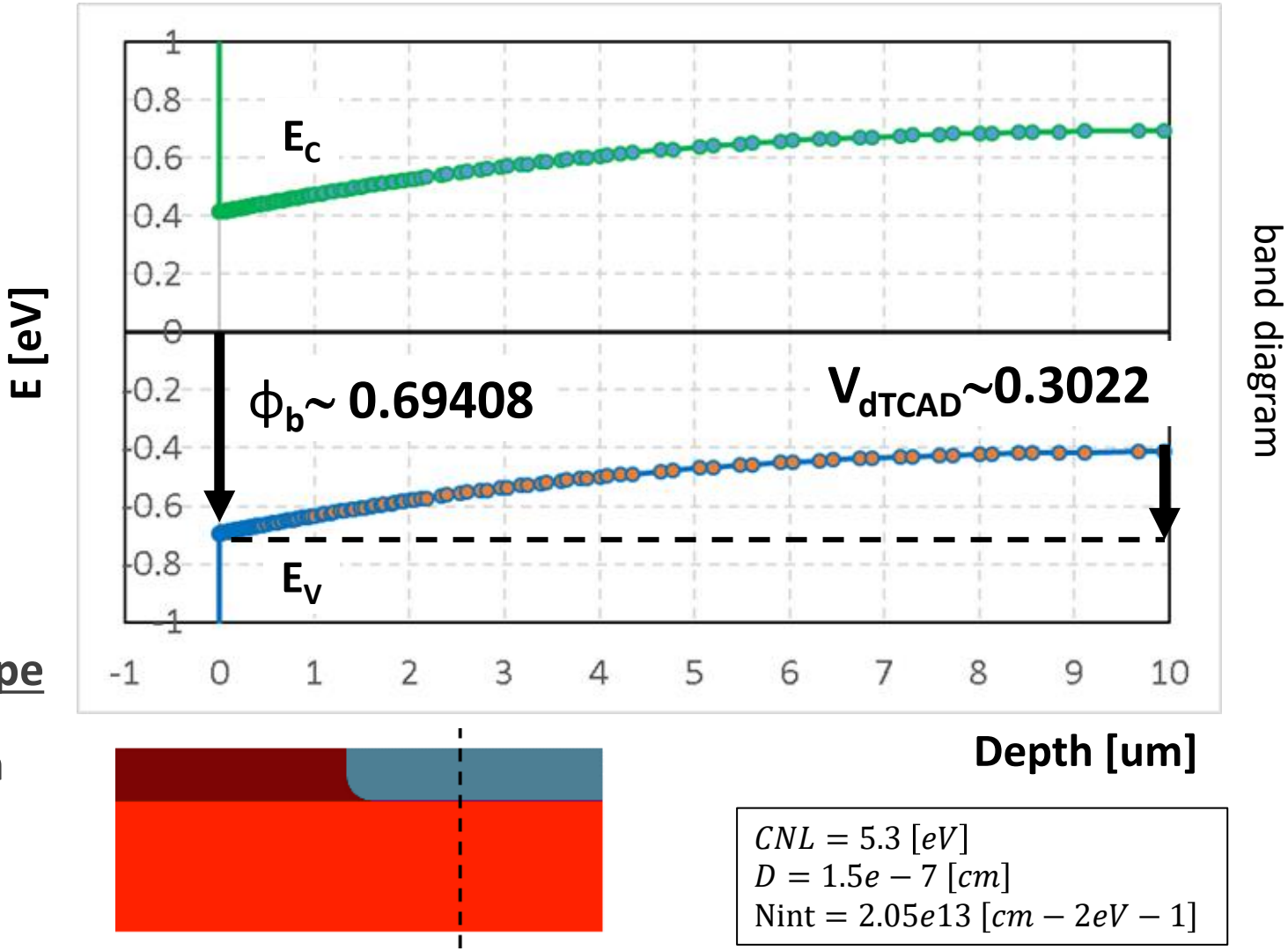
Schottky barrier in TCAD

- experimental data of barrier height vs. metal workfunction for n-type Si

Metal	Si	Ge	GaAs
Al	0.58	0.48	–
Ag	0.54	0.50	0.63
Au	0.34	0.30	0.42
Ti	0.61	0.48	–
Hf	0.54	–	0.68
Ni	0.51	–	–
Pt	0.20	–	–

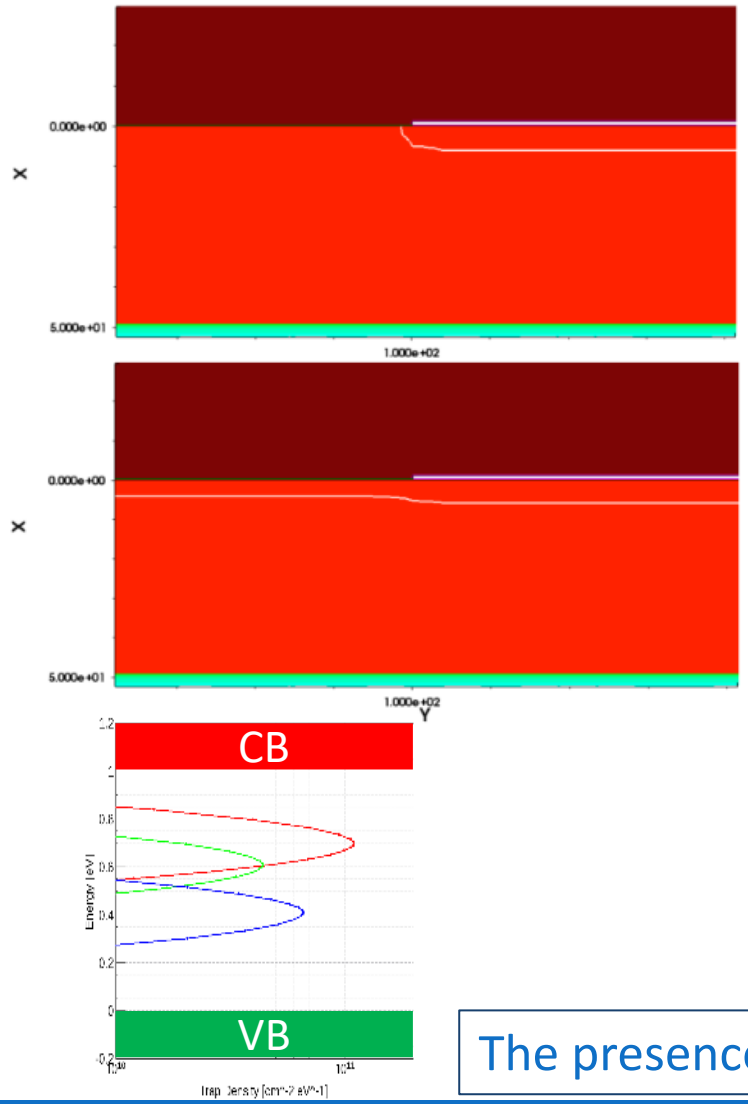
➢ **assuming ~ the same for p-type**

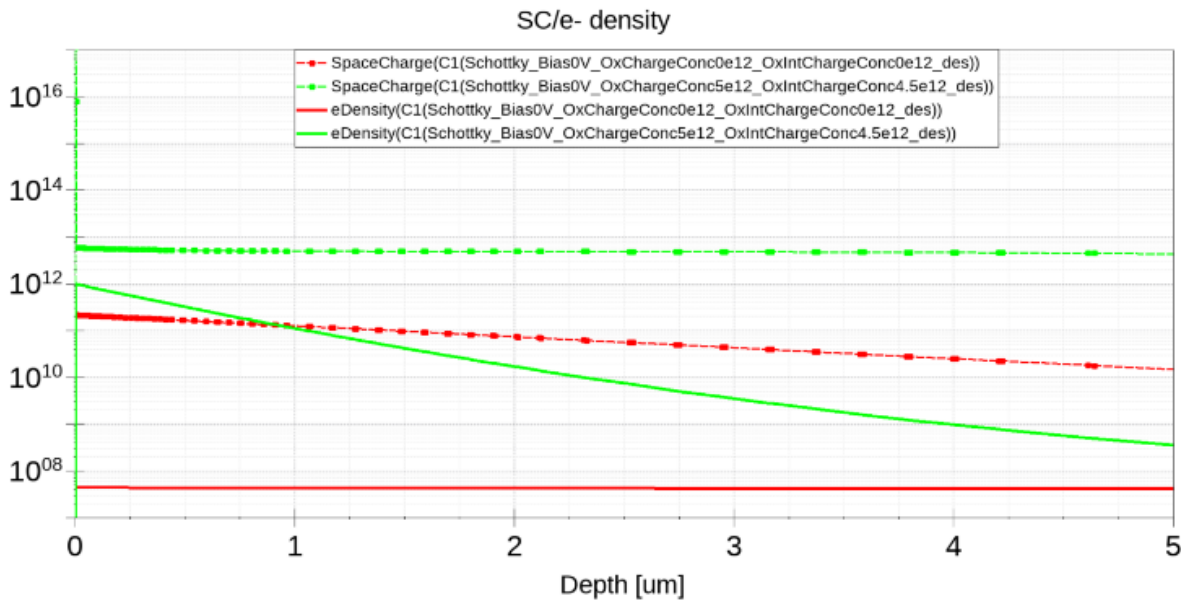
- ϕ_{bp} ~ 0.50-0.58 eV reported in literature



$CNL = 5.3\ [eV]$
$D = 1.5e-7\ [cm]$
$\mathrm{Nint} = 2.05e13\ [cm-2eV-1]$

TCAD: SiO_2 traps





Interface Defect	Level	Concentration	σ
Acceptor	E_C-0.4 eV	40% of acceptor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV
Acceptor	E_C-0.6 eV	60% of acceptor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV
Donor	E_V+0.7 eV	100% of donor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV

* ***Effects of Interface Donor Trap States on Isolation Properties of Detectors Operating at High-Luminosity LHC***, *DOI:* 10.1109/TNS.2017.2709815

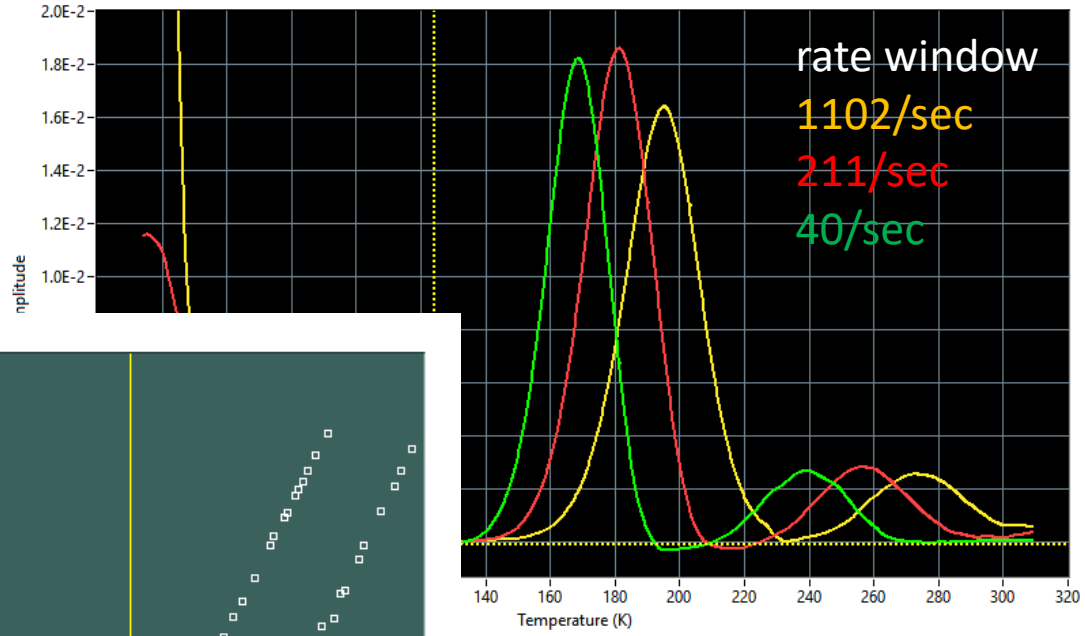
Fixed oxide-charge (**Oxch**) density and interface traps (**Oxint**) included Interface traps distributed among 3 energy levels, Gaussian , σ = 70meV Ratio Oxint/Oxch ~ 0.9

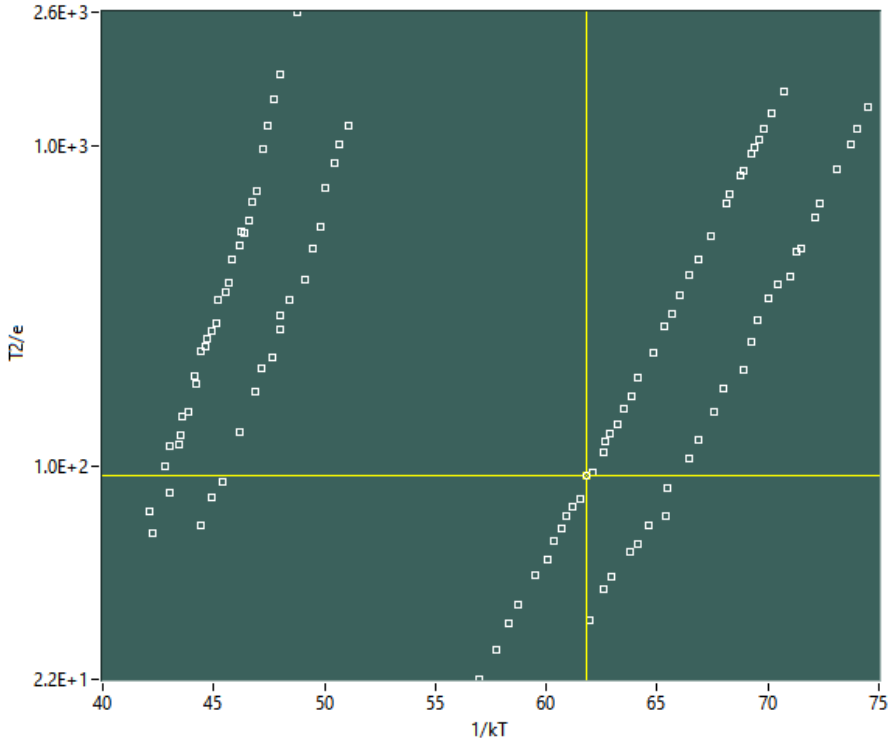
The presence of SiO2- Si interface states affects leakage current between Cath and GR

DLTS measurements: pn-junction diode @Semetrol

DLTS spectrum:

- 2 maxima
- analysis with Gaussian deconvolution
  ⇒ peaks contain 2 traps each





Vf=0V
tf=10ms
Vbias=-1V

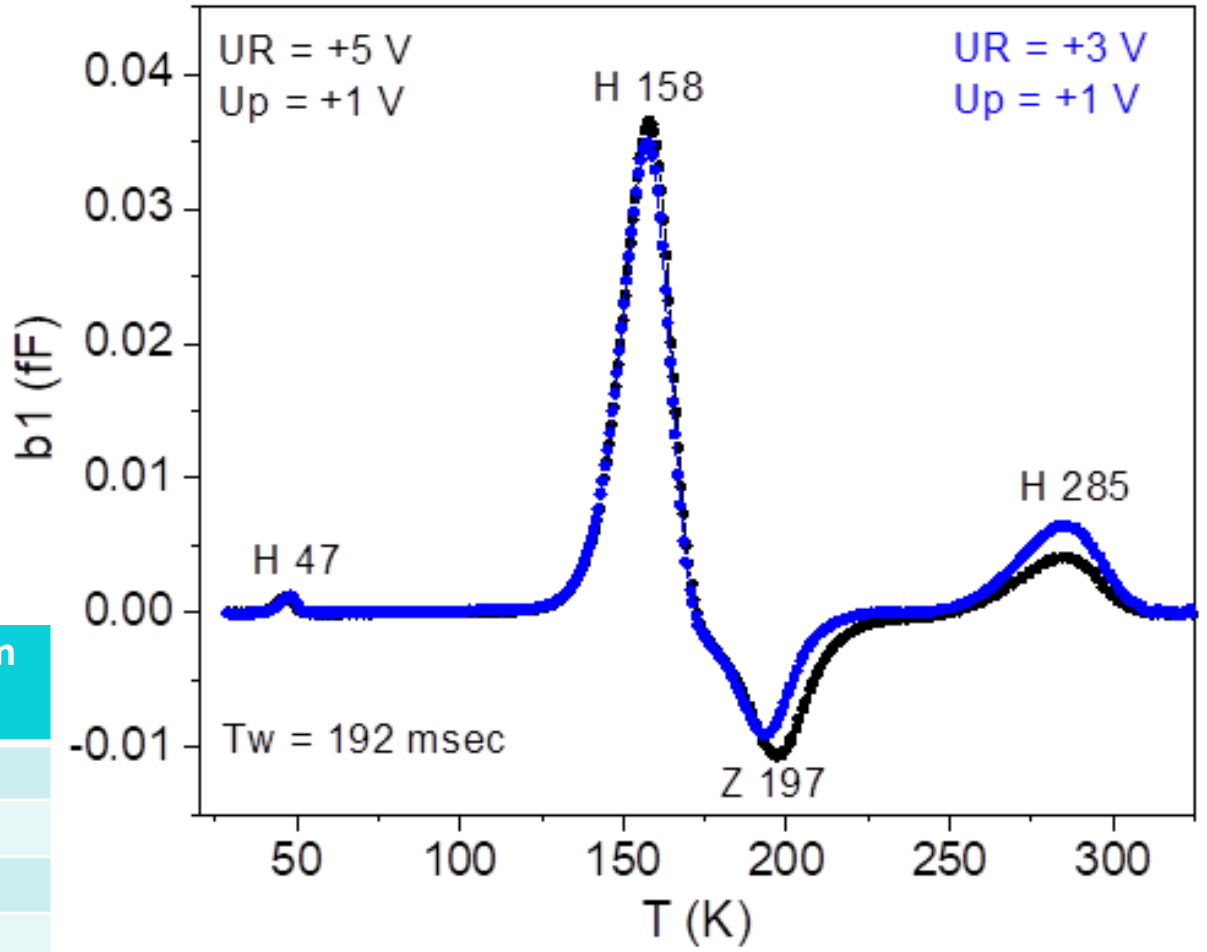
trap params from Arrhenius plot:

Midpoint temp (K)	E_t (eV)	Sigma (cm^2)	N_t/N_s
170.6	0.293	7.6E-16	9.7E-3
182.8	0.310	7.0E-16	2.1E-2
241.8	0.430	1.0E-15	7.6E-4
258.5	0.536	3.2E-14	3.5E-3

DLTS measurements: Schottky diode @Bucharest

DLTS spectrum:

- 3 maxima from hole traps
- 1 minimum, most likely from surface/interface states



trap parameters (Vbias=+5V; Vf=+1V):

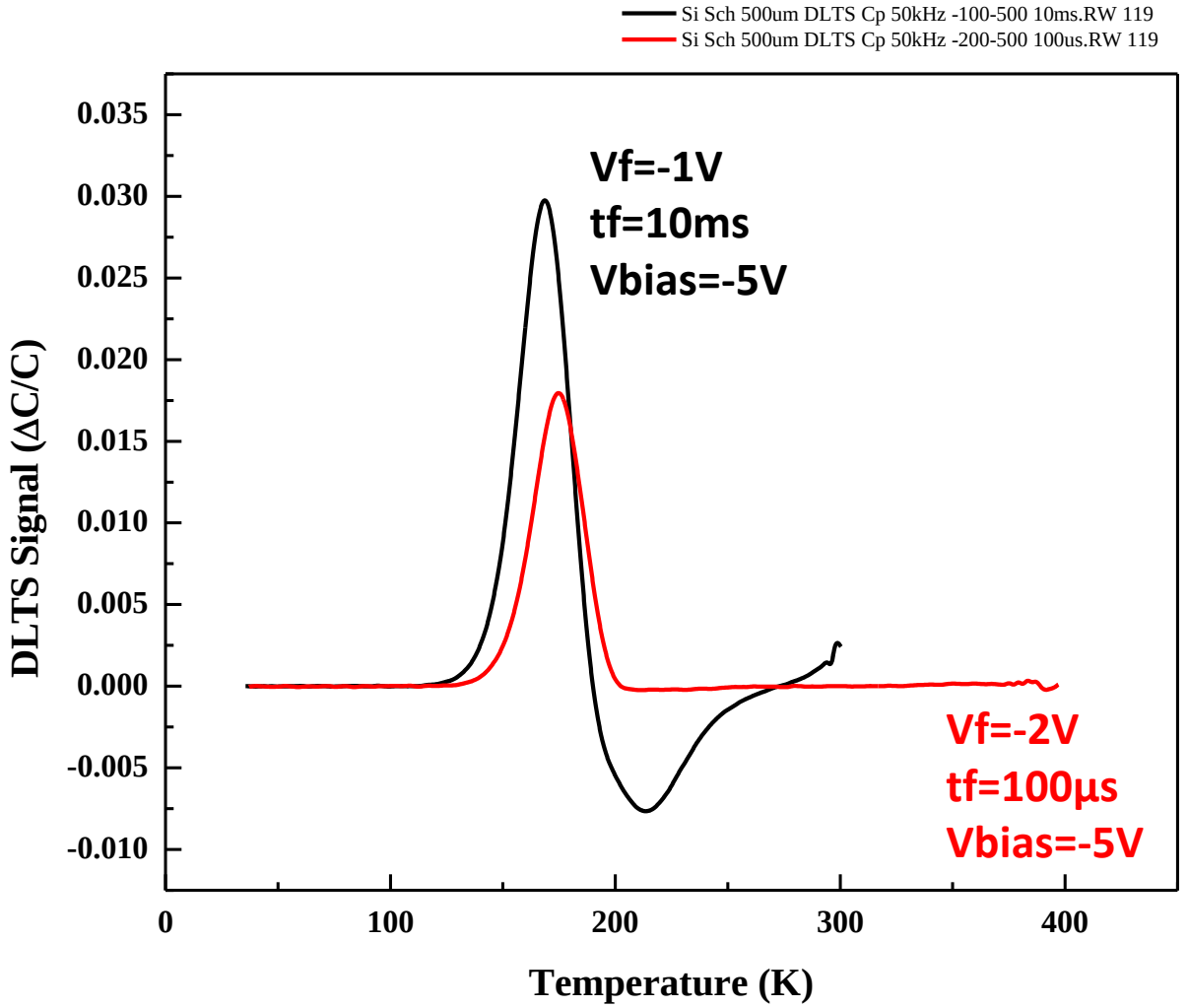
Defect	Temp (K)	Ea (eV)	Sigma (cm2)	Defect concentration (cm-3)
H47	47	0.069	6.87E-17	2.49E10
H158	158	0.294	4.35E-16	9.32E11
Z197	197	0.439	1.85E-14	2.90E11
H285	285	0.611	3.76E-15	1.32E11

DLTS measurements: Schottky diode @Semetrol

DLTS spectrum:

- peak with 2 majority carrier traps
- ‘minority’ carrier trap
  ⇒ vanishes for reduced + shorter filling pulse
  ⇒ surface/interface states likely
- large majority carrier trap for larger filling pulses at room temperature

Midpoint temp (K)	E_t (eV)	Sigma (cm^2)	N_t/N_s
170	0.312	5.5E-15	7.8E-3
180	0.294	3.3E-16	2.2E-2

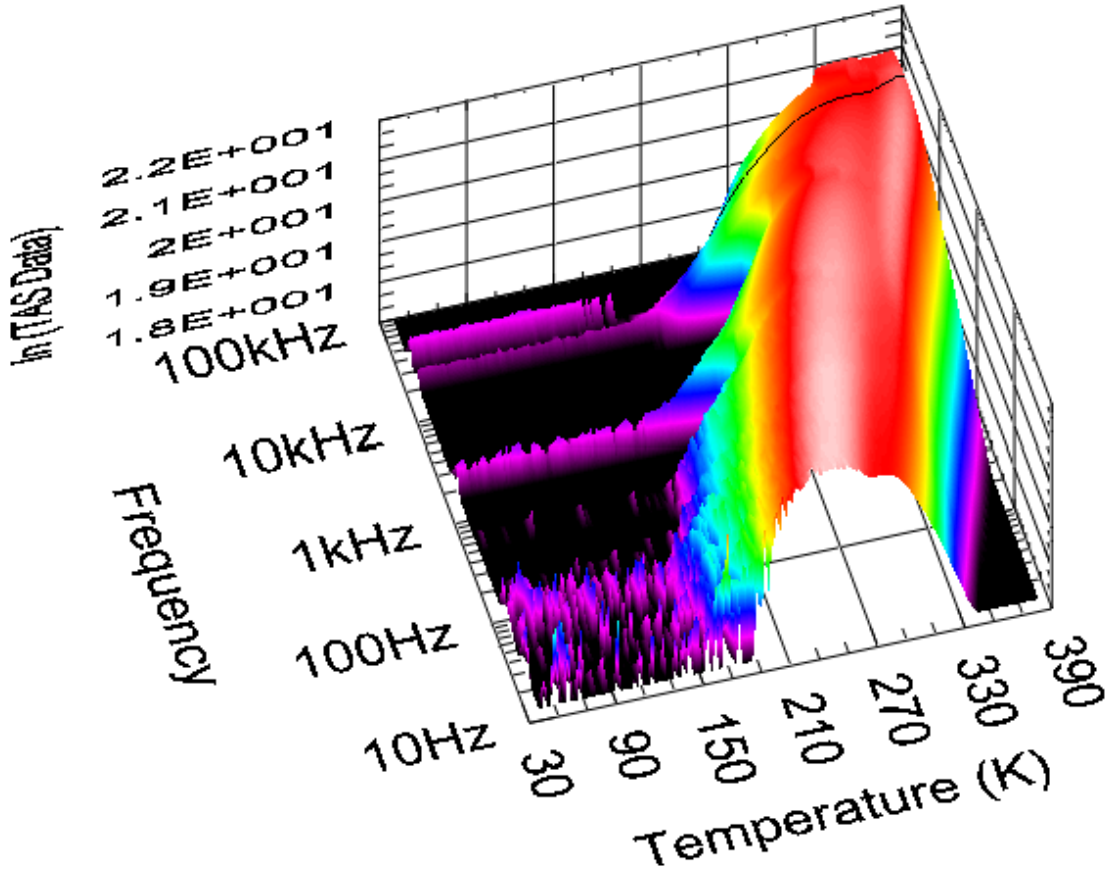


Thermal Admittance Spectroscopy (TAS)

- samples characterized with other spectroscopic techniques @Semetrol (DDLTS, IDLTS, IVT, PICTS, TAS)

<u>TAS:</u>

- measure capacitance C and conductance G as function of frequency and temperature
- defect contribution to C/G depending on test signal frequency and temperature
- steps in C or peak in G for thresholds
- steady-state measurement
- applicable for low-doped or high-resistivity materials, complements DLTS



Thermal Admittance Spectroscopy (TAS)

TAS analysis:

- higher trap energy in Schottky for similar peak
- second Schottky trap near mid-gap
- energy shift at different test voltages
  - field dependence of trap energy
  - might explain difference between Schottky and pn-junction (higher E-fields in pn diode)

Sample	V_{bias}	E_t (eV)	σ (cm^2)
PN	-1V	0.384	1.1E-16
Schottky	-1V	0.498	1.6E-14
Schottky	-2V	0.467	3.0E-15
Schottky	-1V	0.664	3.5E-13
Schottky	-2V	0.614	3.7E-14