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Evaluation of MOS and Gated Diode Devices of the ATLAS ITk Test Chip

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Presented on: 2021-11-19

Overview

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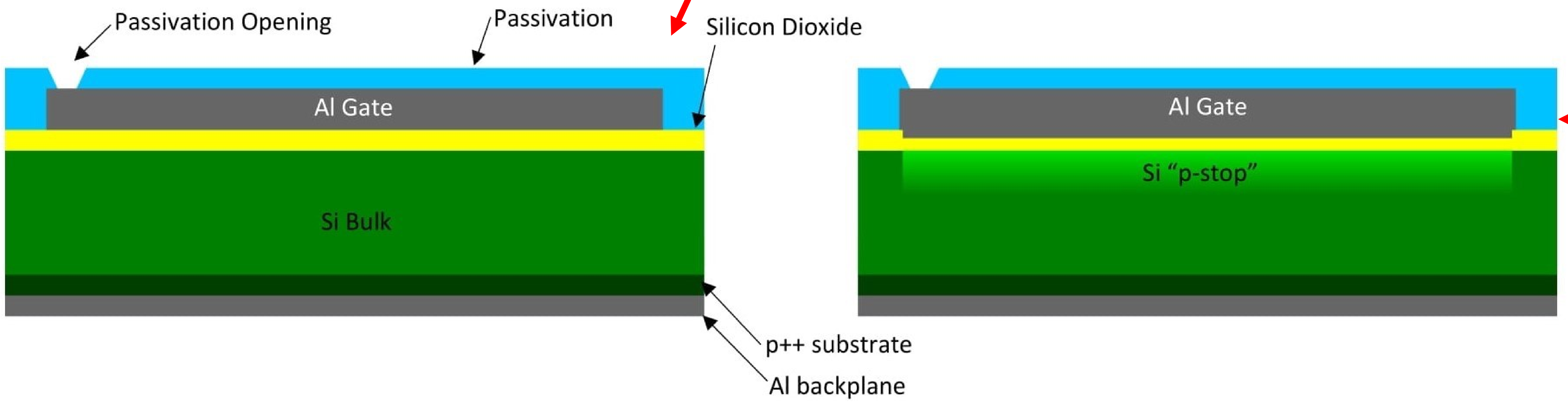
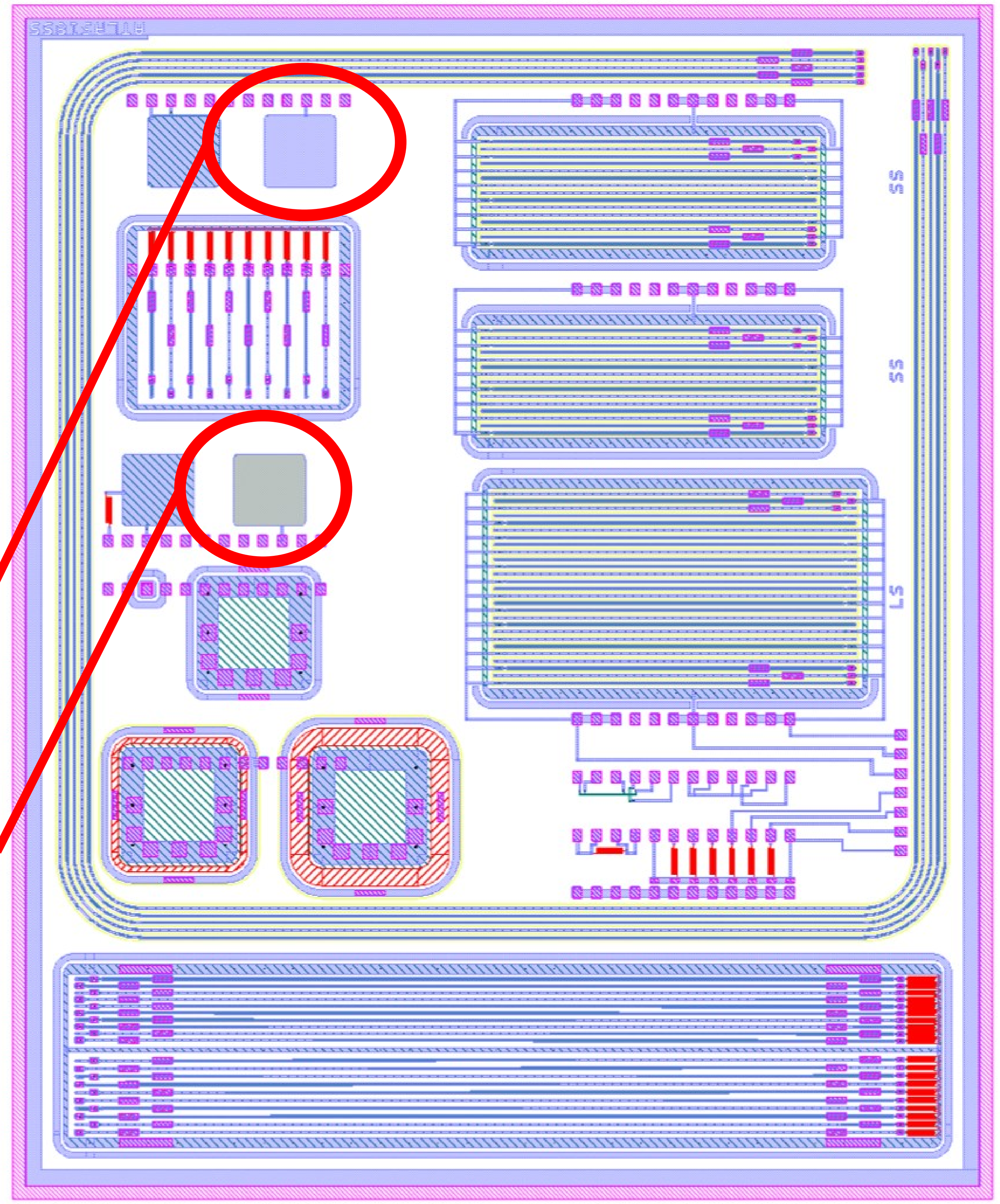
- MOS and GCD devices implemented in the ATLAS test chip
- Investigated suitability of these devices for QA of ITk strip sensors
- Description of device design and intended use/goals
- Test procedures along with results (large number of statistics for MOS device)
- GCD design discussion
- Gamma irradiated samples and samples with special processing

The MOS Device

- Two MOS devices -> with and without p-stop “implant”
- Both have total gate area 0.556mm^2
- Al gate material is the same as the readout strips in ITk sensor
- Same Si bulk as the ITk strip sensor: $N_A = 4\times10^{12} cm^{-3}$
- P-stop implant shares same doping profile as p-stop implemented in main sensor for strip isolation





The GCD Device

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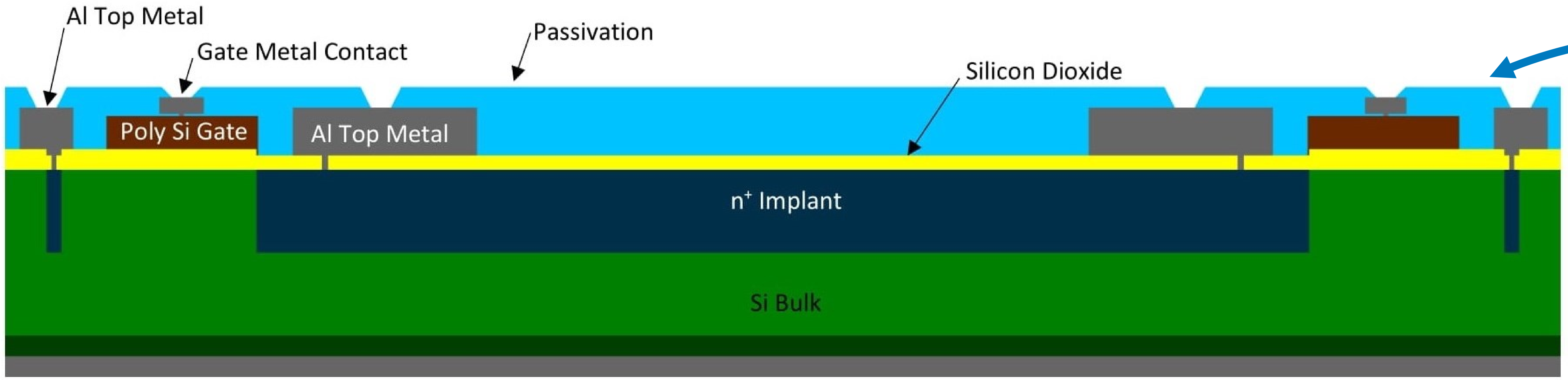
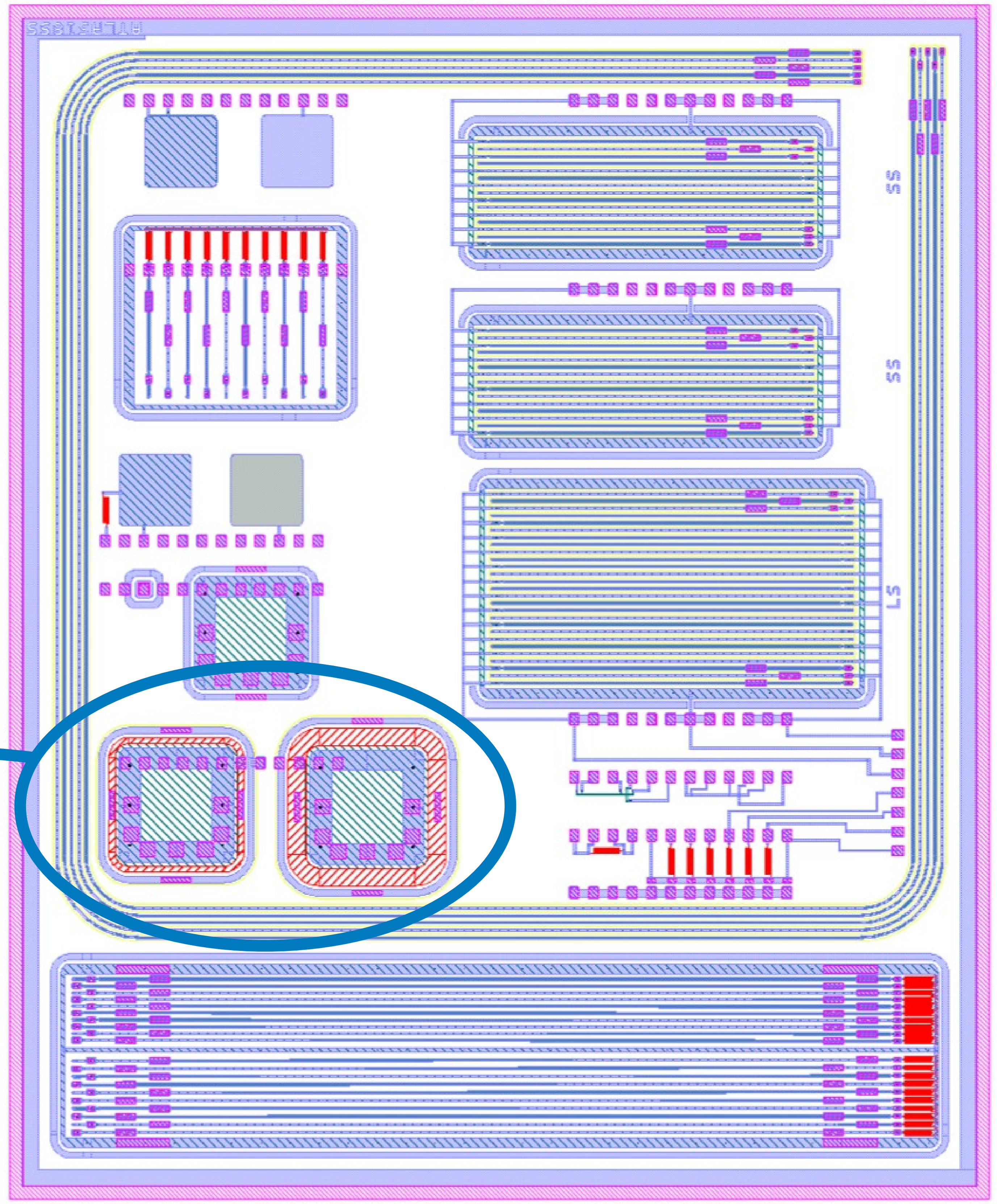
- Two GCD devices -> two different gate widths (areas): 0.183mm (0.988mm^2) or 0.063mm (0.316mm^2)
- Each have 1.597mm^2 n$^+$ diode implant and surrounded by a 18um wide guard ring implant (same n$^+$ as diode)
- poly-Si gate material

Large gate device, to scale in horizontal axis (vertical axis arbitrary)





Device Characteristics

- Extract the oxide capacitance and oxide thickness from the MOS in strong accumulation; treating accumulated MOS like parallel plate capacitor:

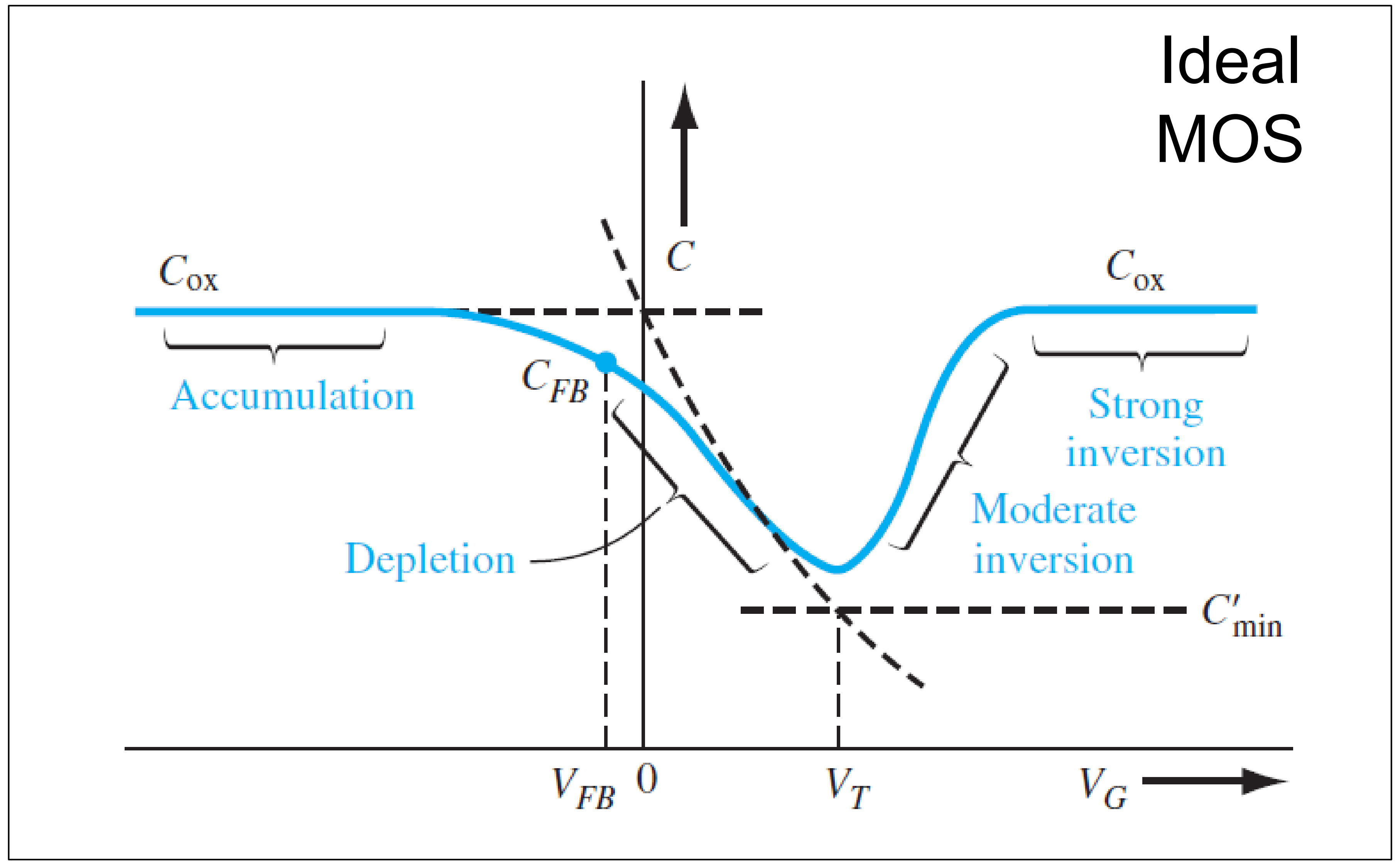
$$C_{ox} = C(-20V) \quad ; \quad t_{ox} = \frac{A\epsilon_{ox}}{C_{ox}}$$

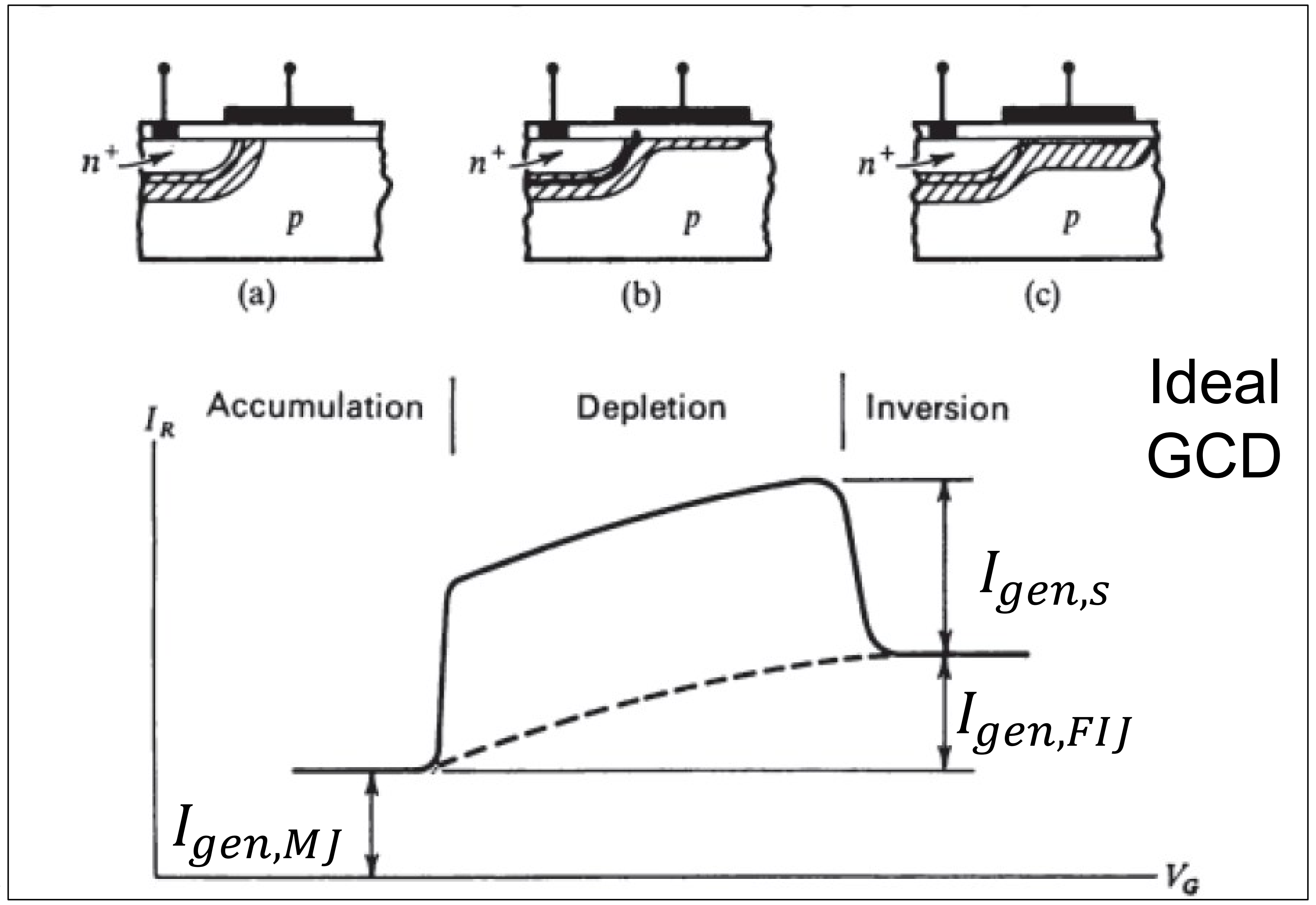
- Use flatband capacitance method to extract flatband voltage:

$$\frac{1}{C_{fb}} = \frac{1}{C_{ox}} + \frac{\lambda_d}{A\epsilon_{Si}} \quad ; \quad \lambda_d = \sqrt{\frac{\epsilon_{Si}kT}{q^2 N_A}} \quad ; \quad C_{fb} = C(V_{fb})$$

- Extract surface recombination velocity and test suitability for capacitive measurements:

$$I_{gen,s} = \frac{1}{2} q n_i s_o A_s \quad \rightarrow \quad s_o = \frac{2I_{gen,s}}{q n_i A_s}$$





Goals

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- Quality Assurance (QA) program is already in place for ITk Strip Sensor production -> Monitor consistency of sensor manufacturing and study effects of radiation without sacrificing main sensors

- Each device can be used in QA program:
  - MOS -> oxide thickness should be consistent across many wafers
  - MOS -> measured flatband voltage used to characterize surface damage due to ionizing radiation ie. increased positive space charge in oxide
  - GCD -> surface reco. velocity used to further characterize surface damage due to ionizing radiation ie. increased fast surface states
  - GCD -> can also be used for capacitive measurements similar to MOS (e.g. with diode and guard ring floating)

- Should establish test procedures for each of these devices and threshold recommendations for the QA program

MOS Test Procedure

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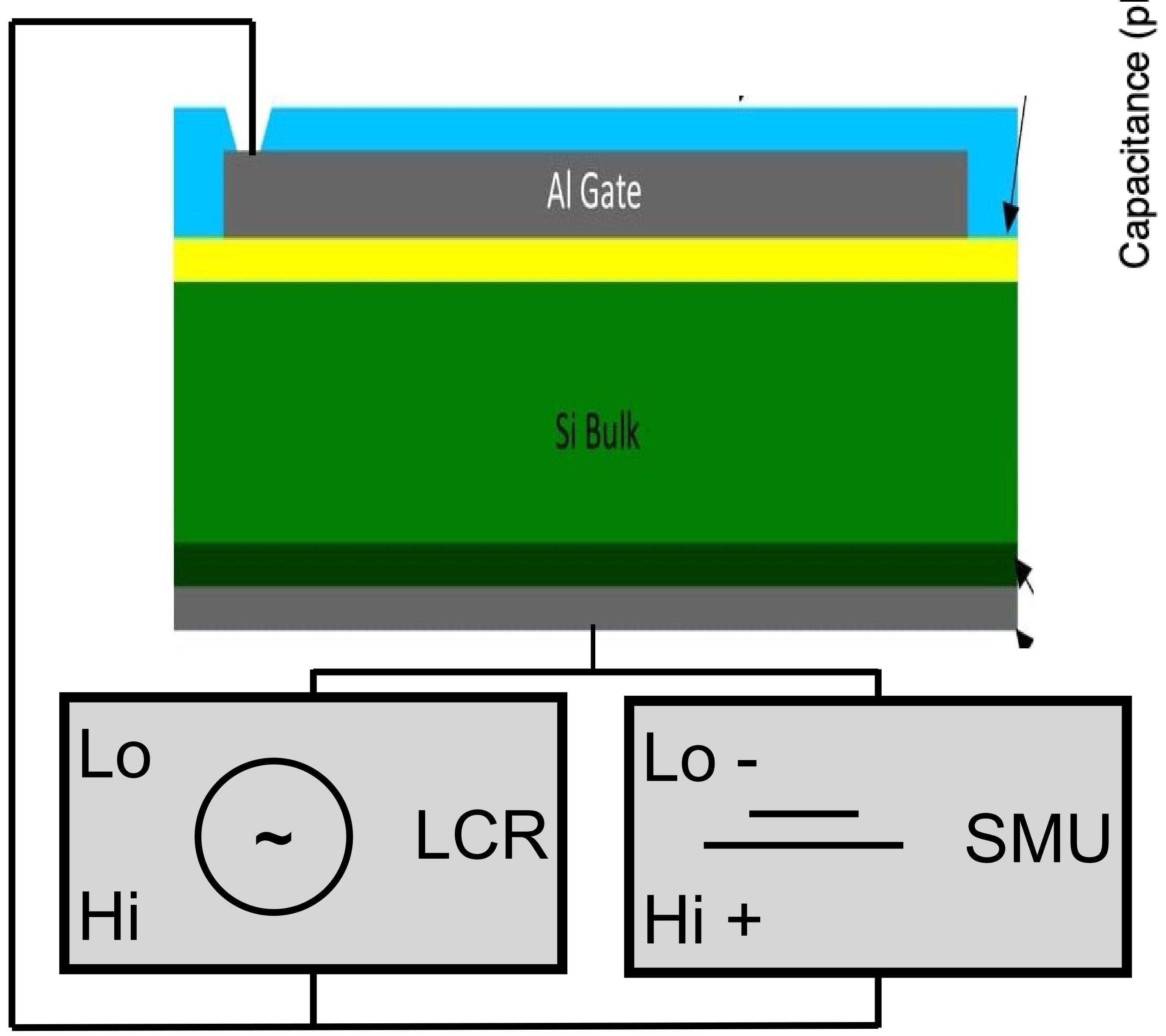
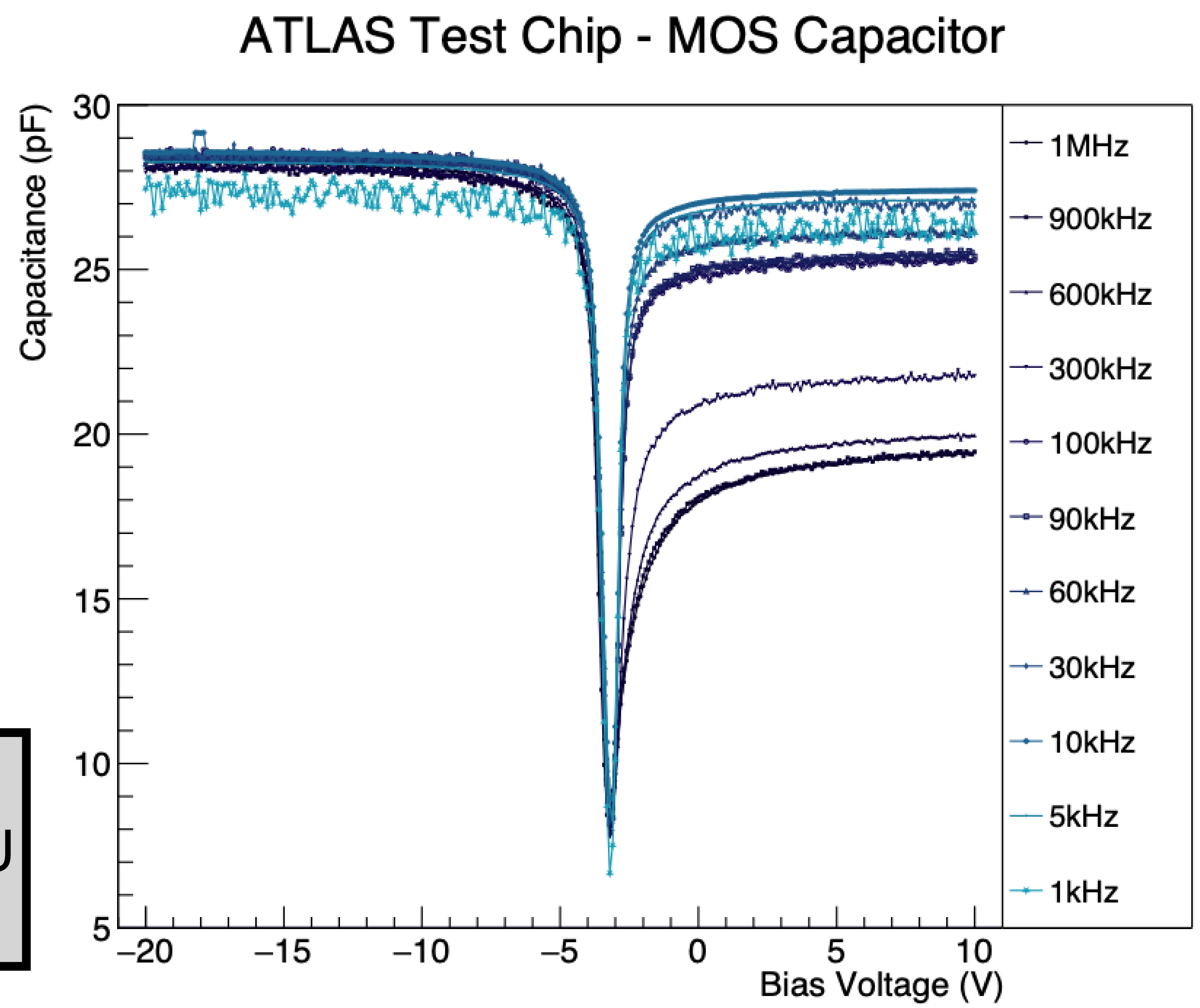
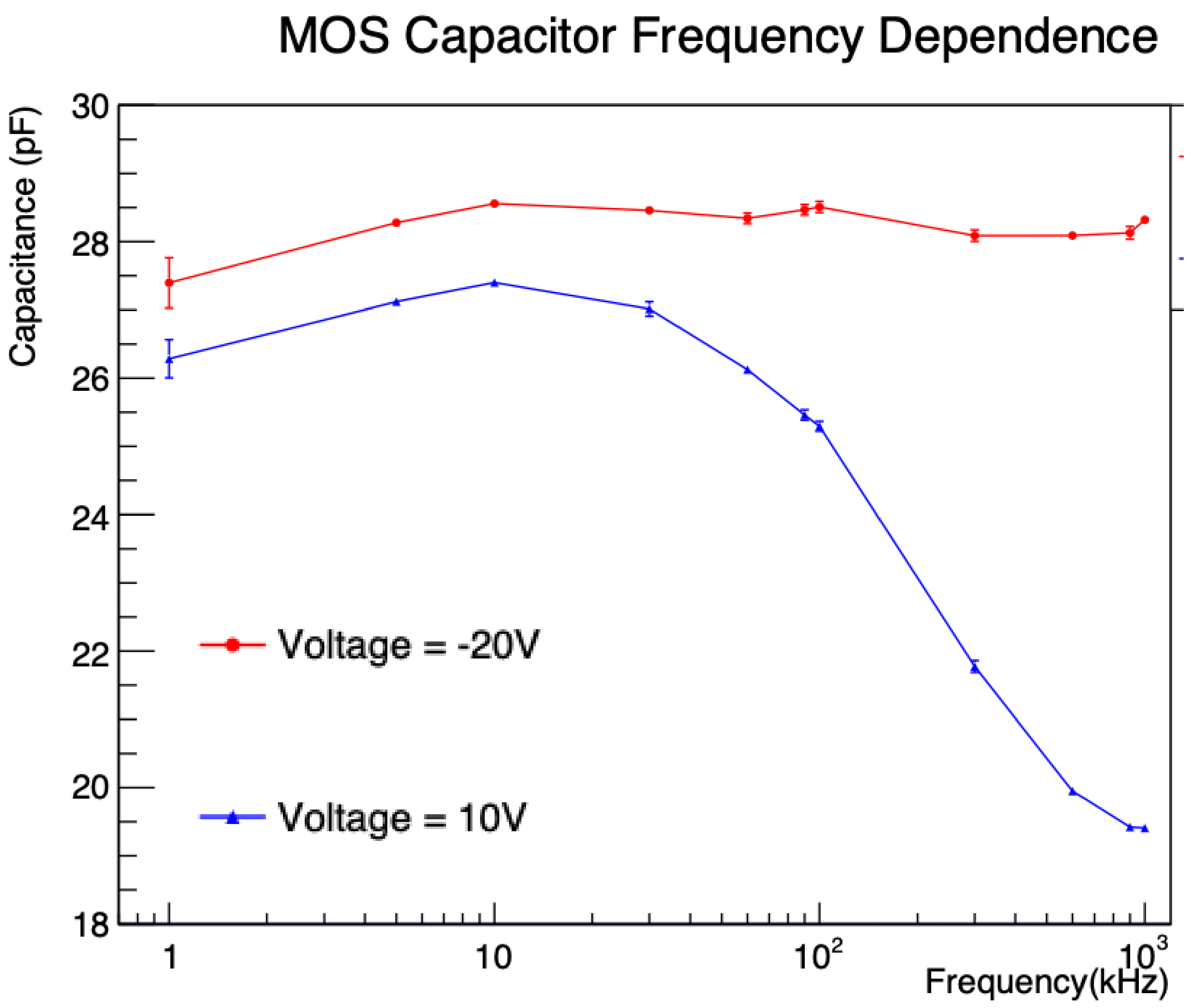
- Backplane held at ground, scan gate voltage from inversion to accumulation (+2V to -20V) in 0.1V steps
- LCR meter measures capacitance at each voltage step. RC modelled in series, sourcing 100mV, 10kHz AC test signal
- Procedure adjusted for Gamma Irradiated samples (see slide 16)







Statistics of the MOS Device

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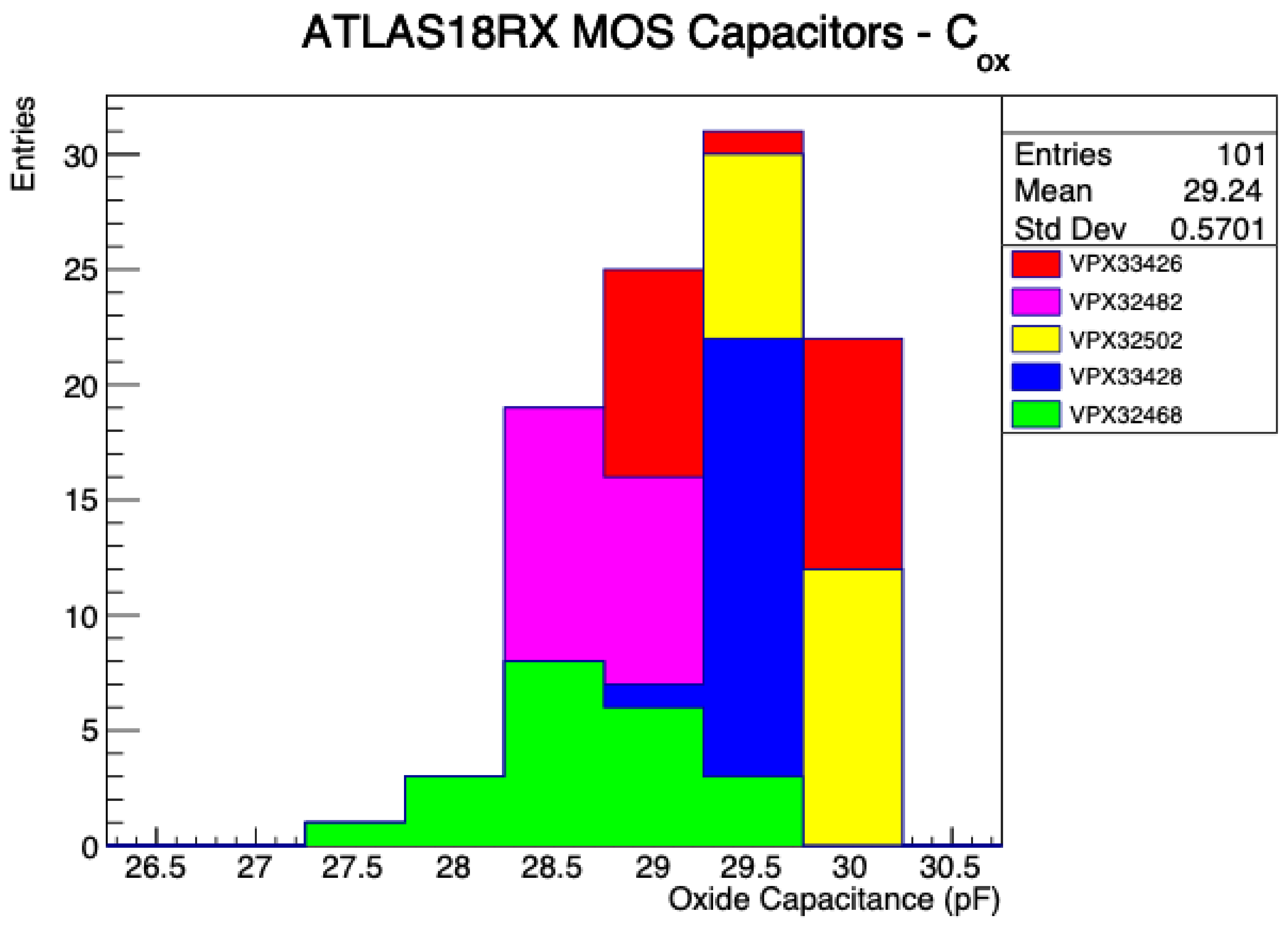
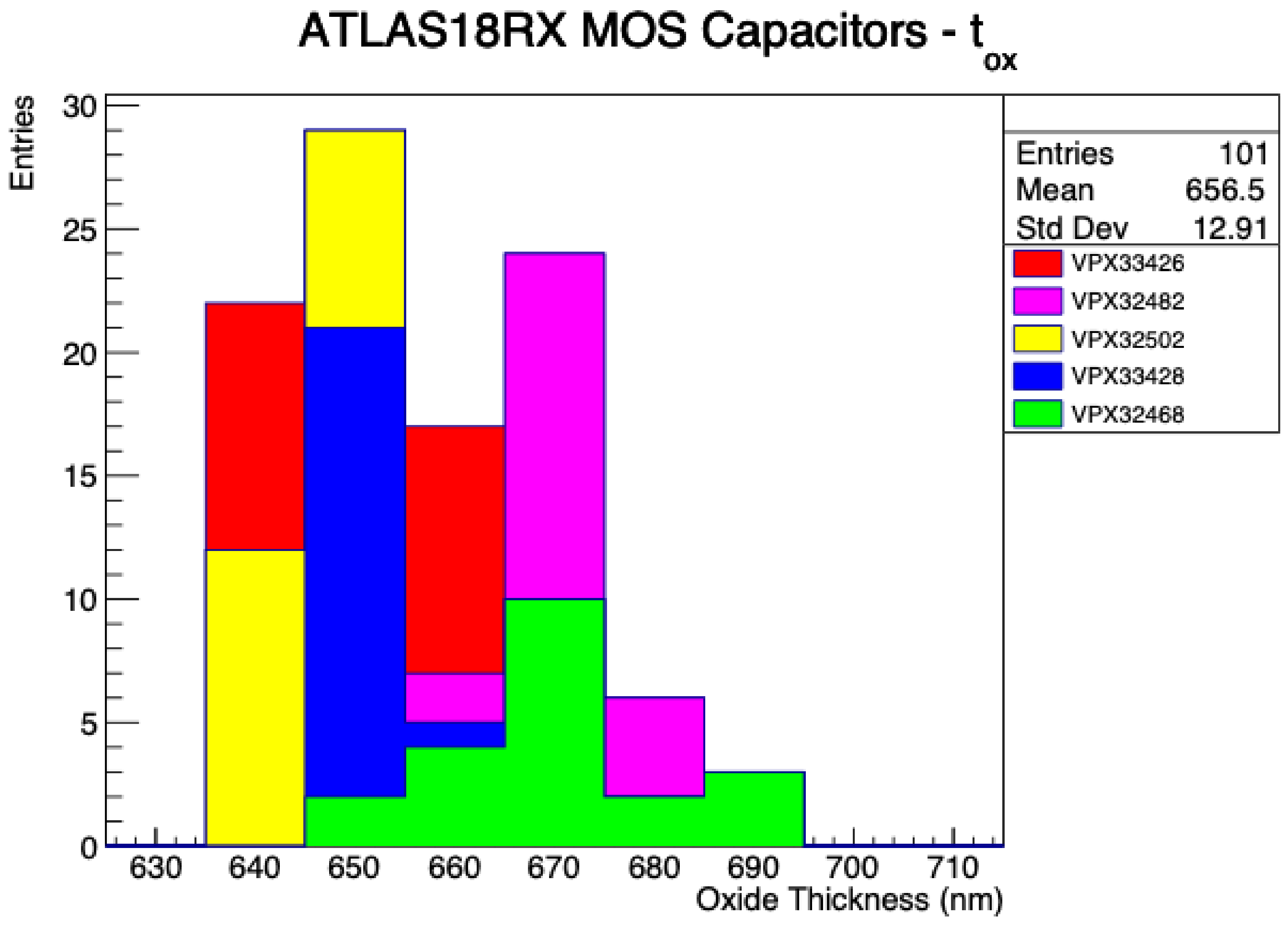
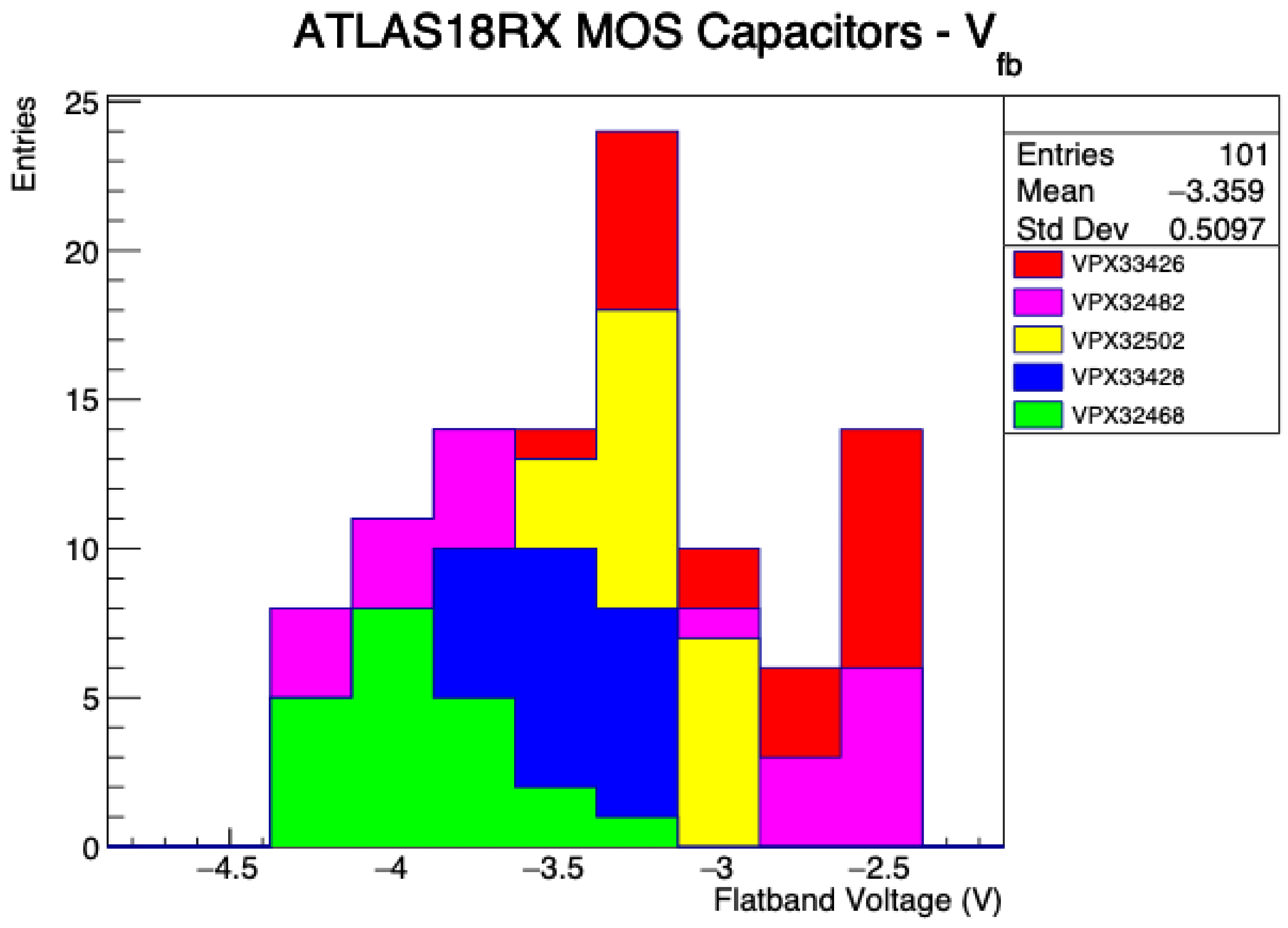




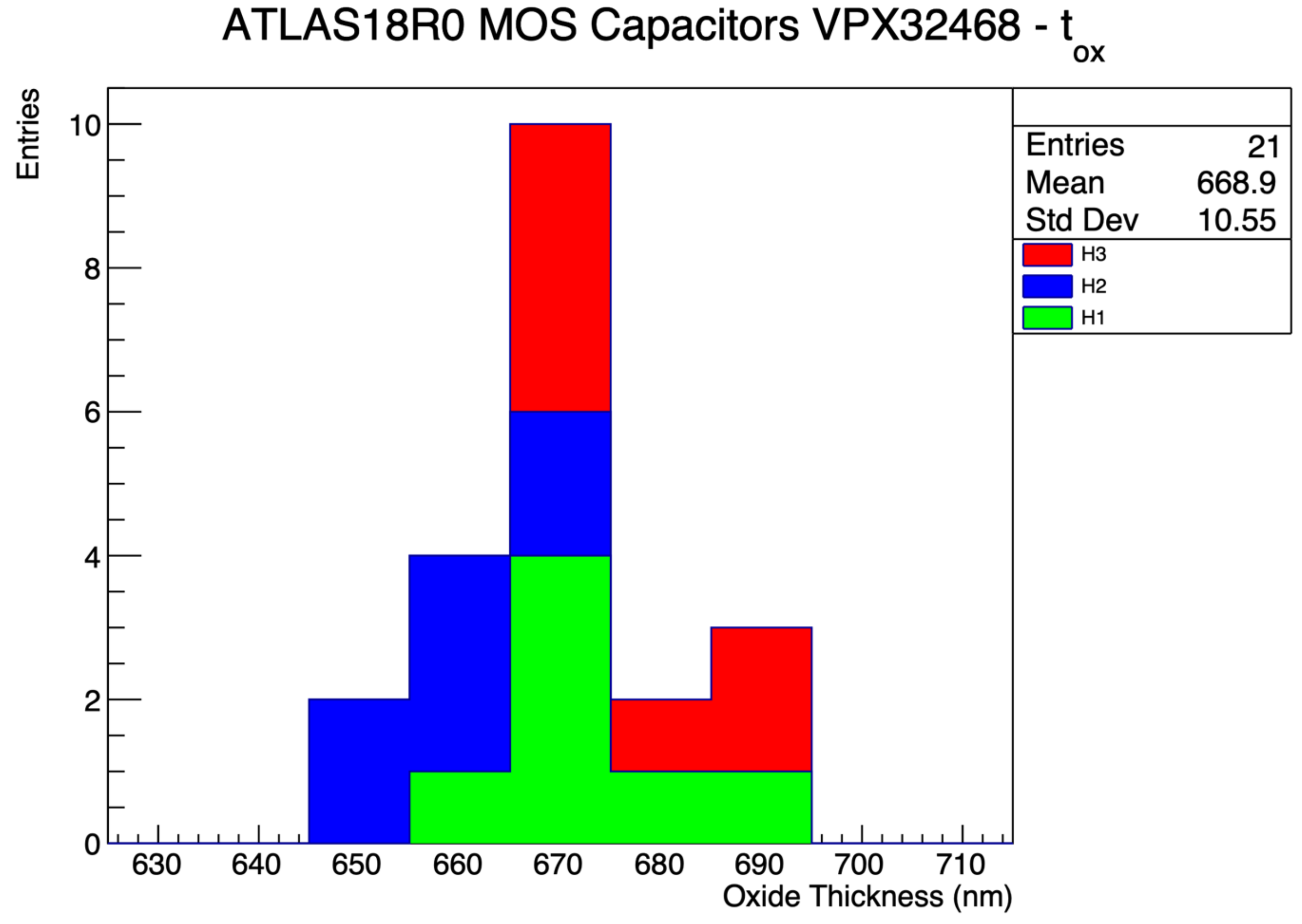


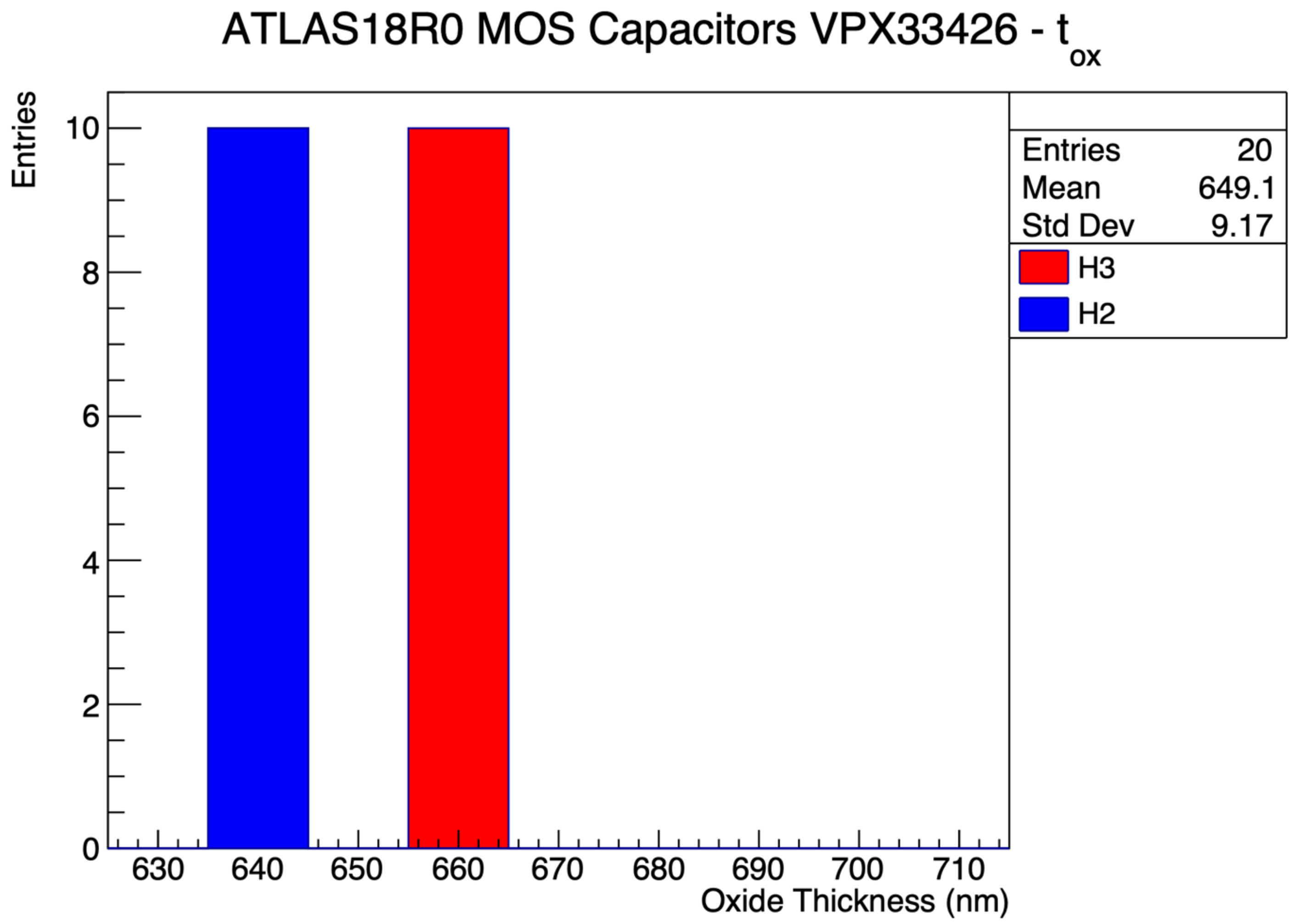
- Colours represent five pre-production batches sampled ~20 from each
- Batch-by-batch breakdown in following slides

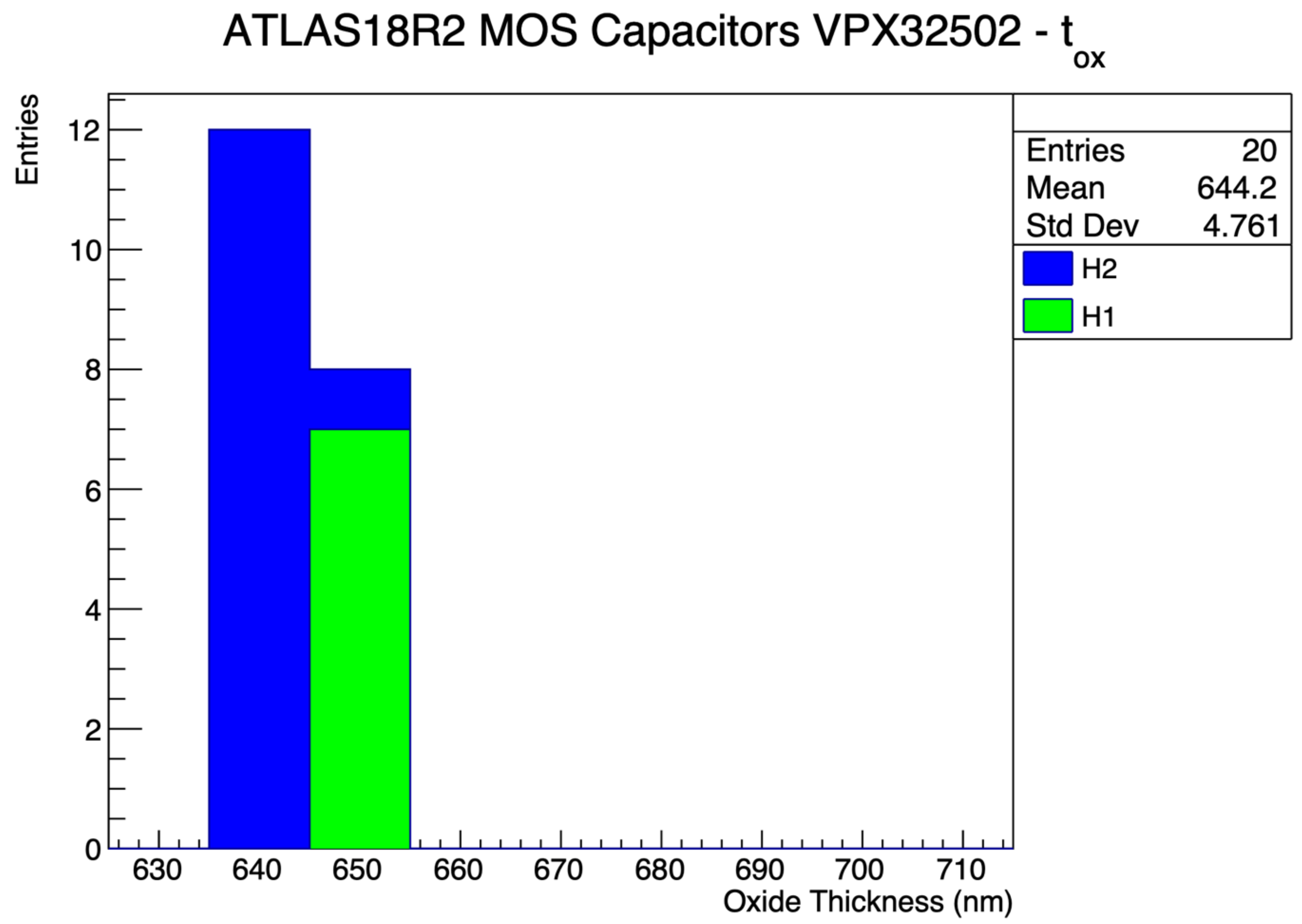
t_{ox} by Batch

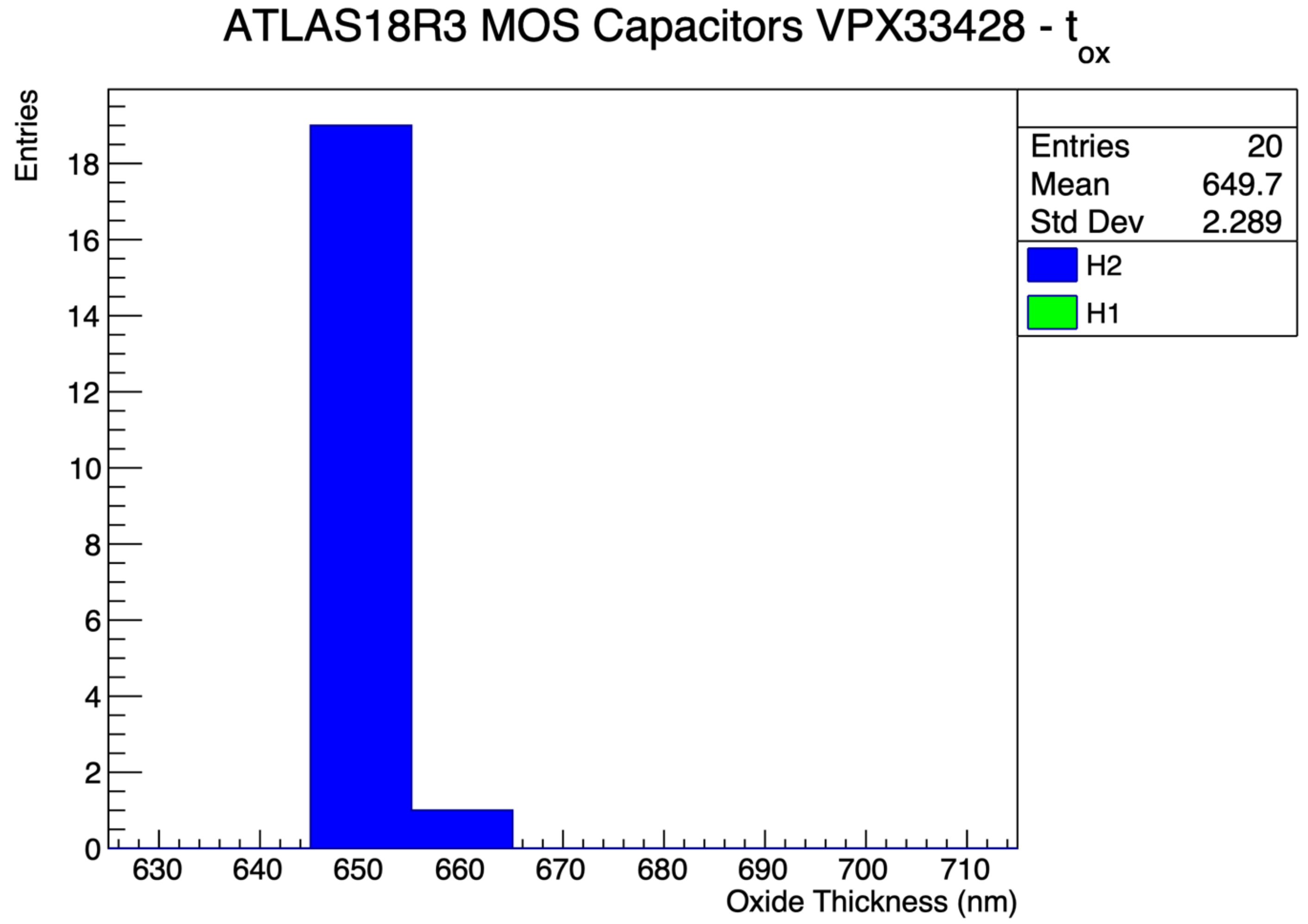
$$t_{ox} = \frac{A\epsilon_{ox}}{C_{ox}}$$

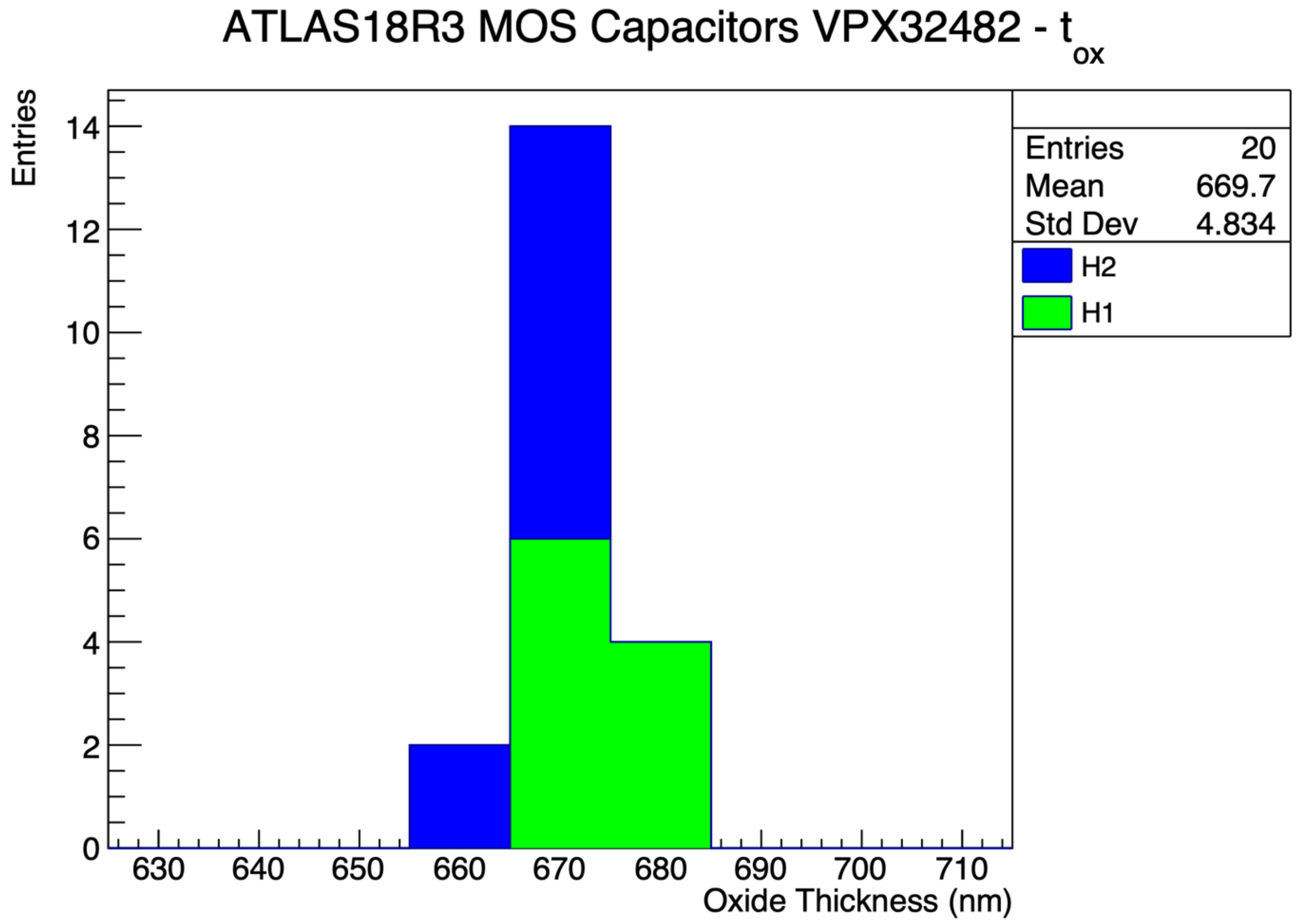
"Left-to-right" trend → Oxide is generally thicker on right side of wafer

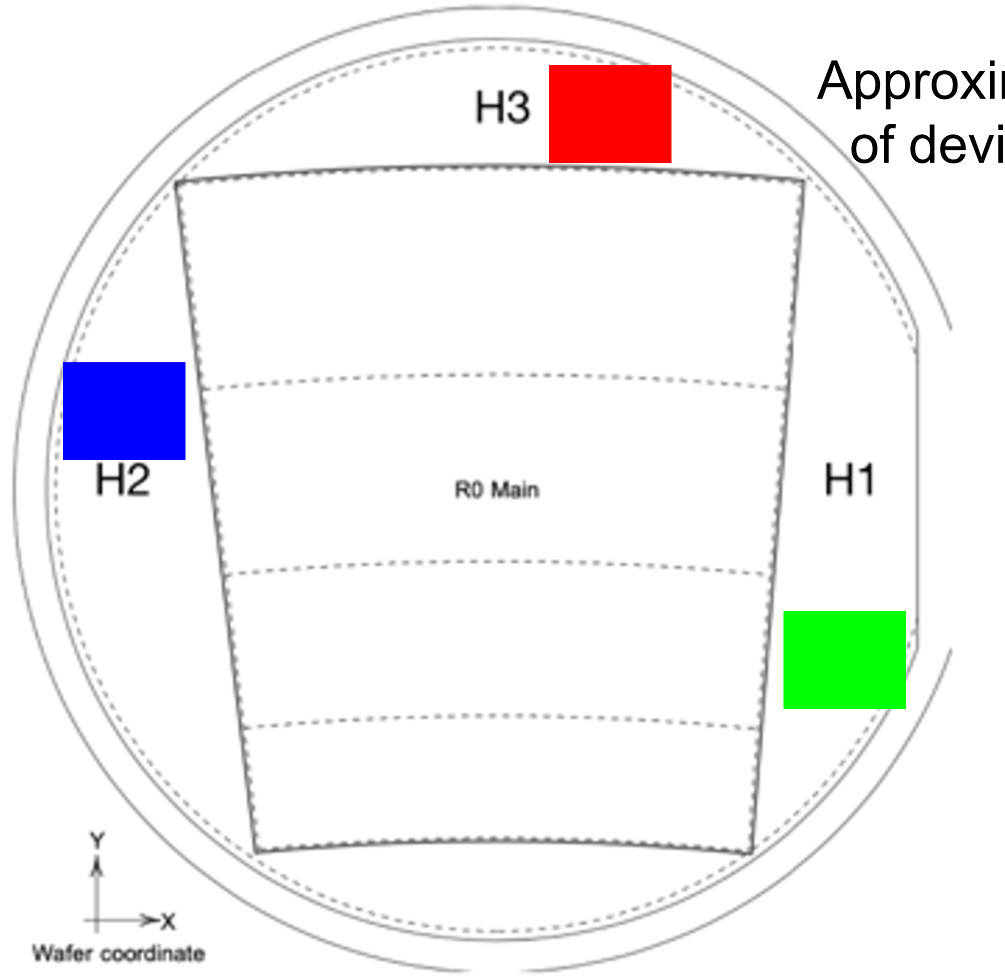








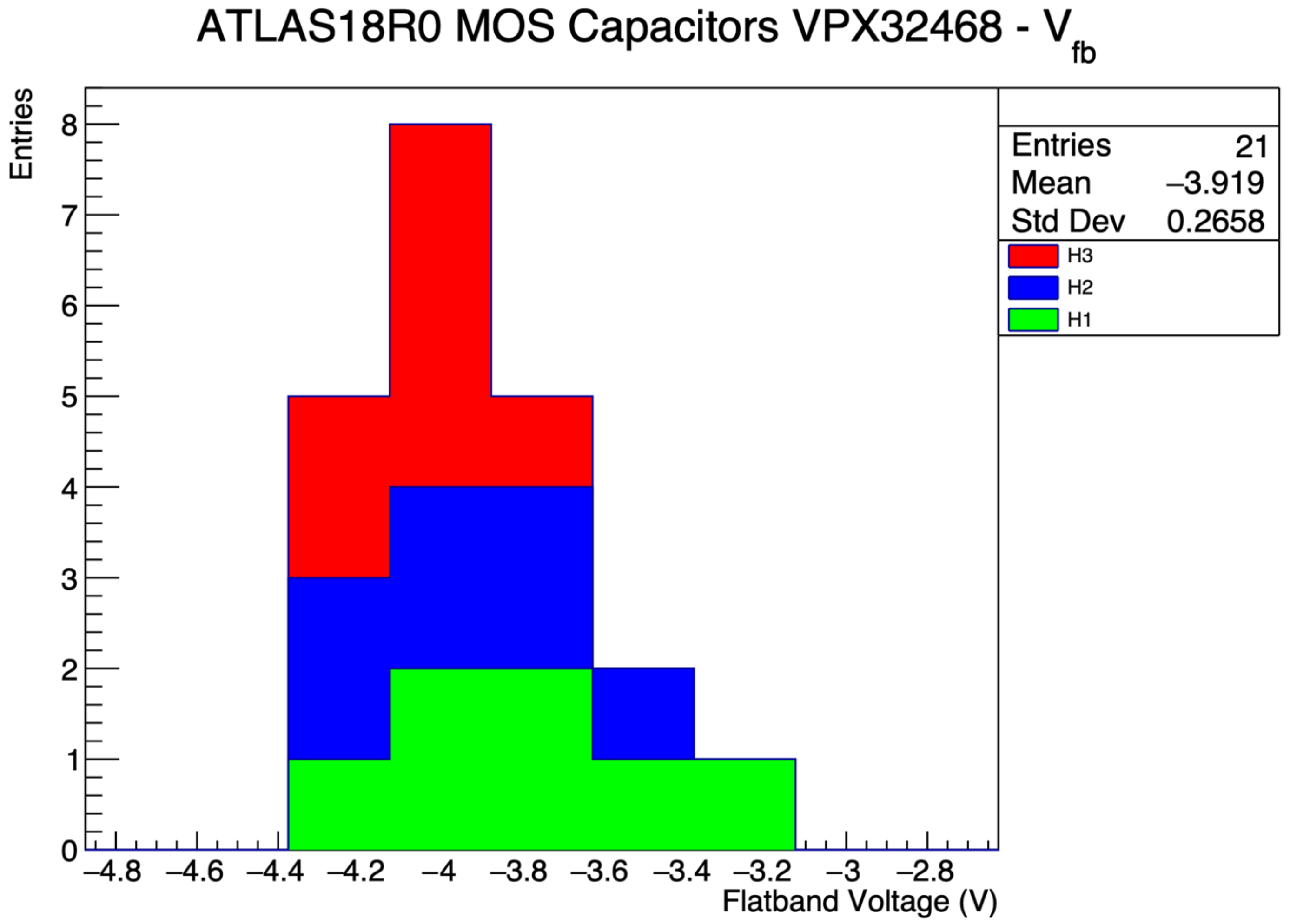


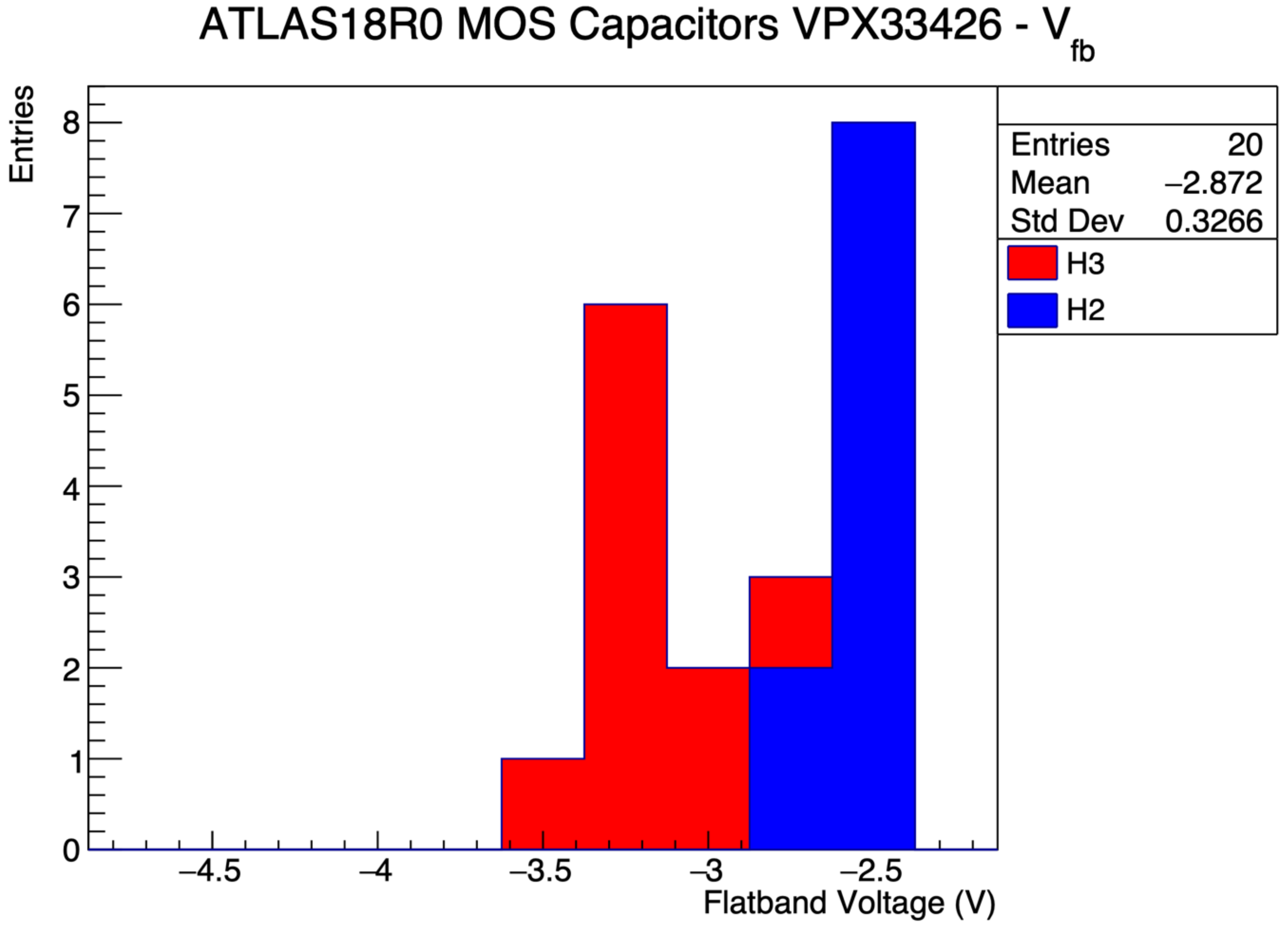


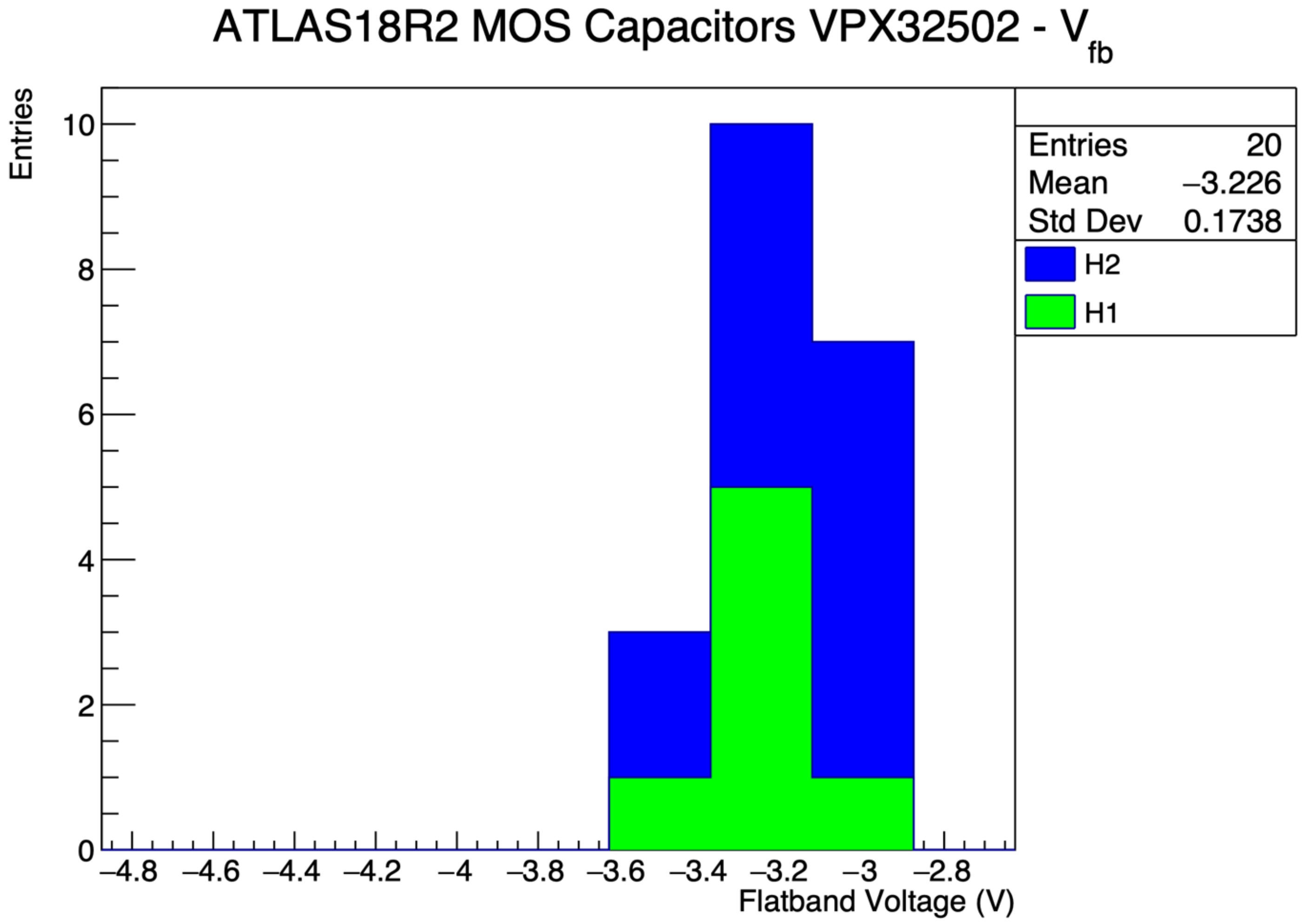
Approximate location of device on wafer

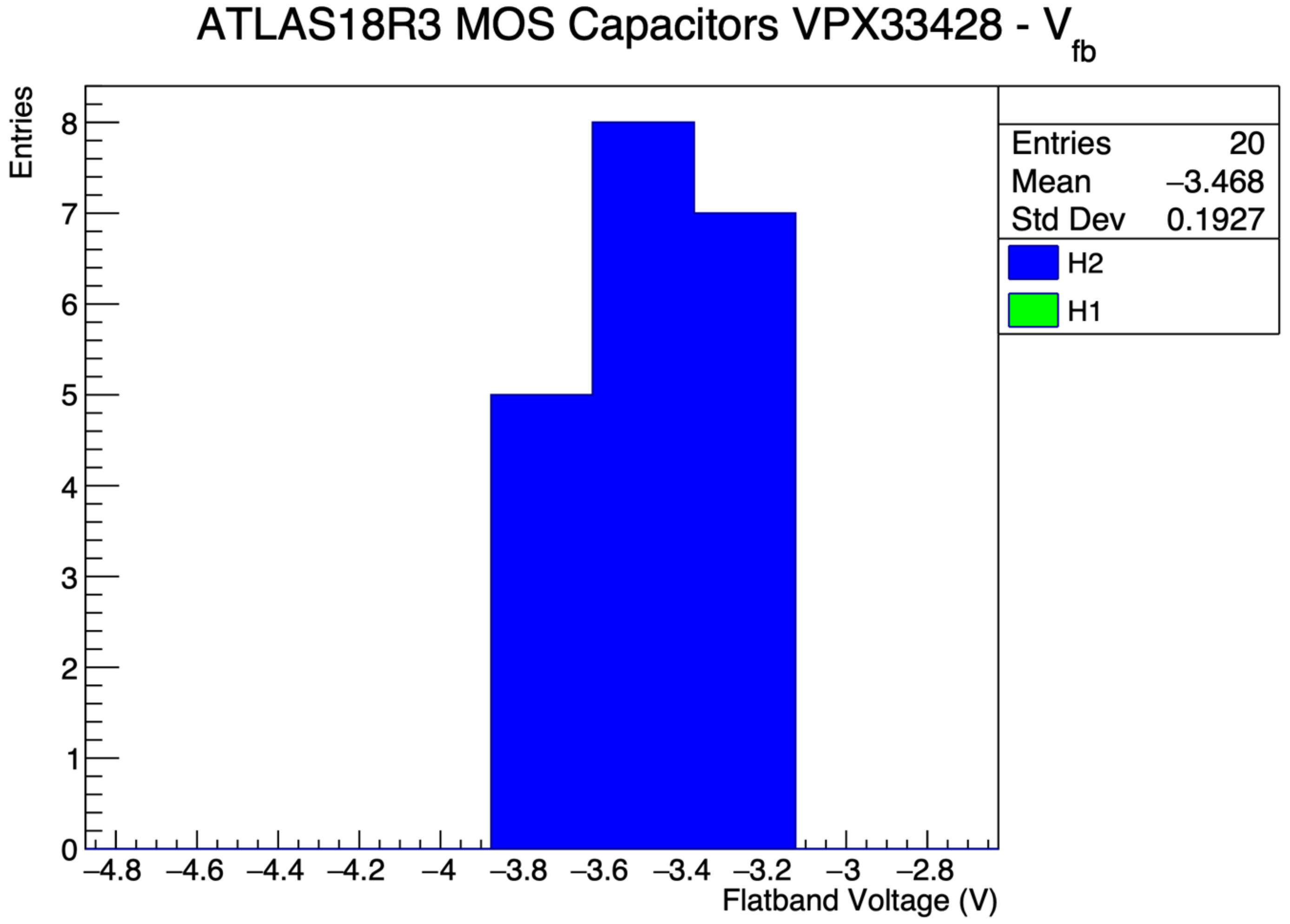
V_{fb} by Batch

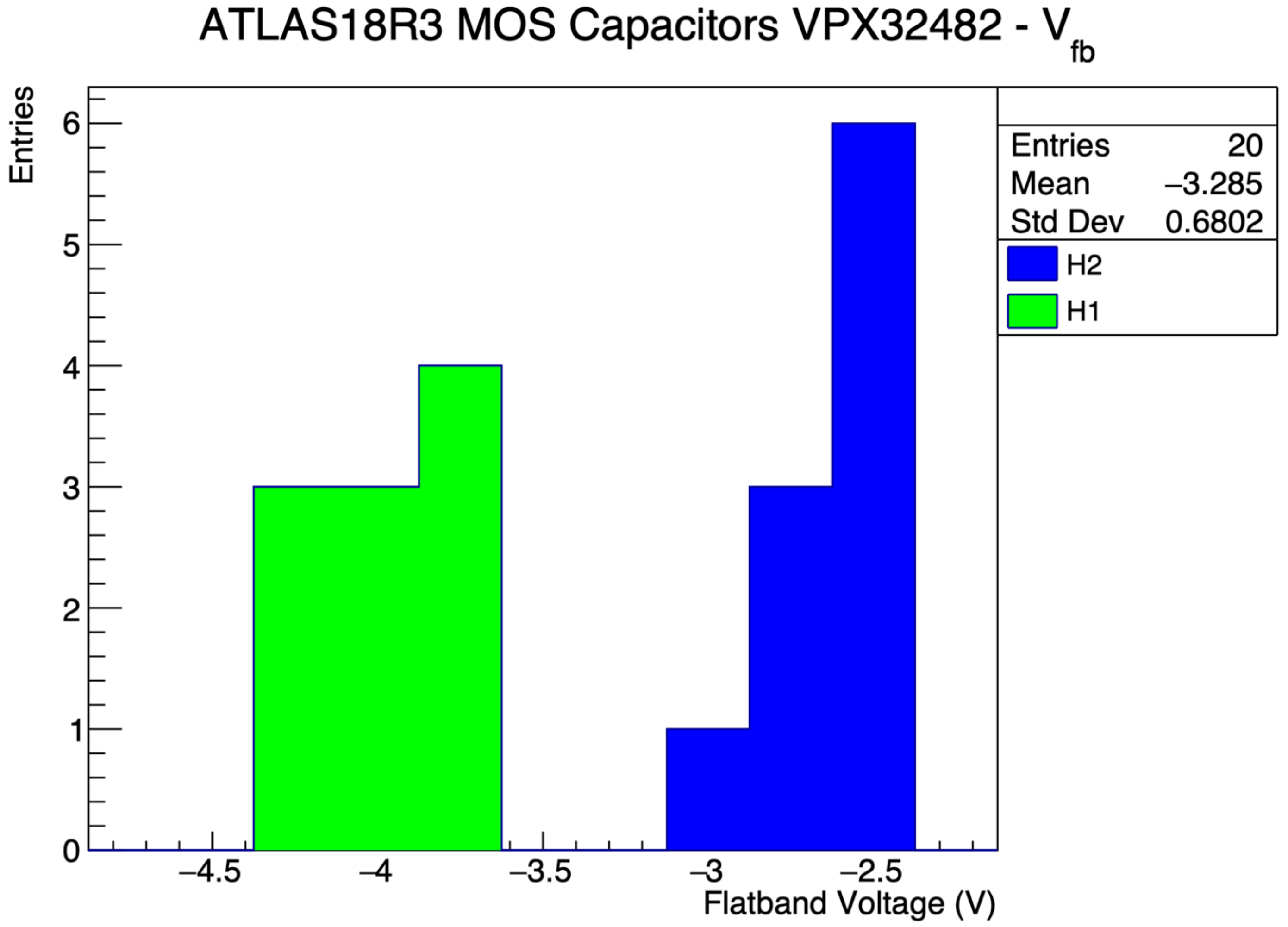
“Left-to-right” trend → more positive space charge in right side of wafer

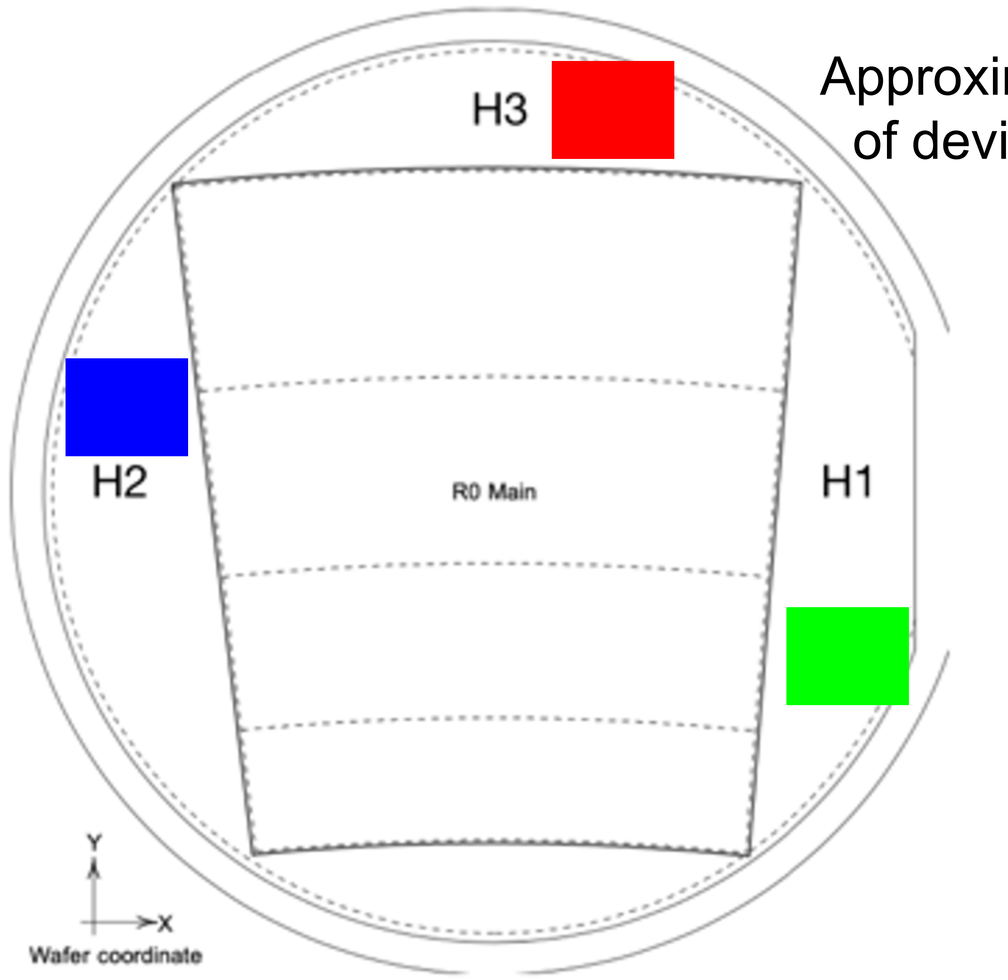












Approximate location of device on wafer

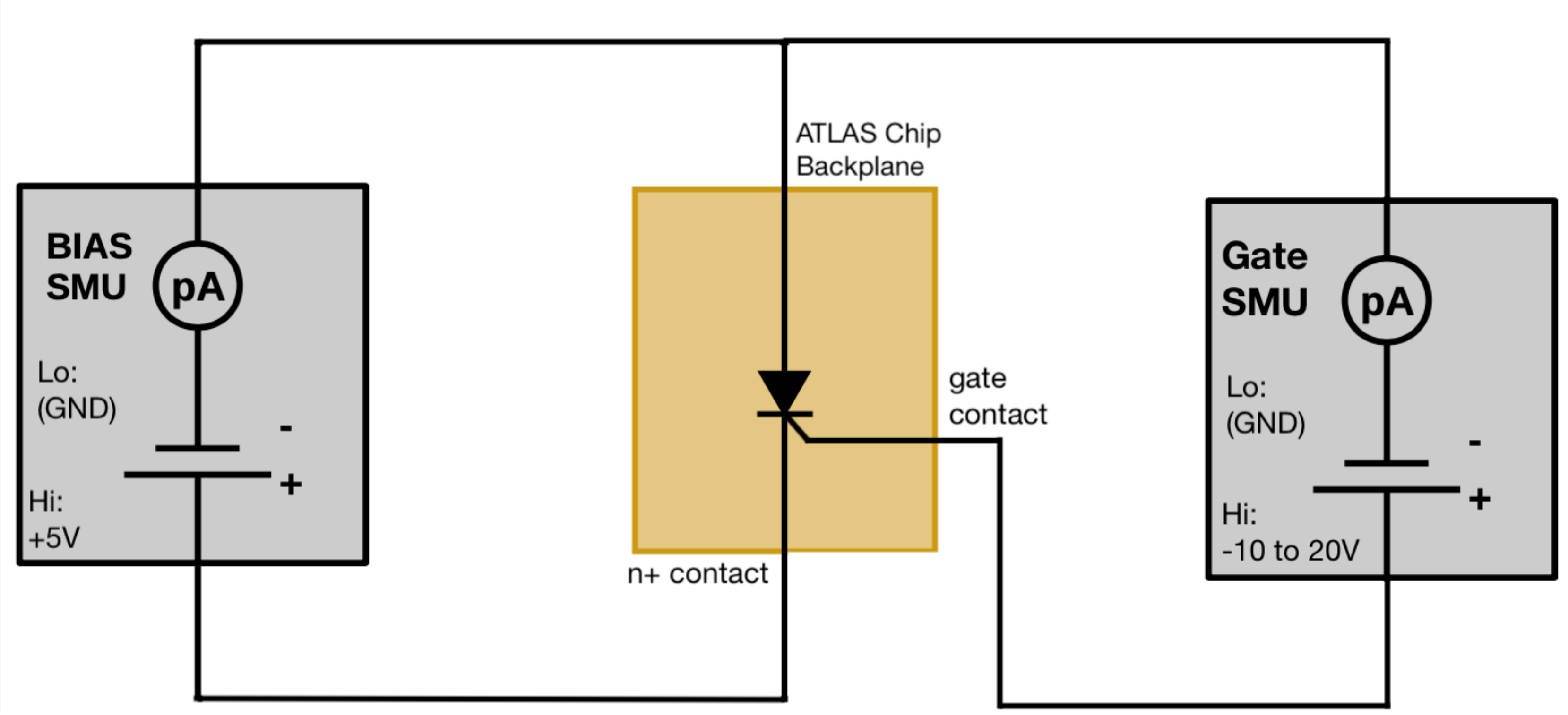
GCD Test Procedure

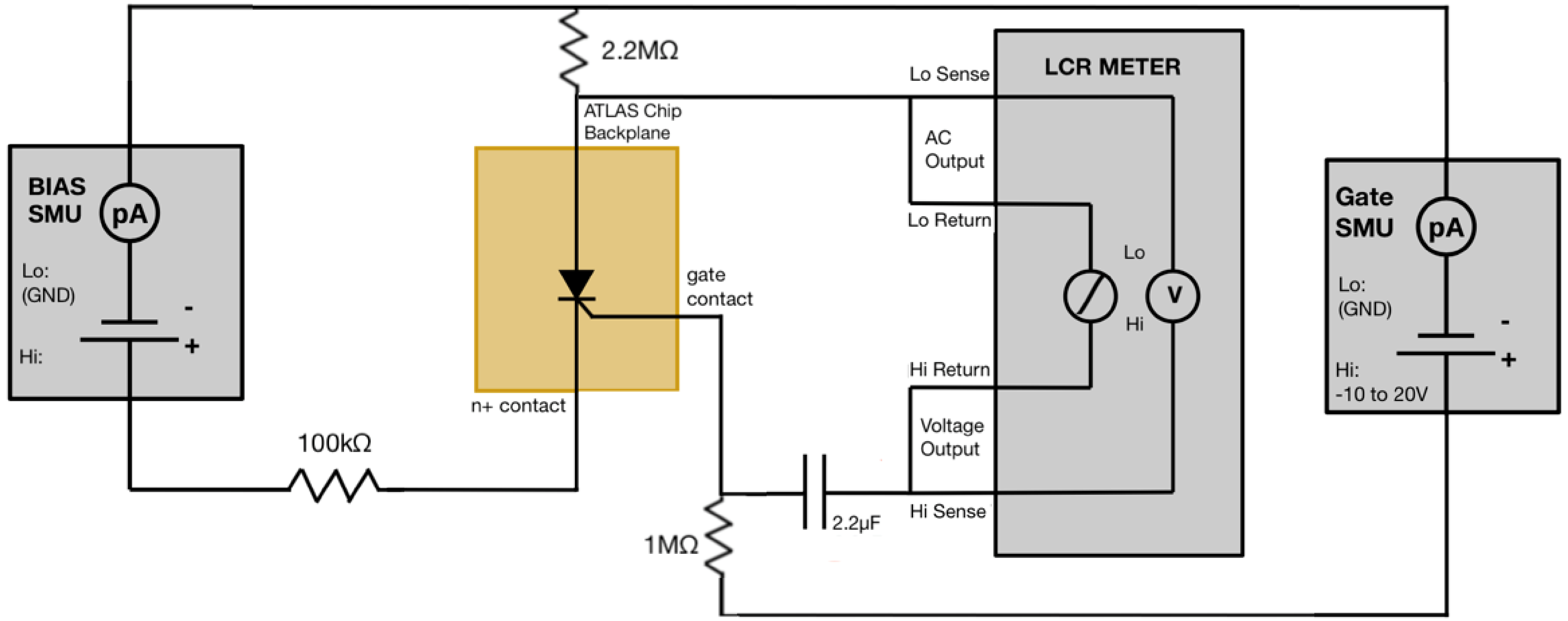
For the GCD IV:

- Bias the diode to constant voltage
- Scan voltages on the gate from -10V to +10V in 0.2V steps, measure the current through the diode (eg. via the bias SMU)

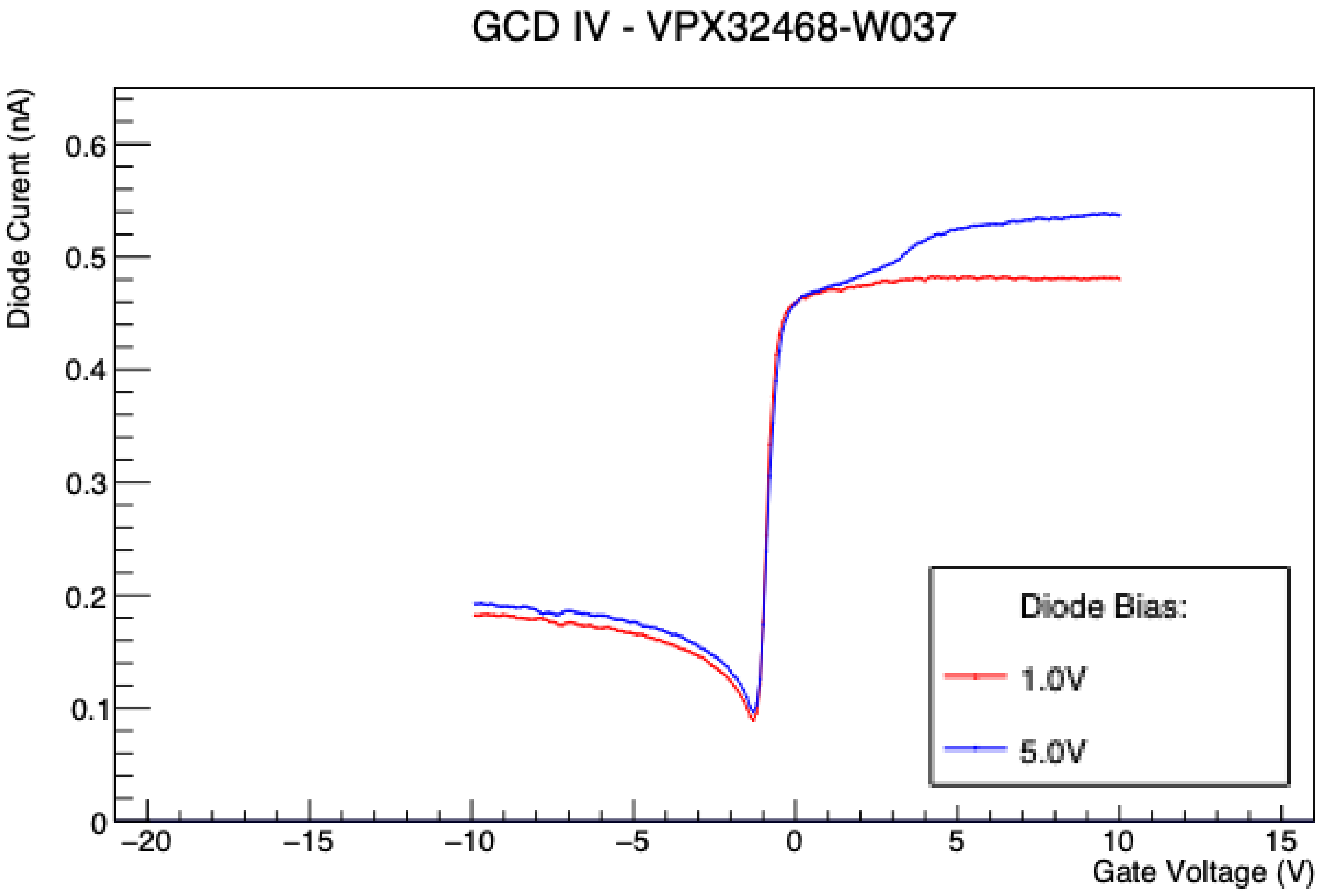
For the GCD CV:

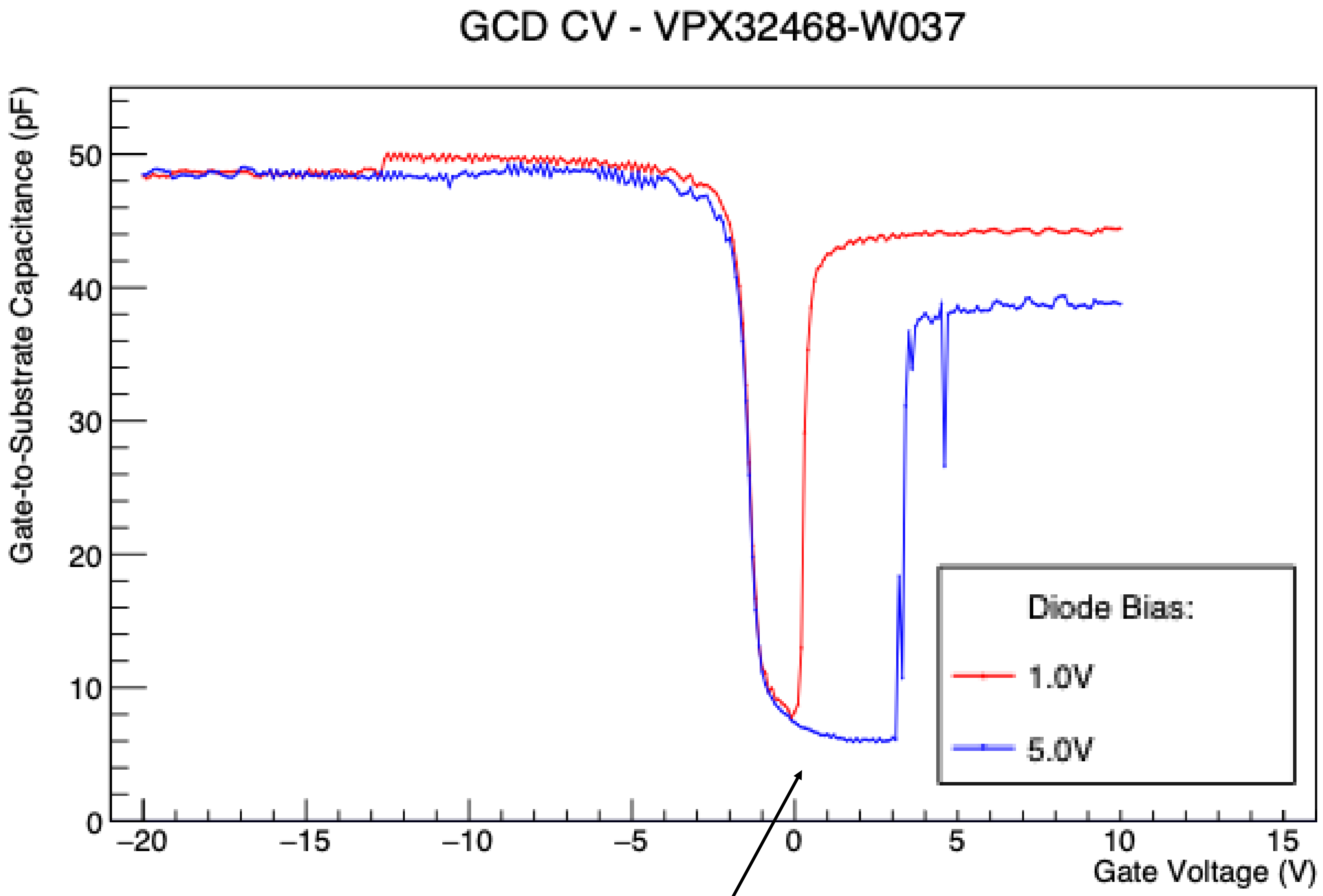
- Again, constant diode bias
- Measure CV of the gate using same procedure as for the MOS device





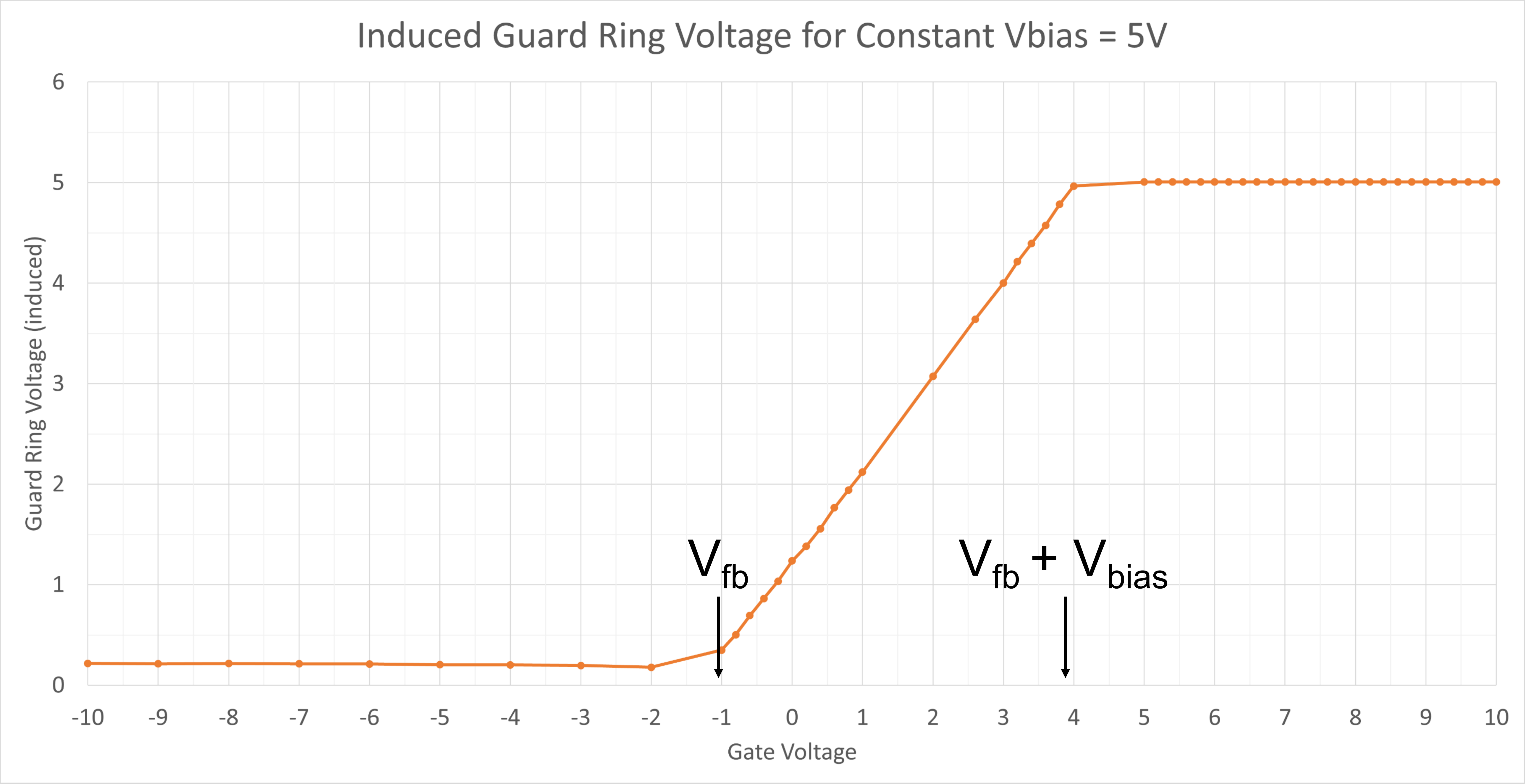
IV and CV of the GCD

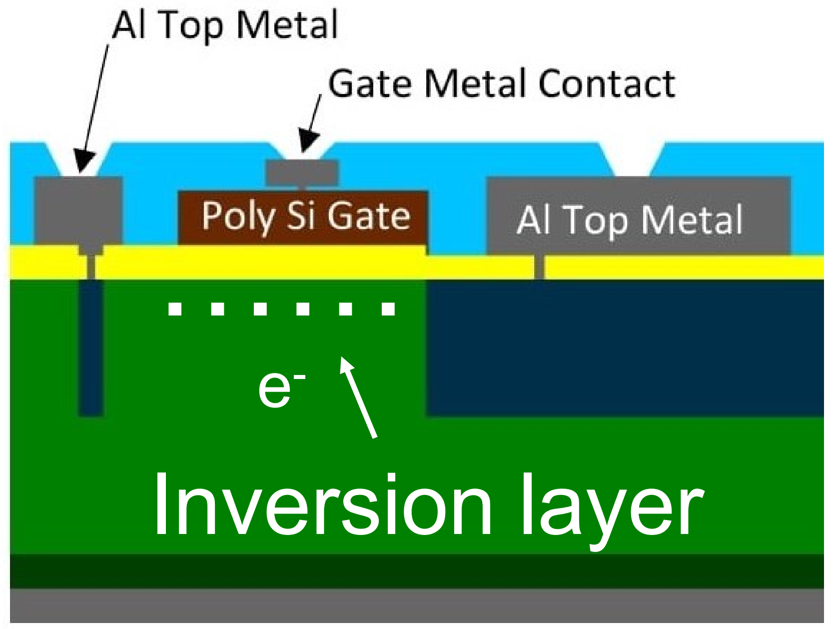


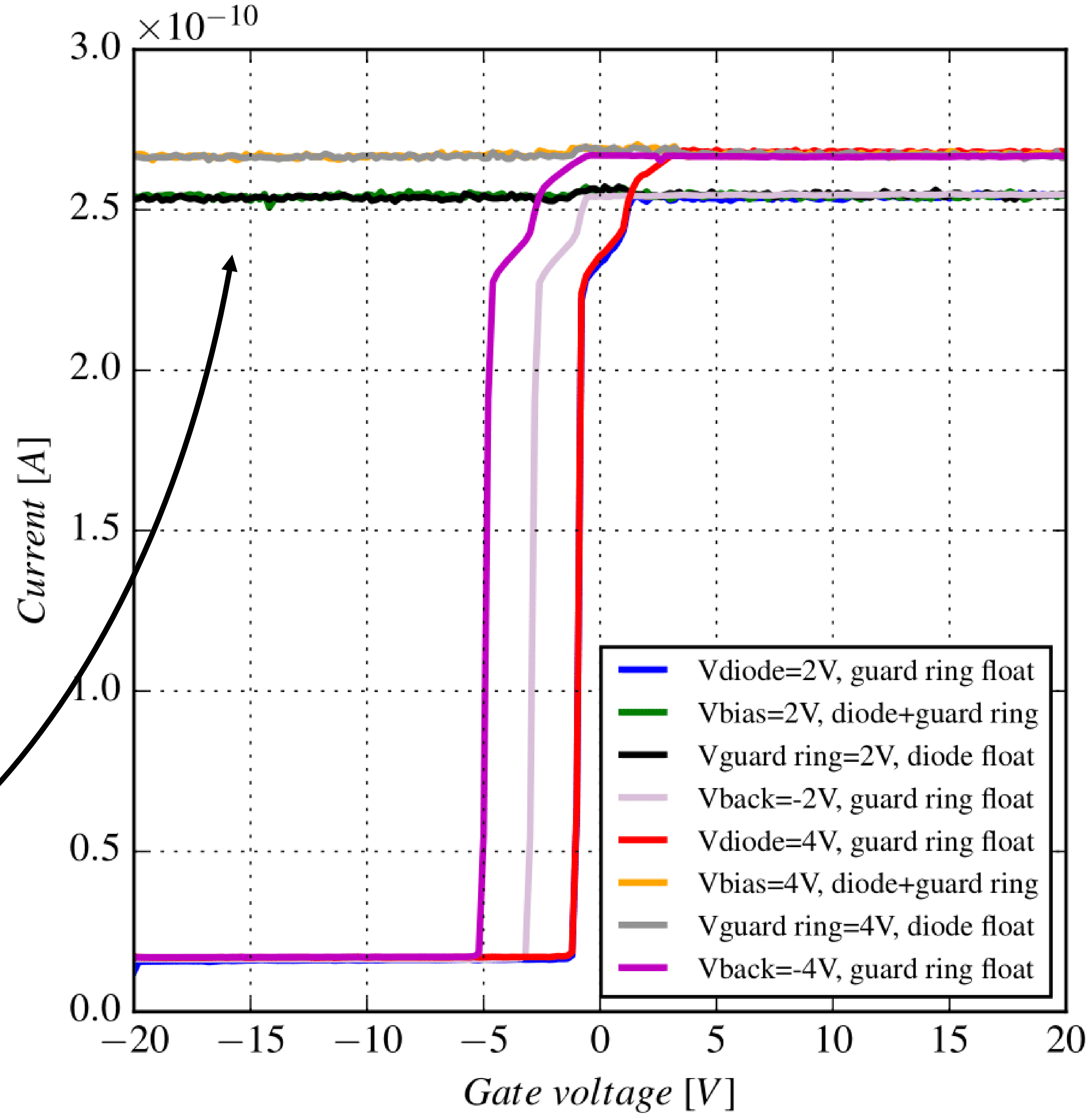


- Unable to extract surface reco. velocity
- No “turn around” in inversion for IV curve (should be around $V_{fb} + V_{bias}$)

Limitation of the GCD Design

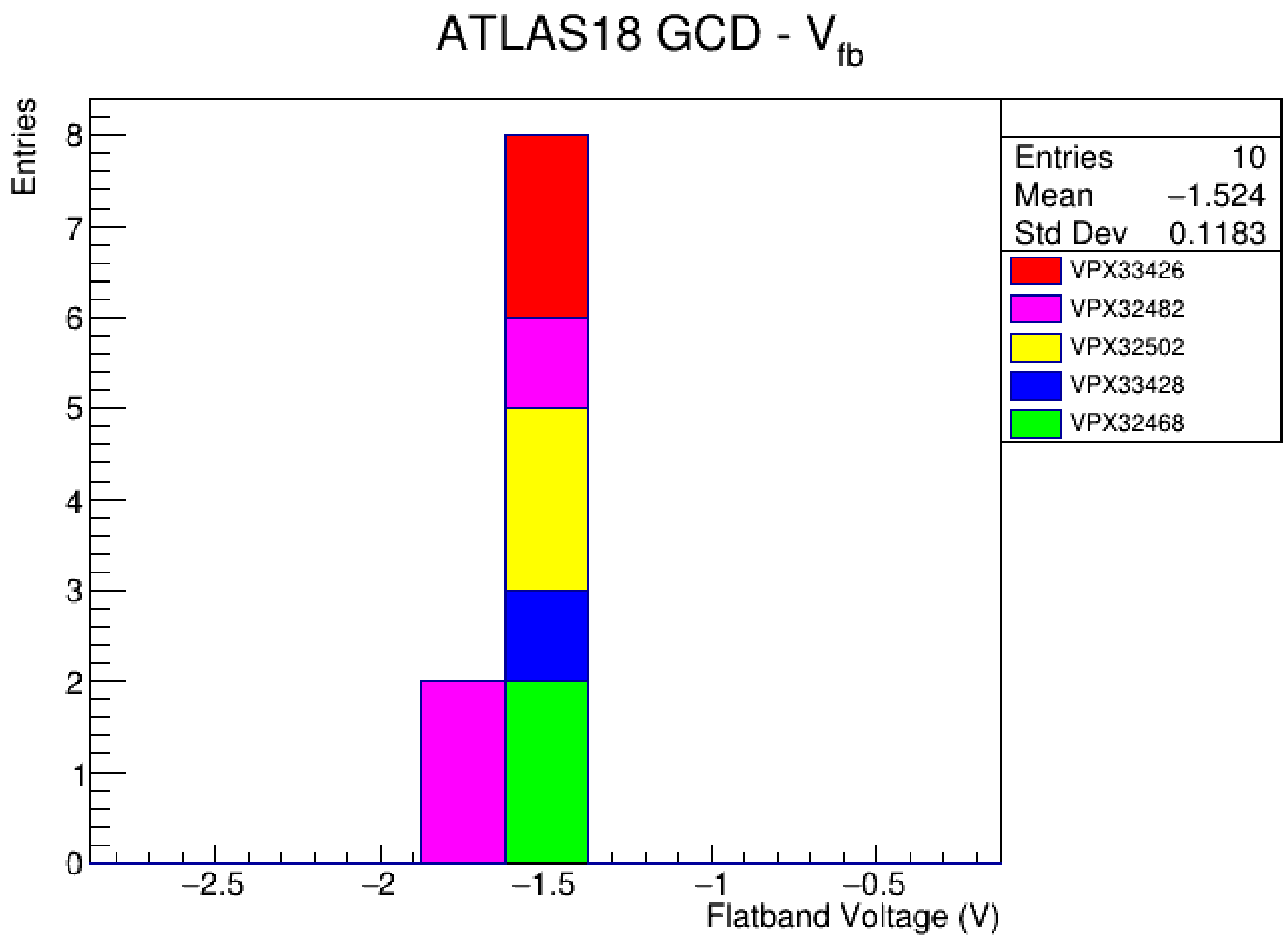


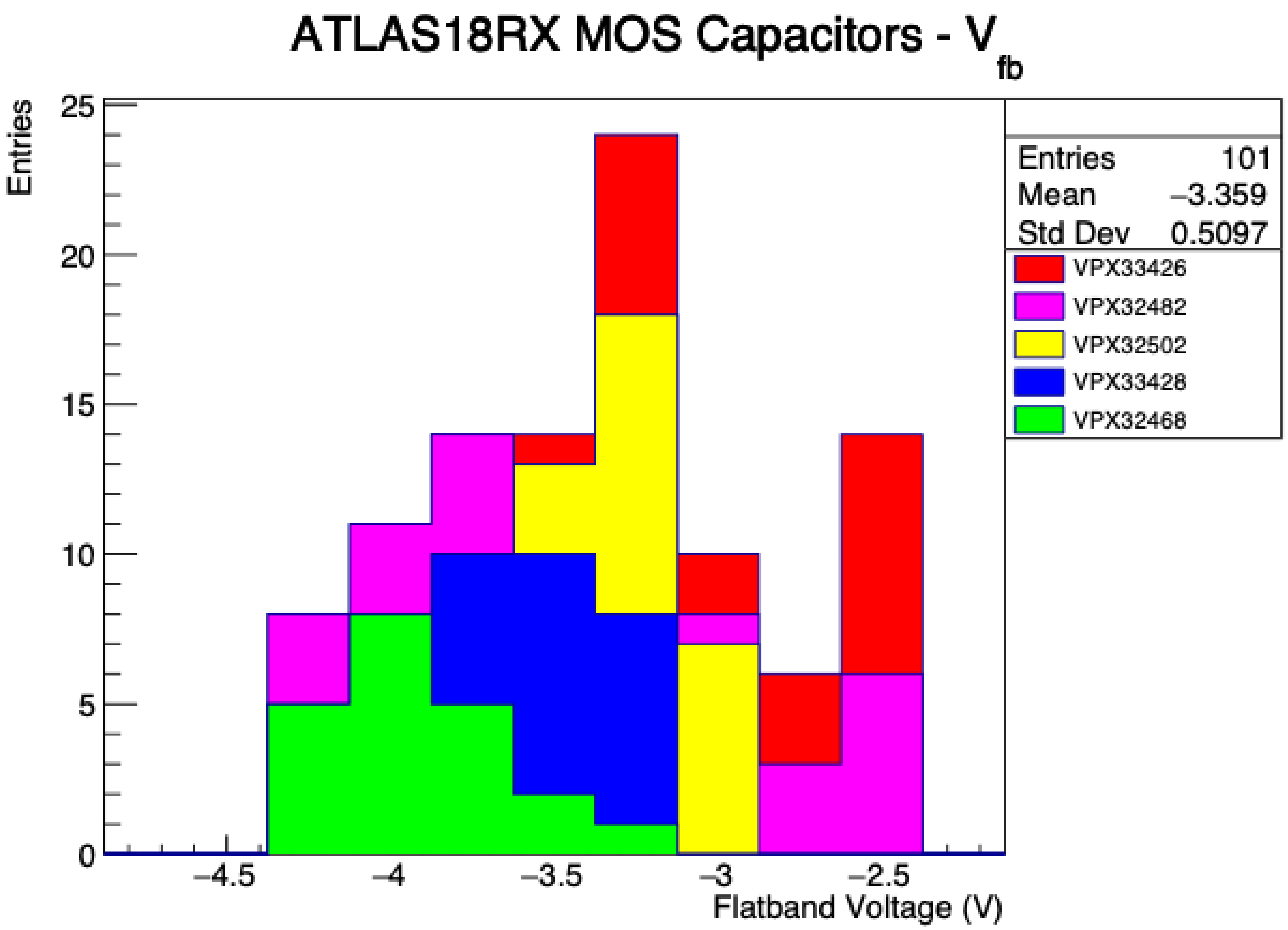




- Constant voltage at the diode, vary the voltage at the gate, measure voltage at the GR
- Conducting channel in inversion brings potential of GR to that of diode bias
- Current in inversion dominated by leakage from GR

Comparing MOS and GCD V_{fb}

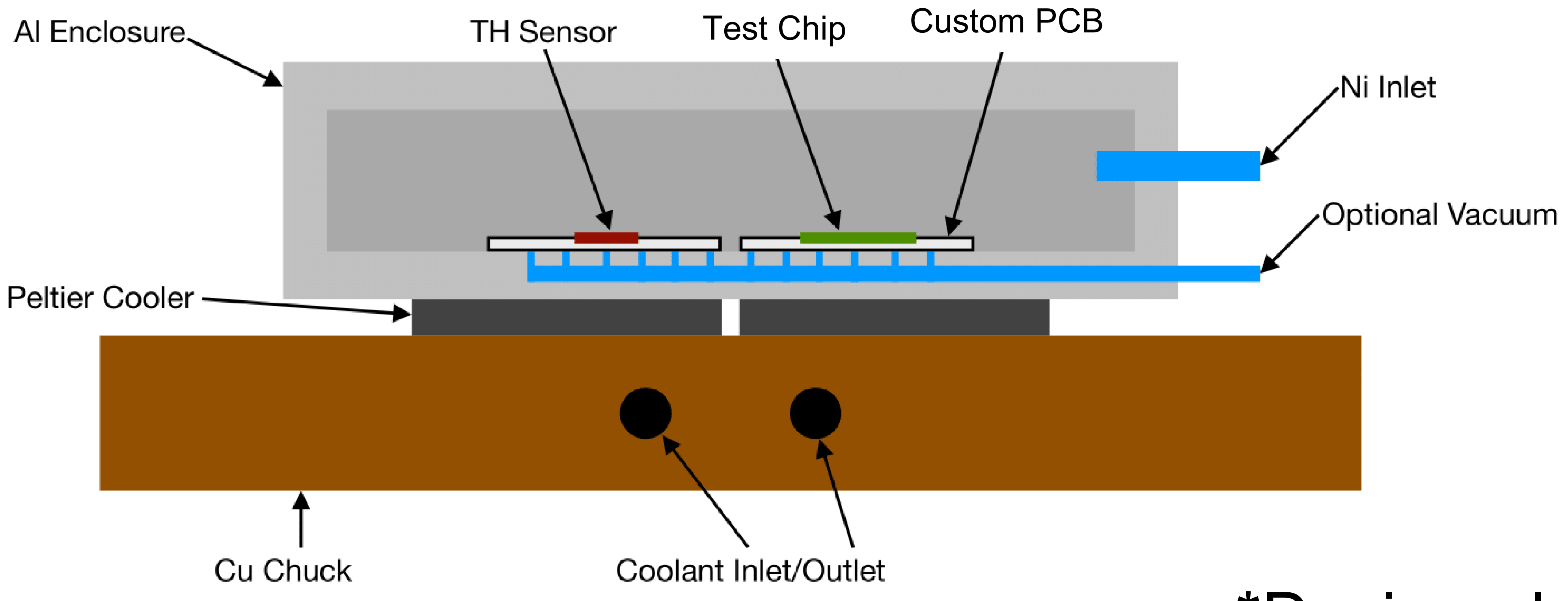




- Smaller sample of GCD CVs measured, but much lower variance in V_{fb}
- GCD appears to provide a better handle on V_{fb} measurement, probably due to guard ring

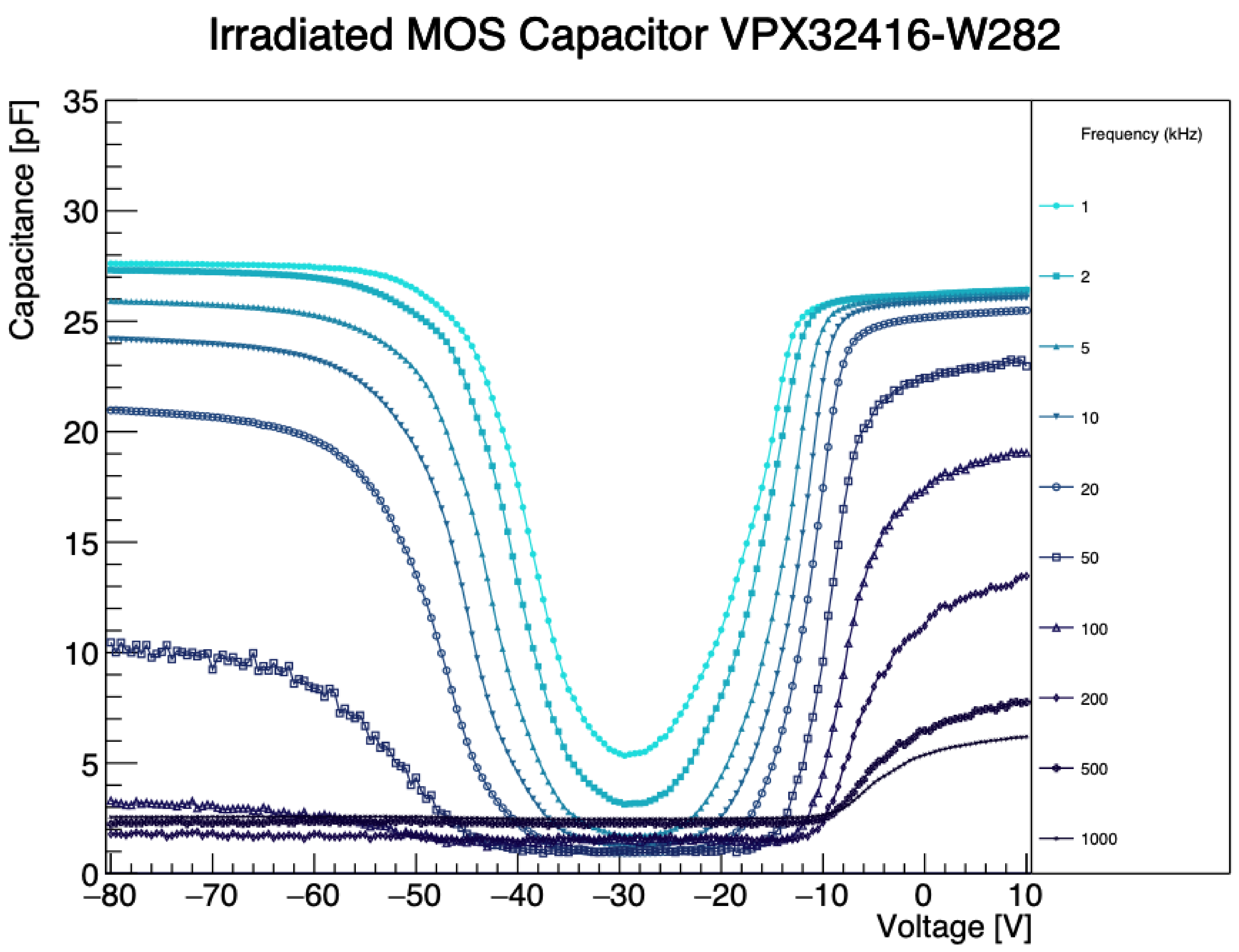
Gamma Irradiations

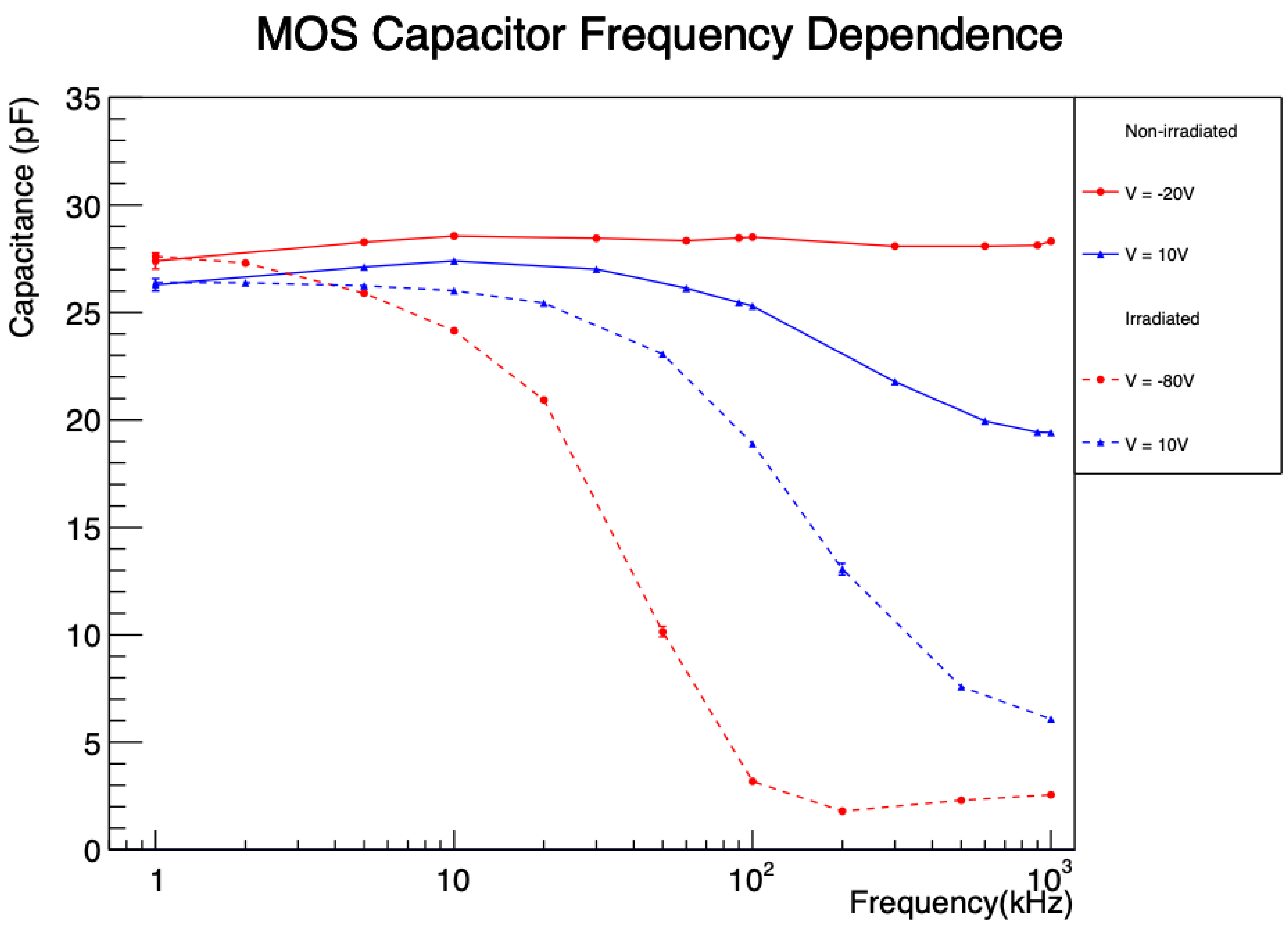
- Sample of test chips irradiated with gammas from Co-60 at UJP Praha as., Prague. 28.2 hours at dose rate 39krad/min for TID of 66Mrad
- Samples annealed at 80C for 1 hour and stored at or below -20C
- Test chips mounted to custom PCB* and measured in a custom cold jig which maintains -20C and <35% RH (see backup for more photos)
- Expect to see radiation induced surface damage -> increased positive space charge in oxide; fast surface states give rise to larger s_o



*Designed and supplied by University of Toronto

Gamma Irradiated MOS

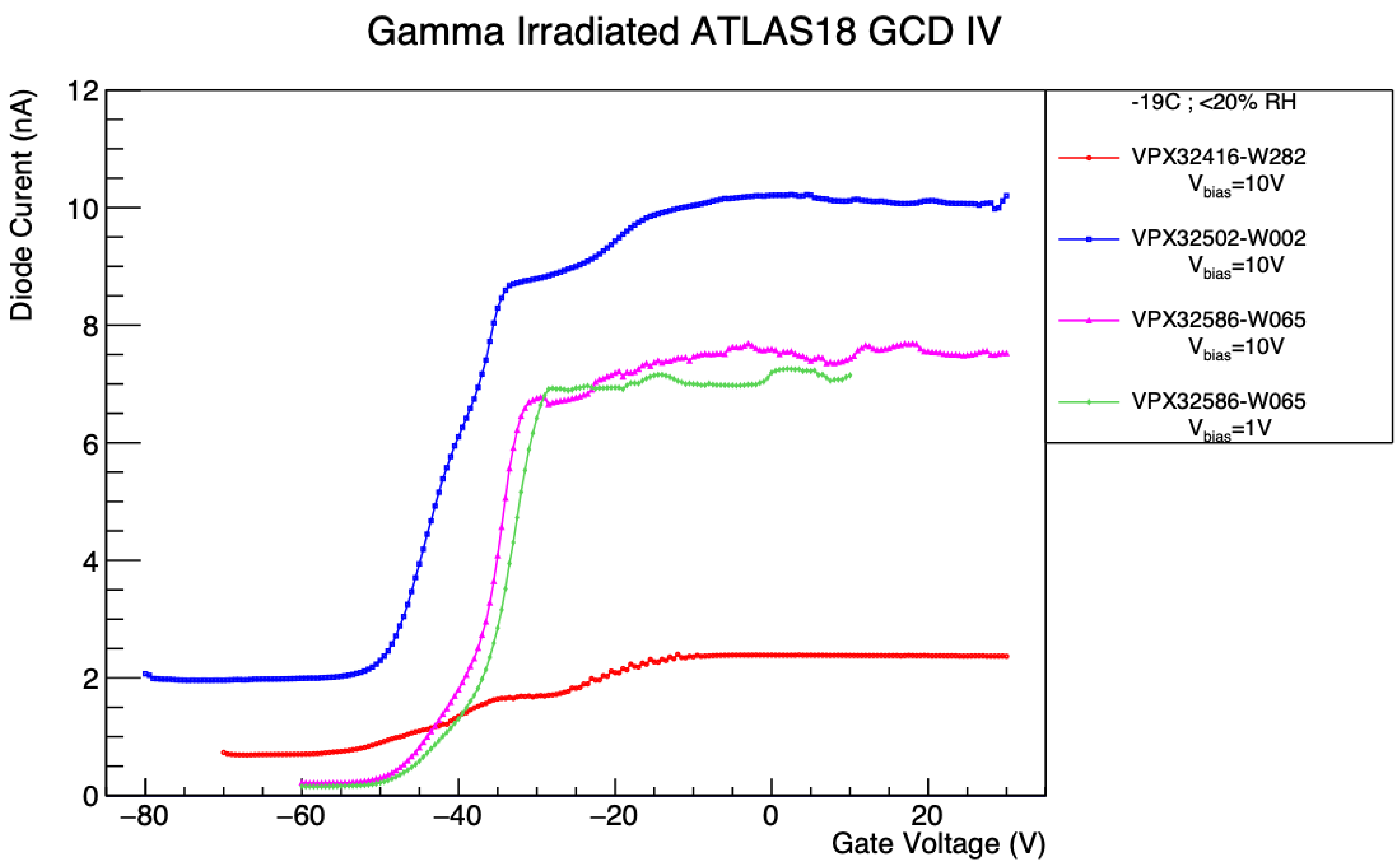


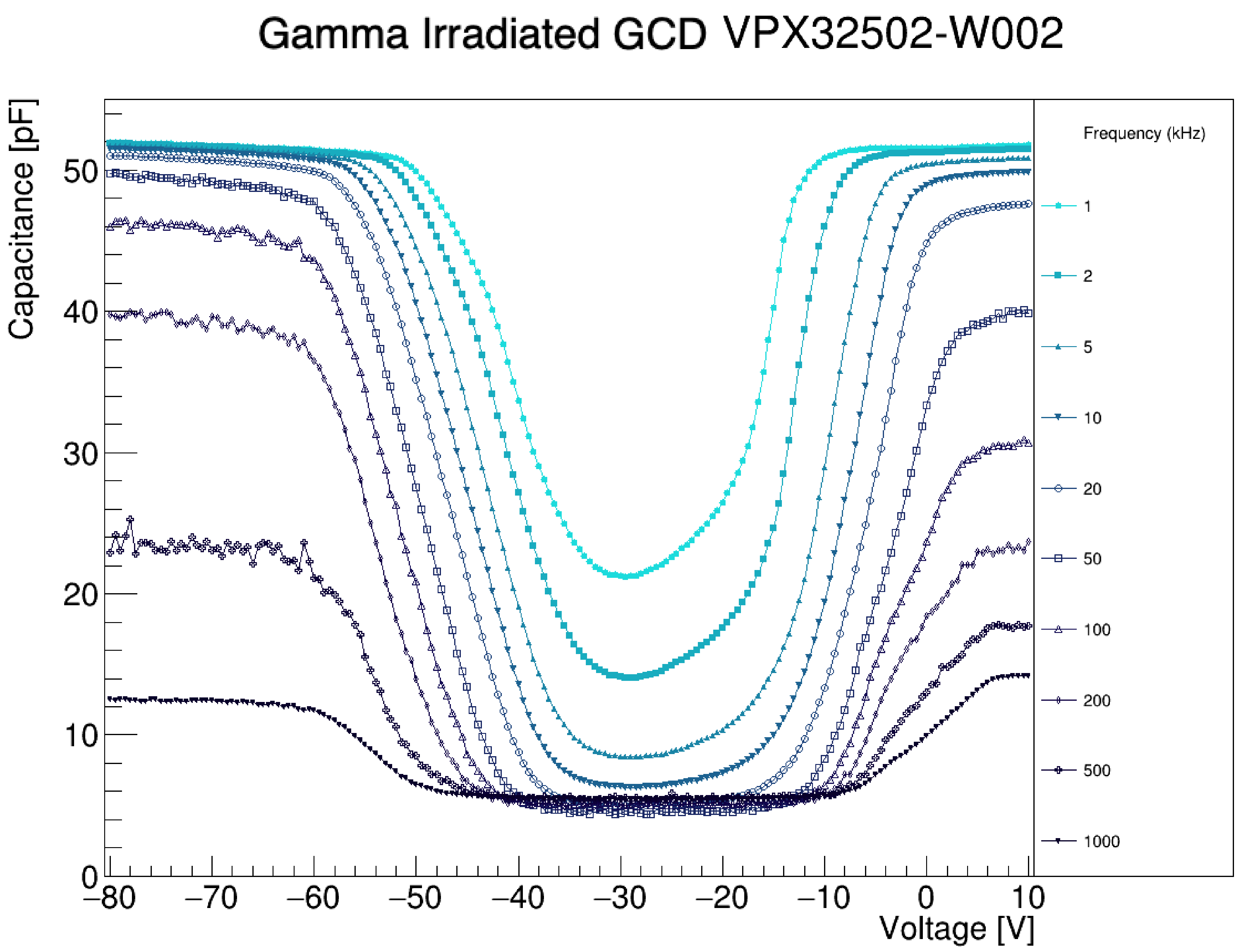


- High bulk resistivity -> measured capacitance in accumulation decreases for high frequencies
- V_{fb} now shifted to ~-40V -> increase in trapped charges in the oxide

$$C_{meas} = \frac{C}{1 + \omega^2 R_s^2 C^2}$$

Gamma Irradiated GCD – CV





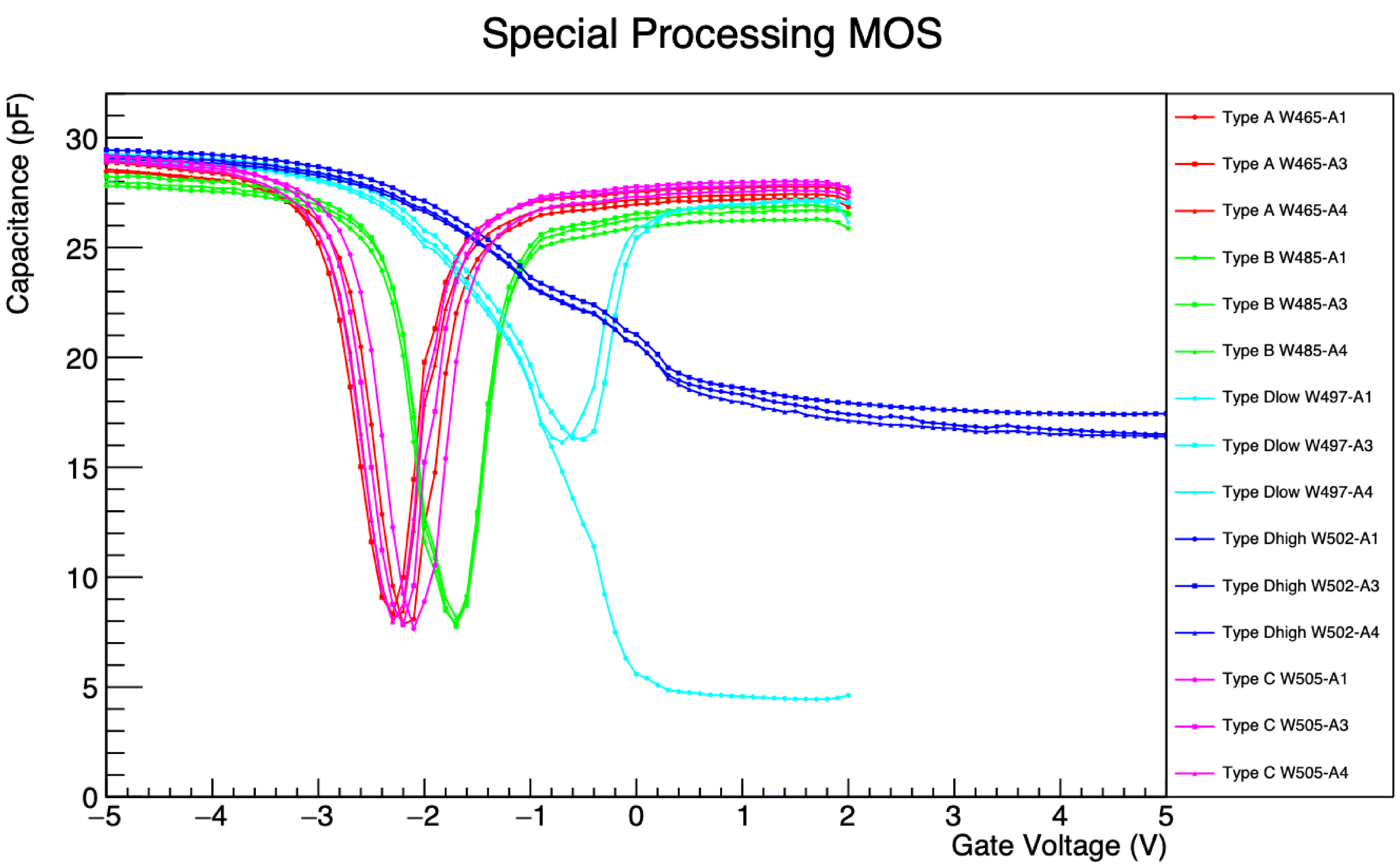
- IV cannot be used to extract s_o as with the non-irradiated devices
- CV can still be used as another handle for V_{fb} determination; again, V_{fb} shifted to ~-40V (1kHz)

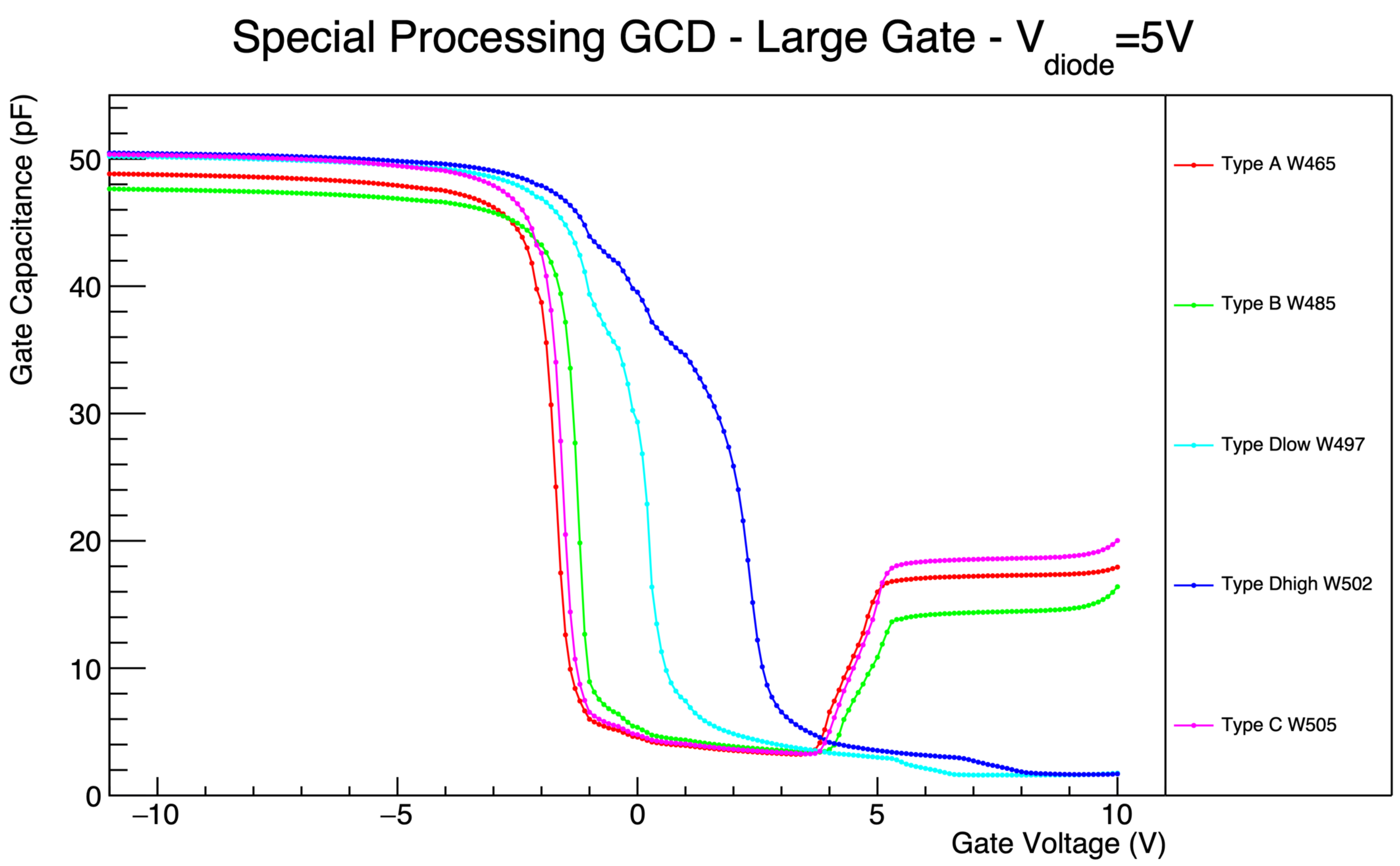
Split Process Wafers

- Attempt to mitigate humidity-induced effects (link)
- 5 types of special process wafers*:
  - Type A -> Special treatment for passivation, implemented in pre-pro sensors
  - Type B -> Type A + “Special Masking”
  - Type C -> Type A + “Thicker Passivation”
  - Type D (low and high) -> Type A + “P-spray process” (low and high dose)

*Processing information courtesy of ITk strips collaborator Xavi Fernandez-Tejero (SFU)

SP Wafers MOS and GCD





A – Production Treatment

B – Special Mask

C – Thicker Pass.

Dlow – P-spray low

Dhigh – P-spray high

- V_{fb} changes for various treatments
- Can compare V_{fb} from GCD CV

Conclusions

- Study of MOS and GCD devices of the ATLAS test chip presented
- The MOS can be used to extract parameters: oxide capacitance, oxide thickness, flat band voltage -> useful to monitor manufacturing consistency and radiation induced positive charge buildup
- The gated diodes cannot be used to extract a surface recombination velocity, but the CV can be used as another measure of the oxide thickness, V_{fb}
- Large variation in MOS performance -> GCD is more consistent
- Special split processes were also studied with a measurable effect in device characteristics being observed

Backup

Setup for the MOS Device

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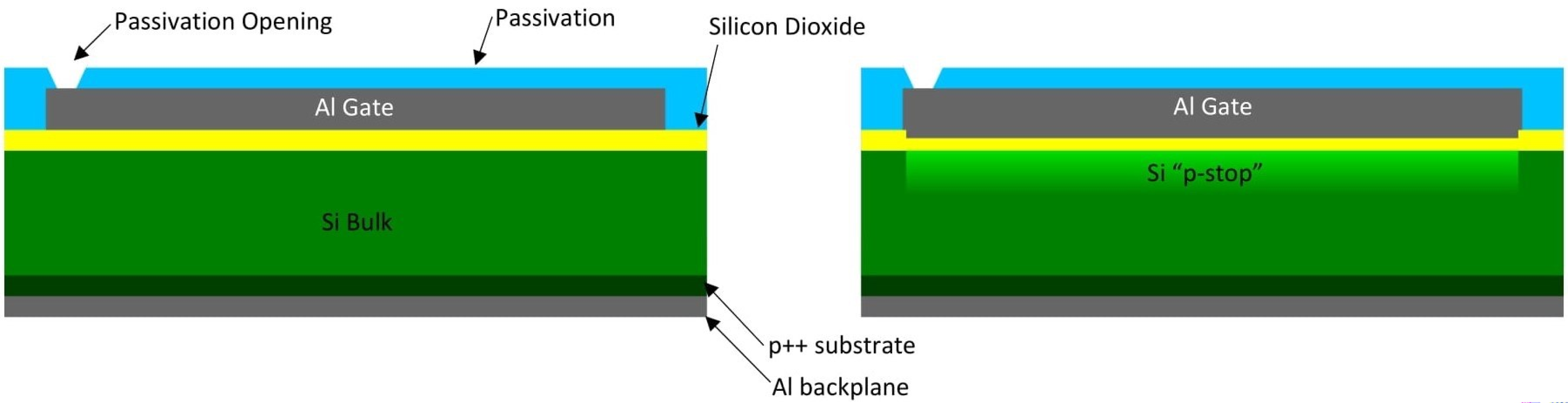
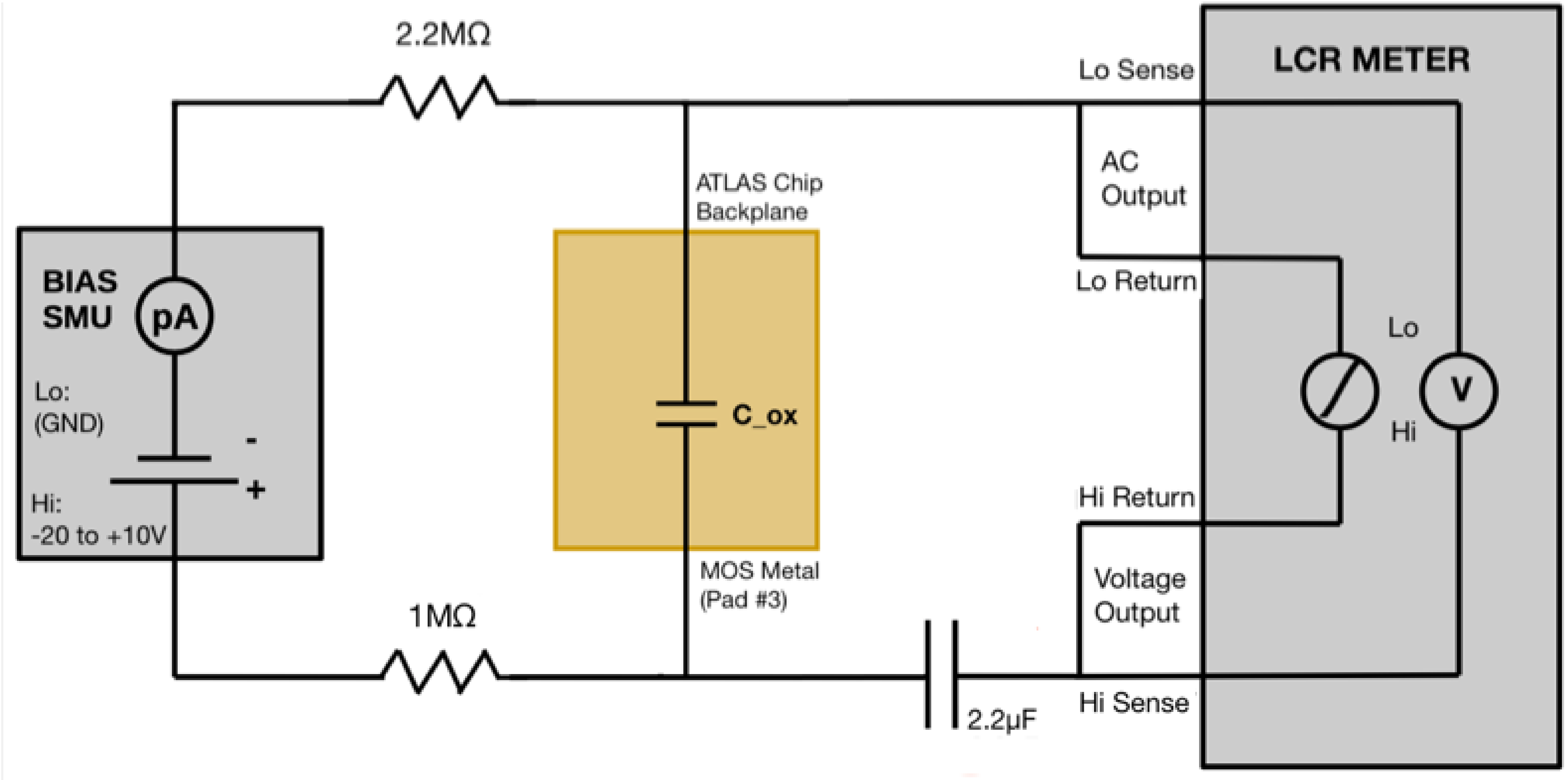
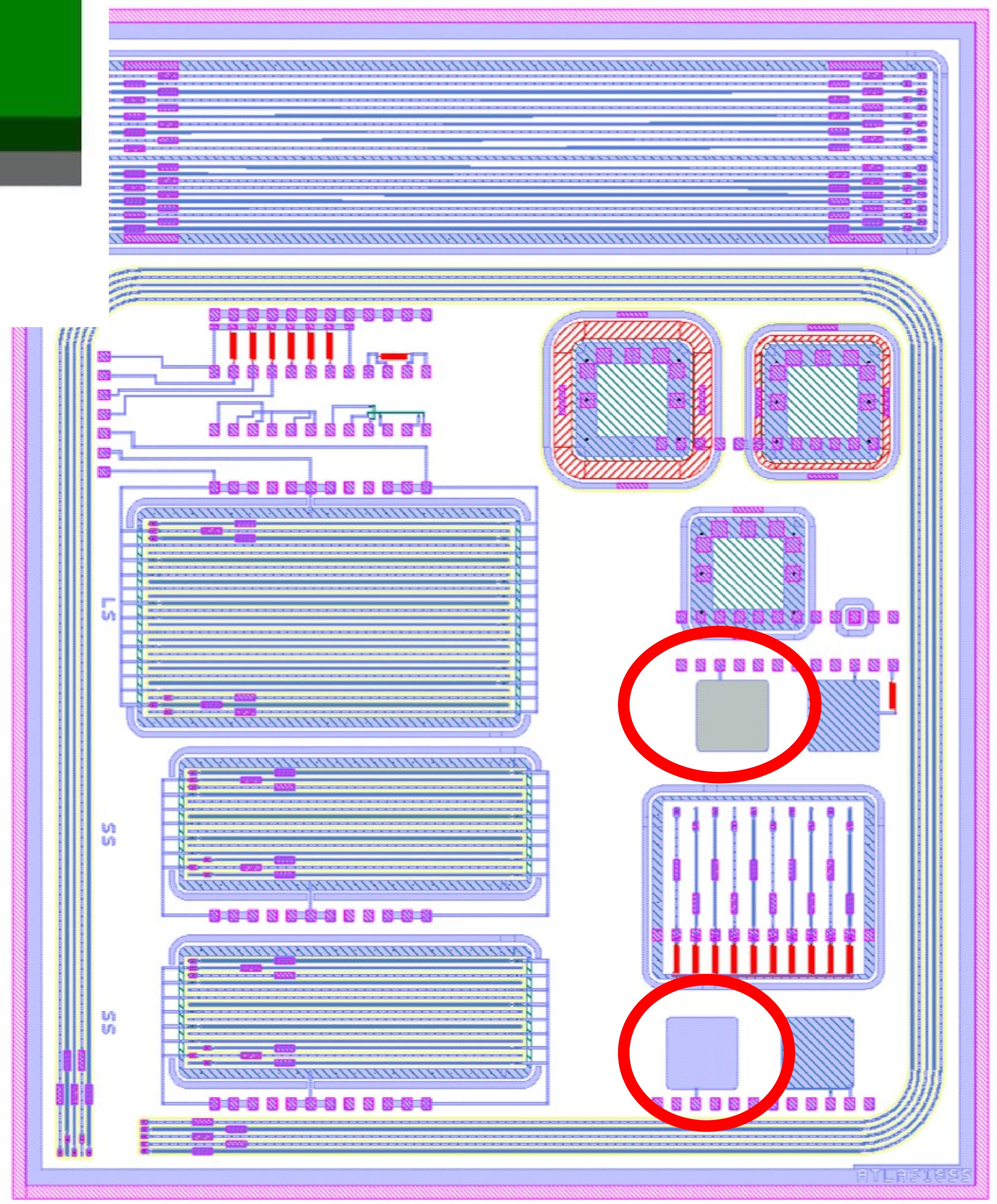
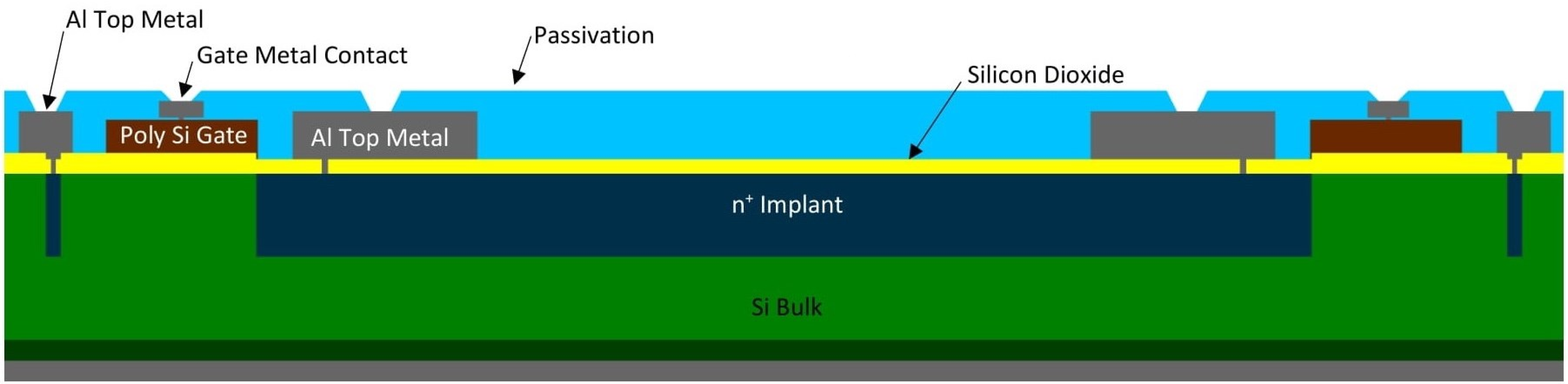


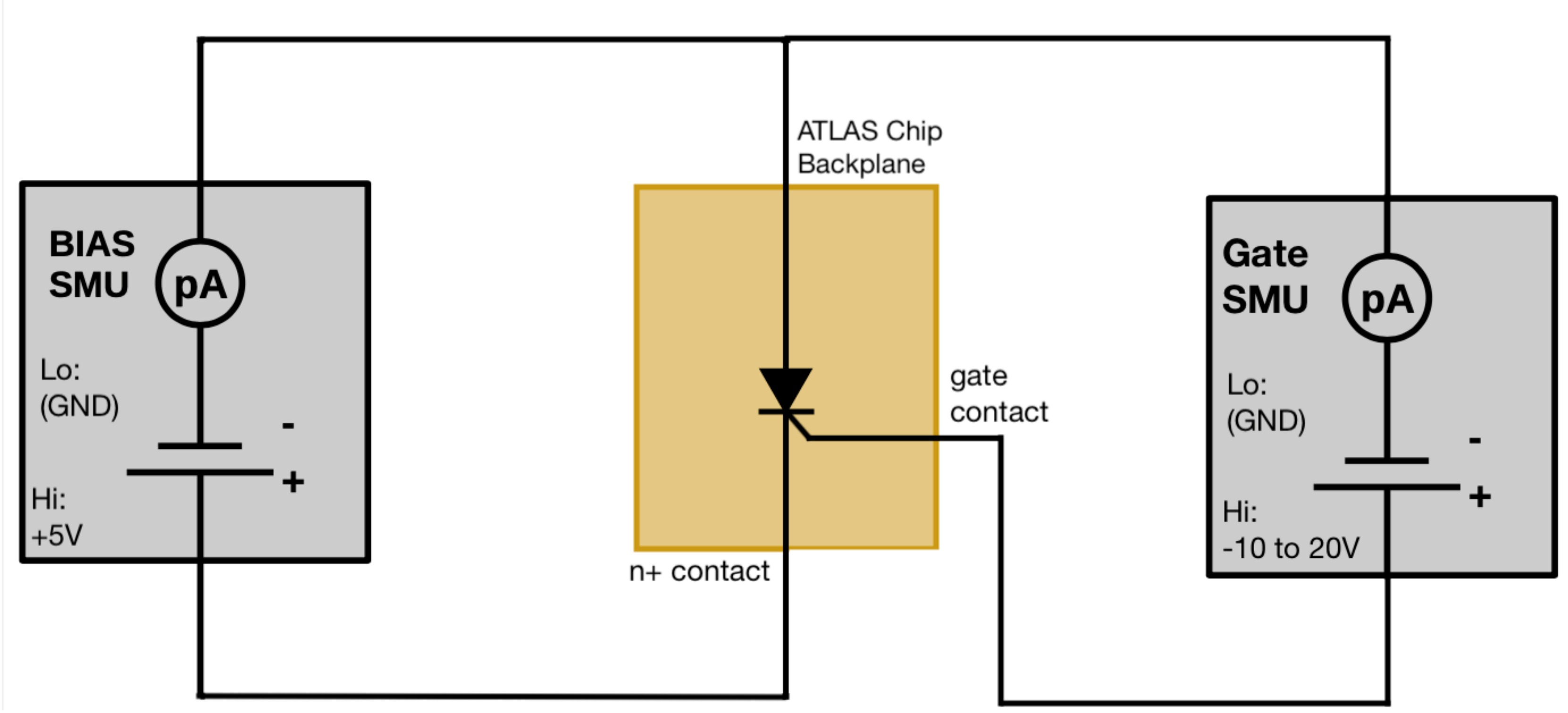




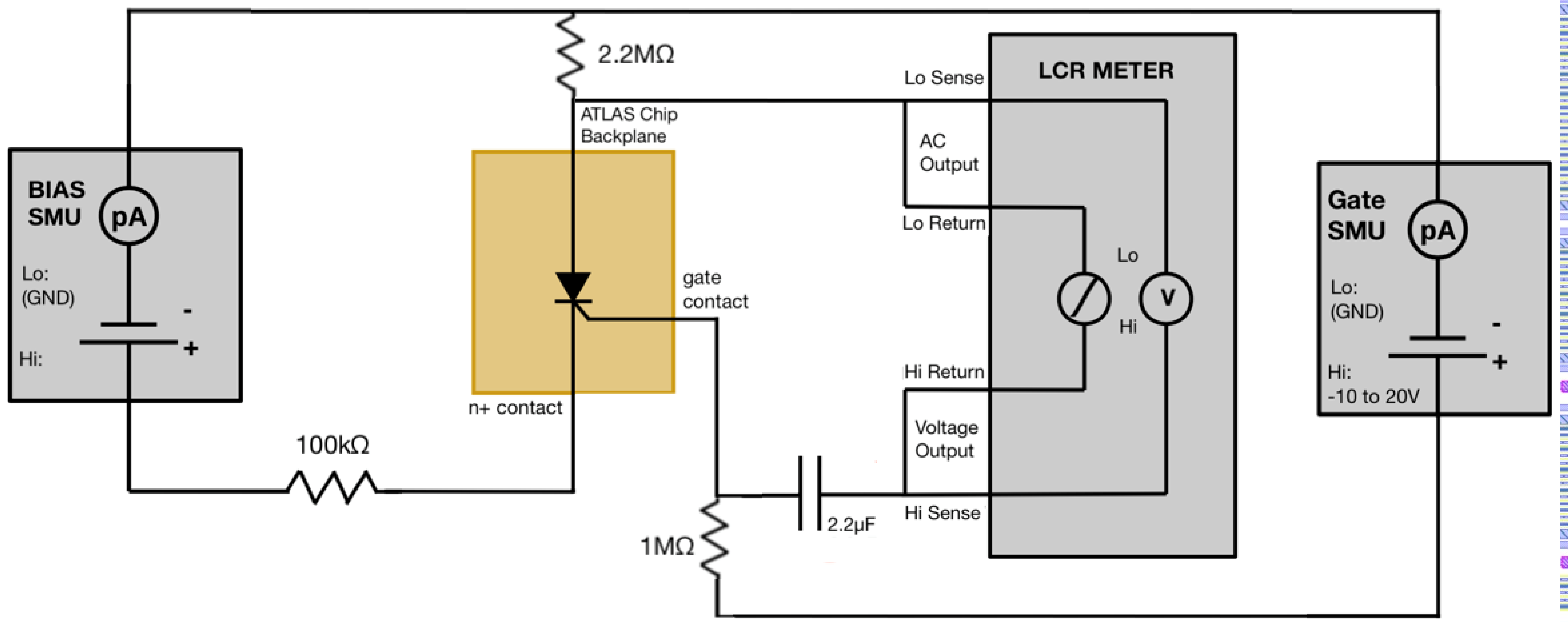
Setup for the GCD

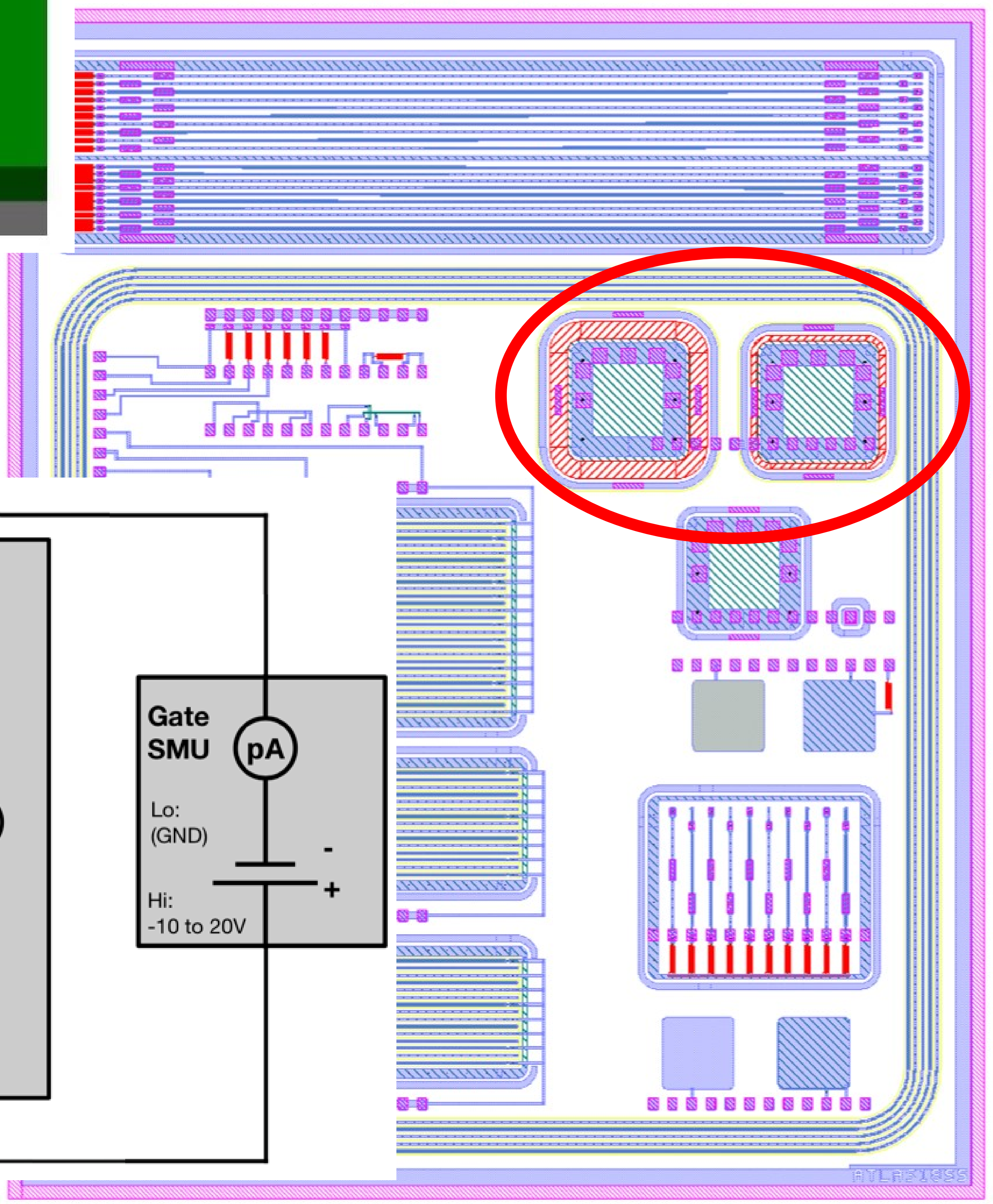


Current Measurement



Capacitive Measurement

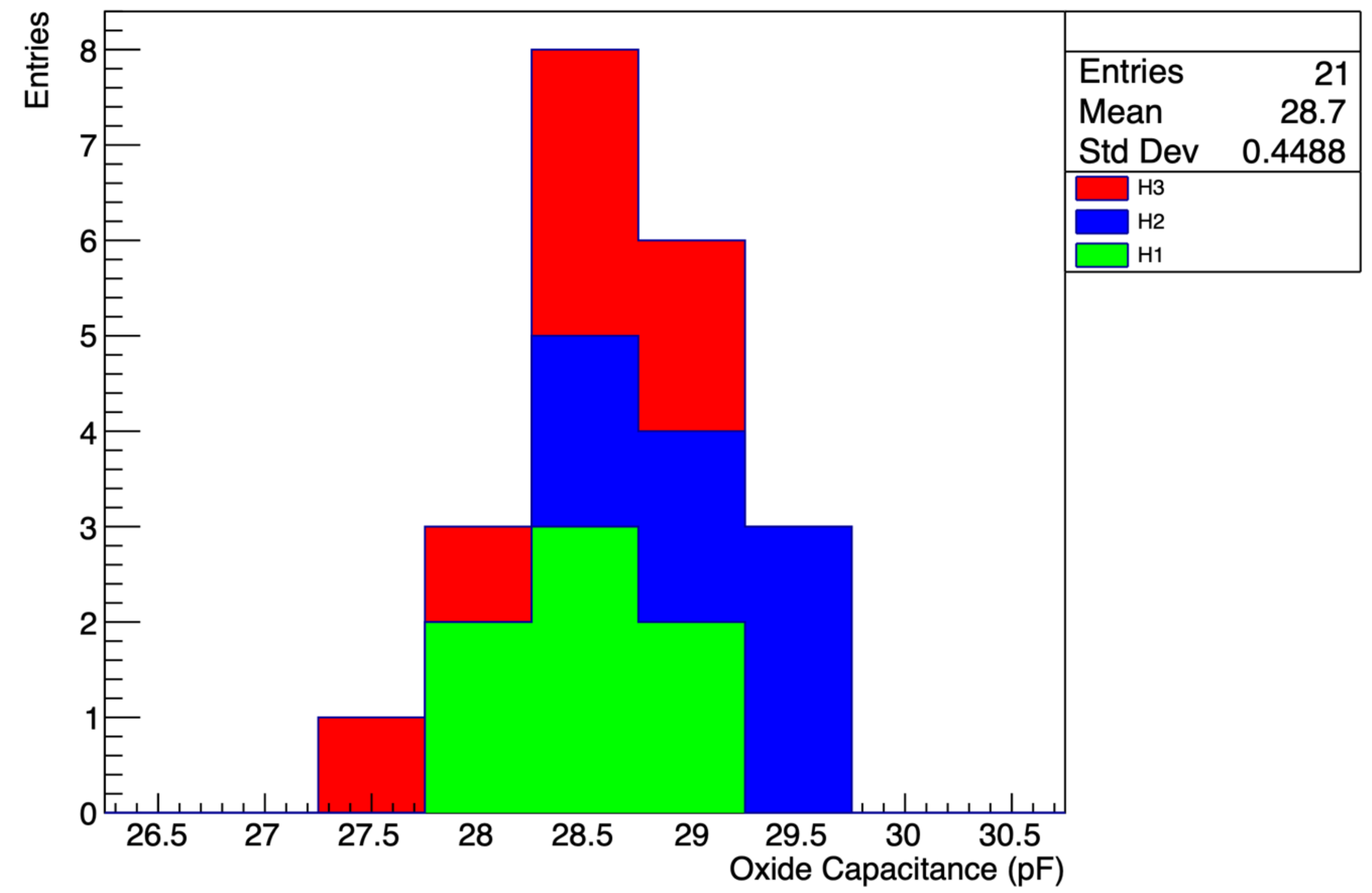




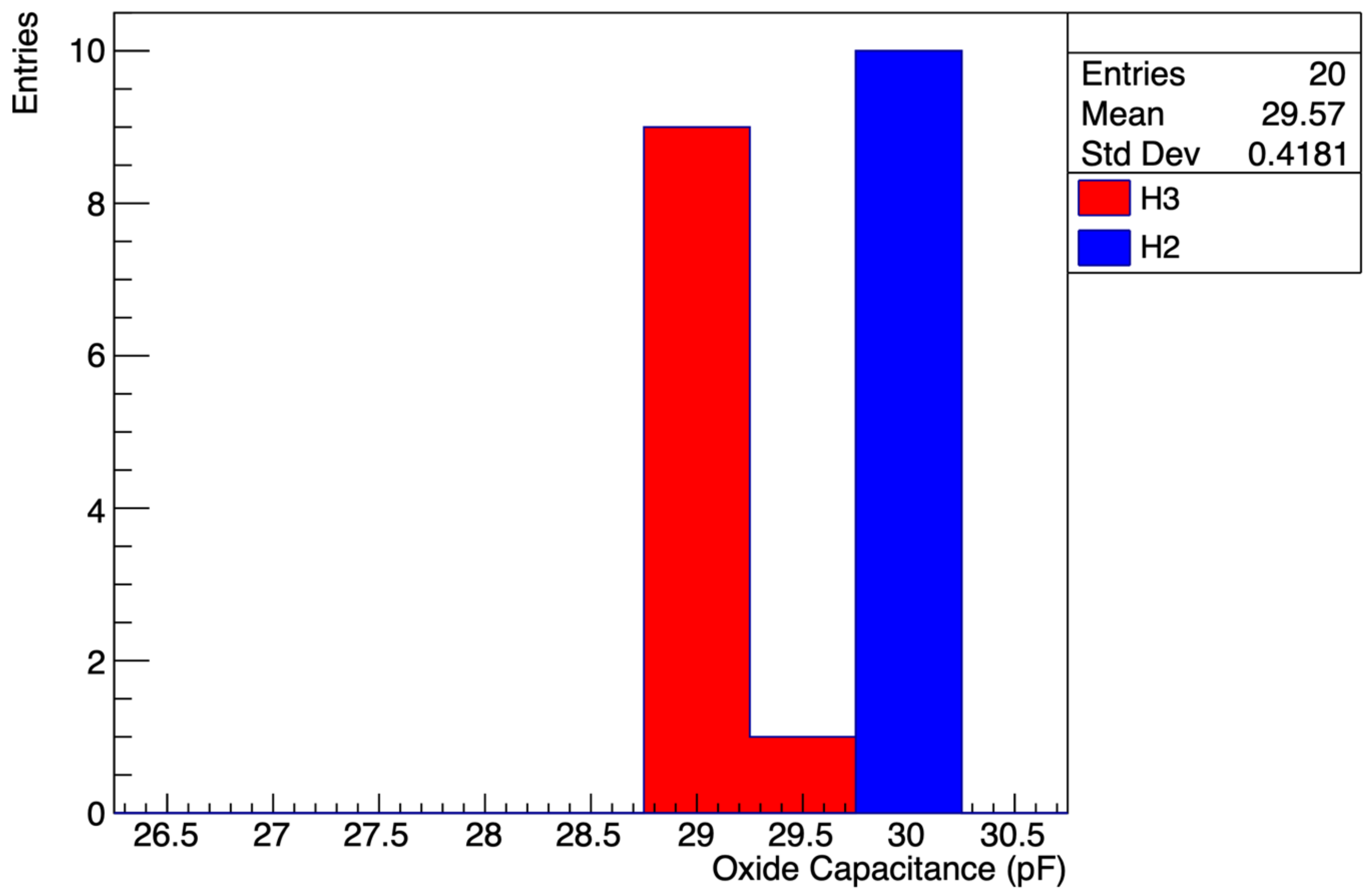
C_{ox} by Batch

“Left-to-right” trend → Oxide is generally thinner on right side of wafer

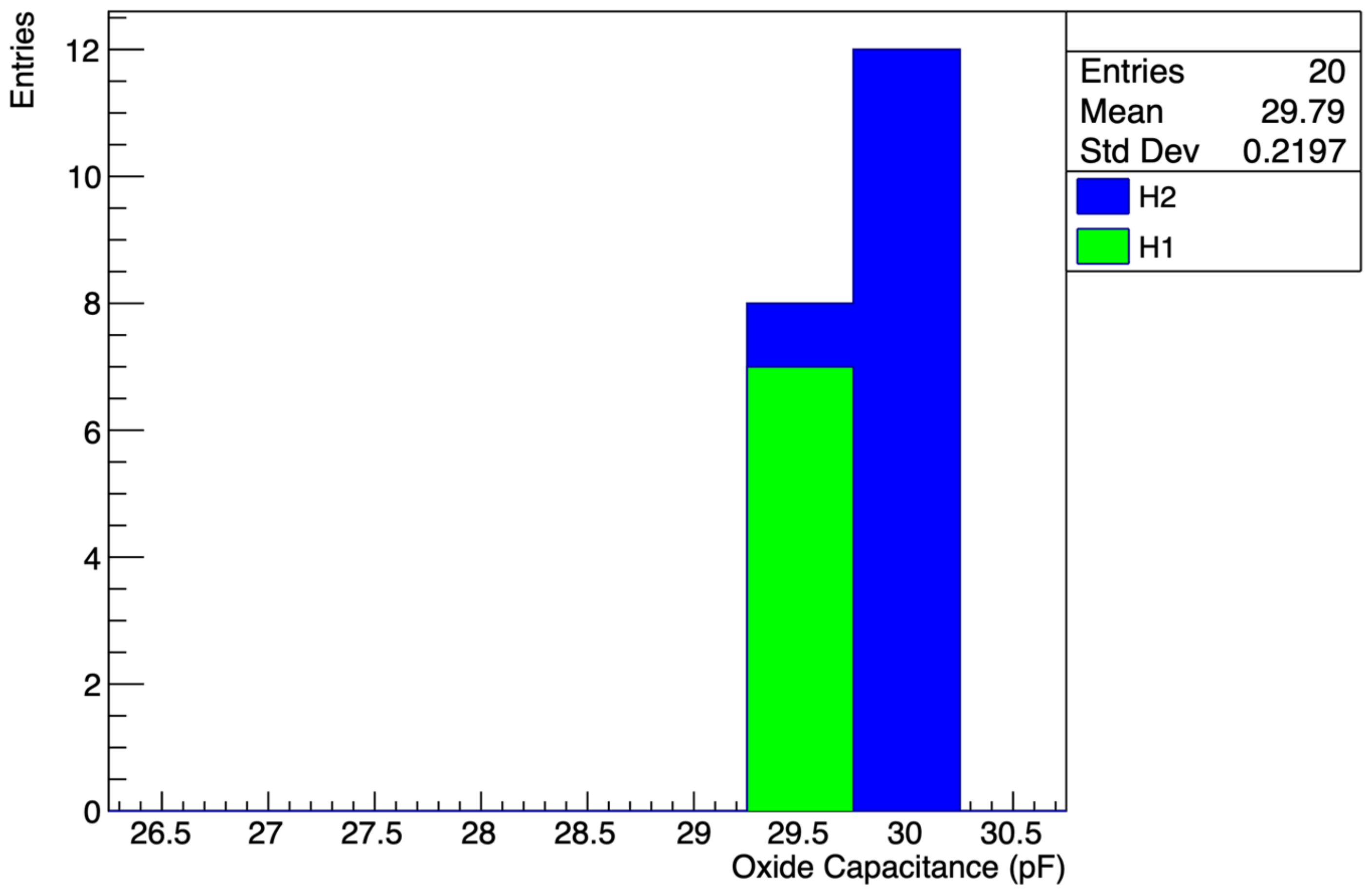
ATLAS18R0 MOS Capacitors VPX32468 - C_{ox}



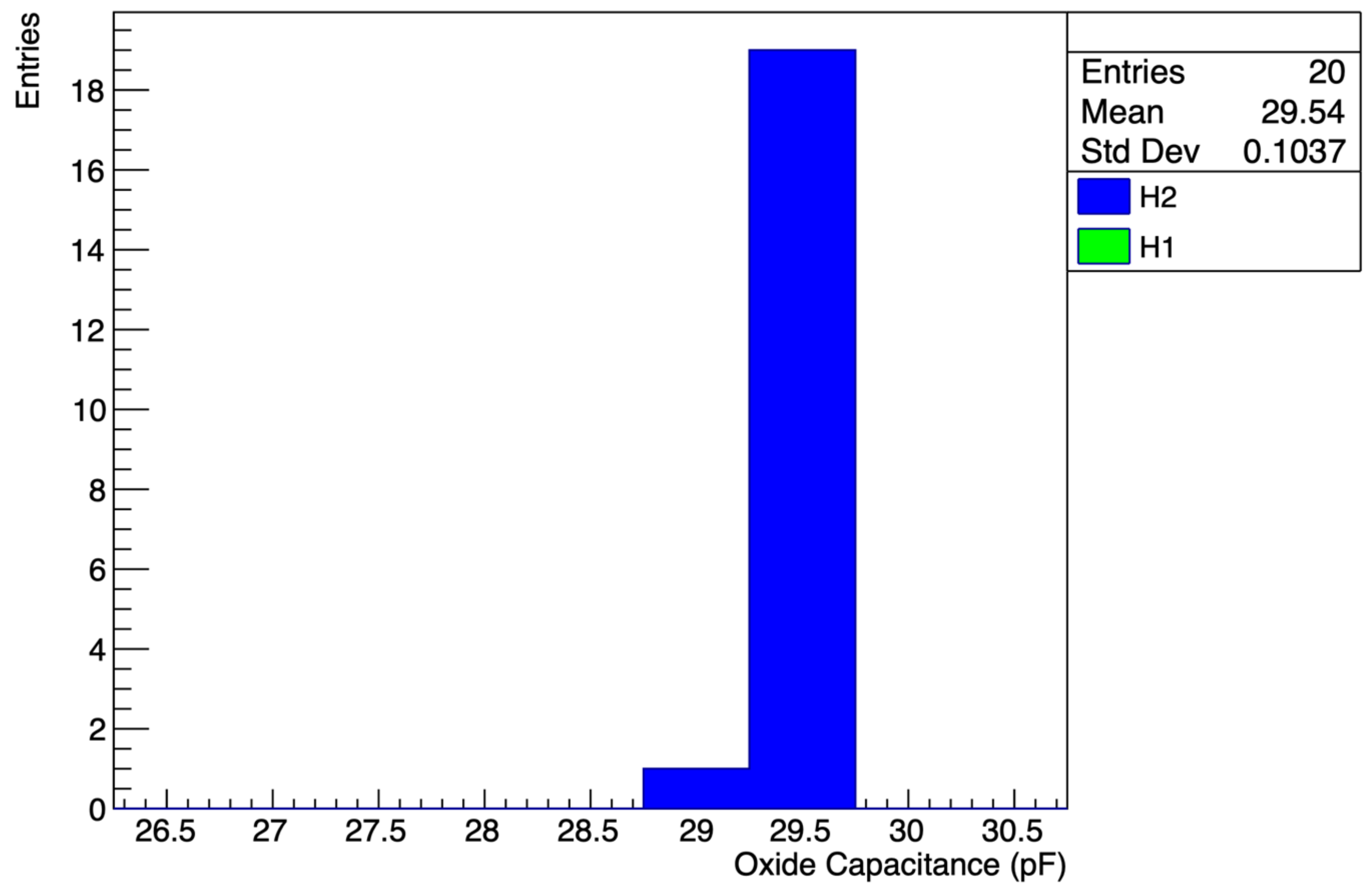
ATLAS18R0 MOS Capacitors VPX33426 - C_{ox}



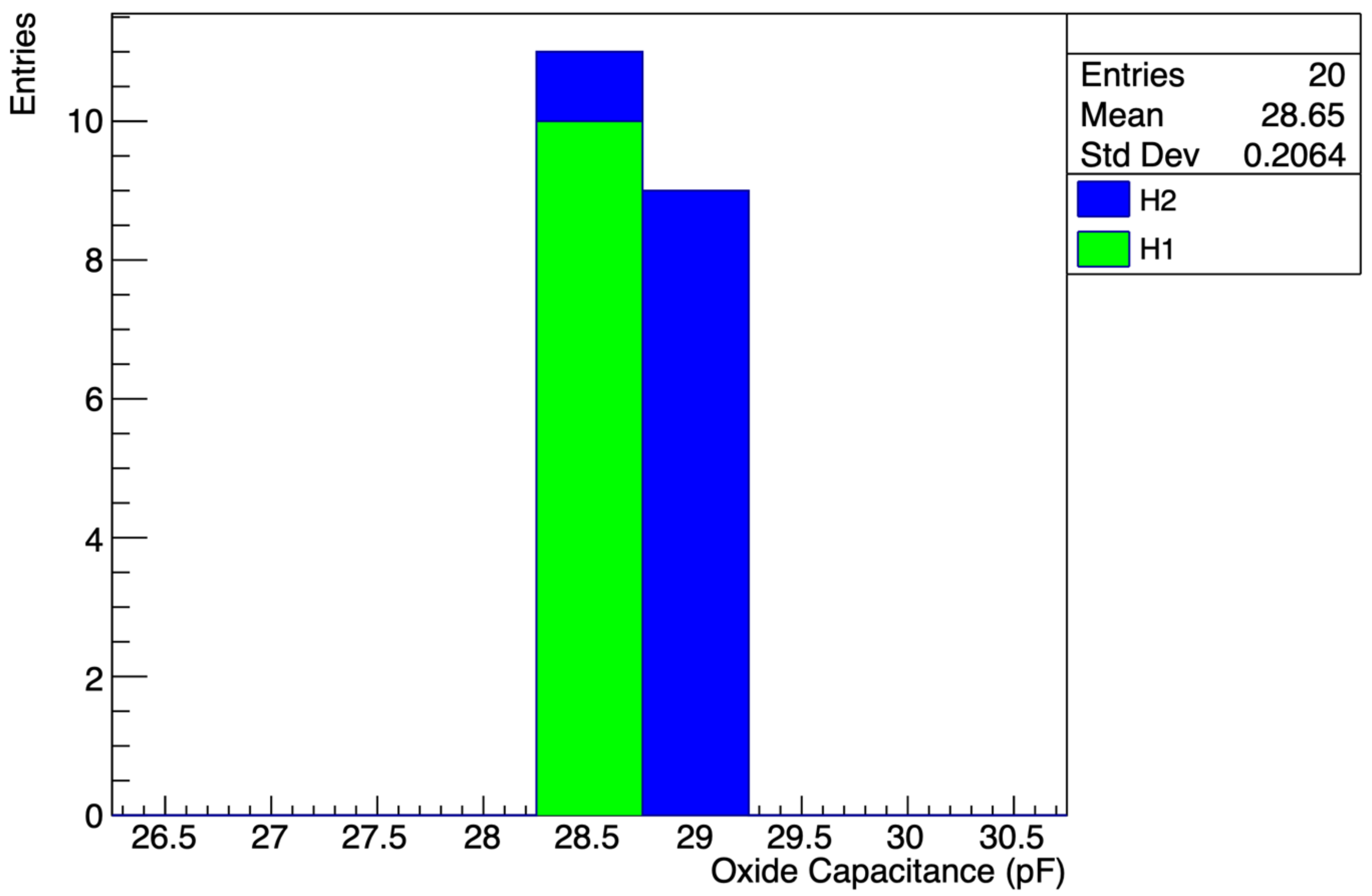
ATLAS18R2 MOS Capacitors VPX32502 - C_{ox}

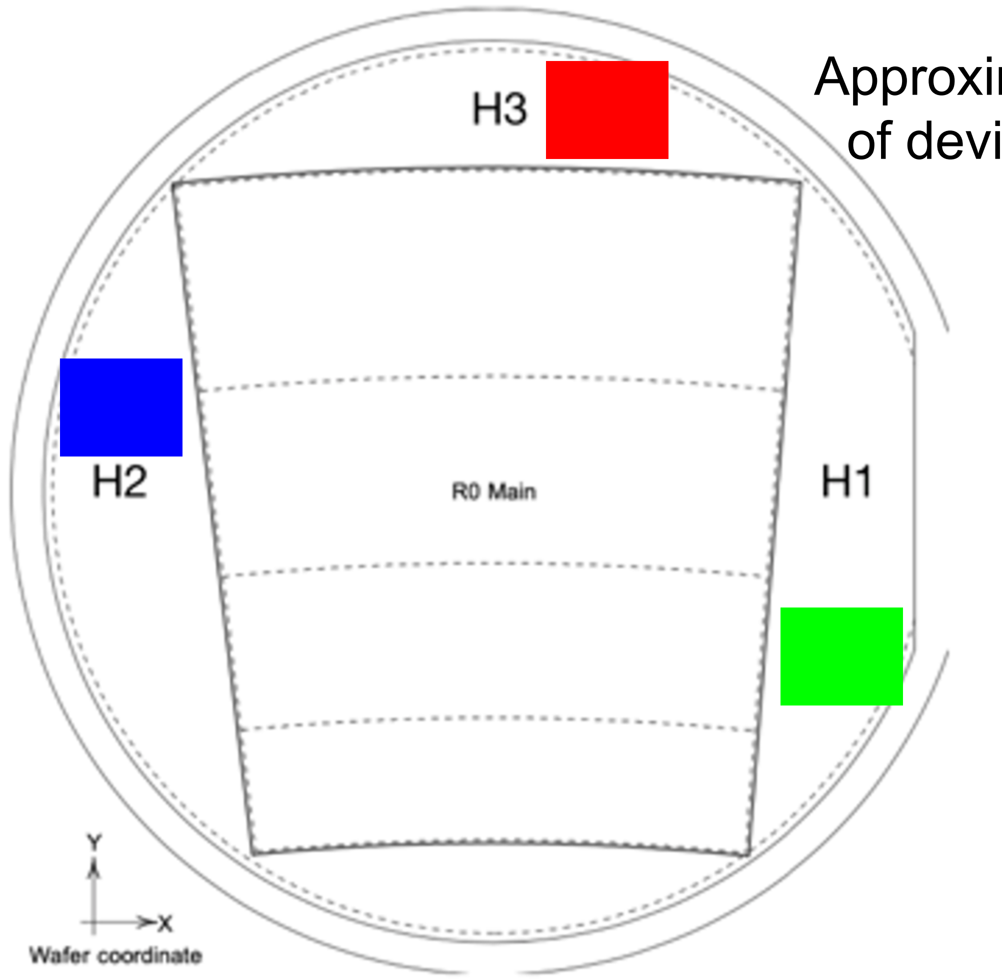


ATLAS18R3 MOS Capacitors VPX33428 - C_{ox}



ATLAS18R3 MOS Capacitors VPX32482 - C_{ox}

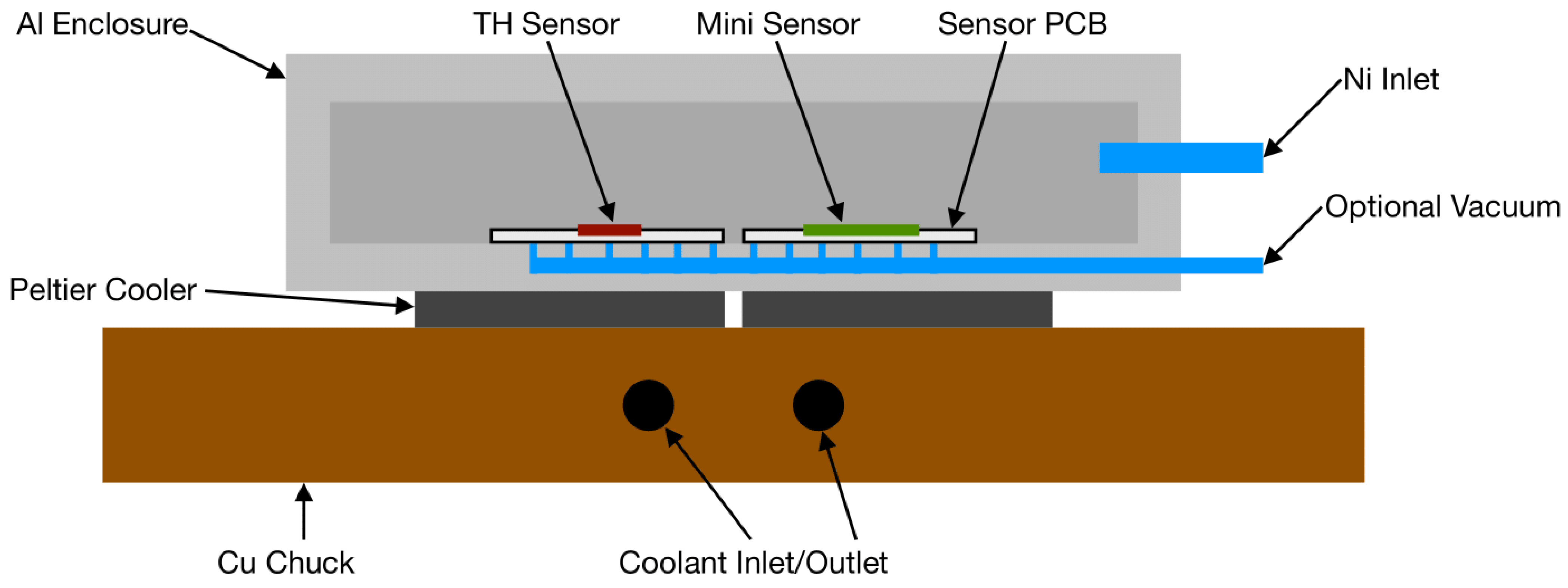


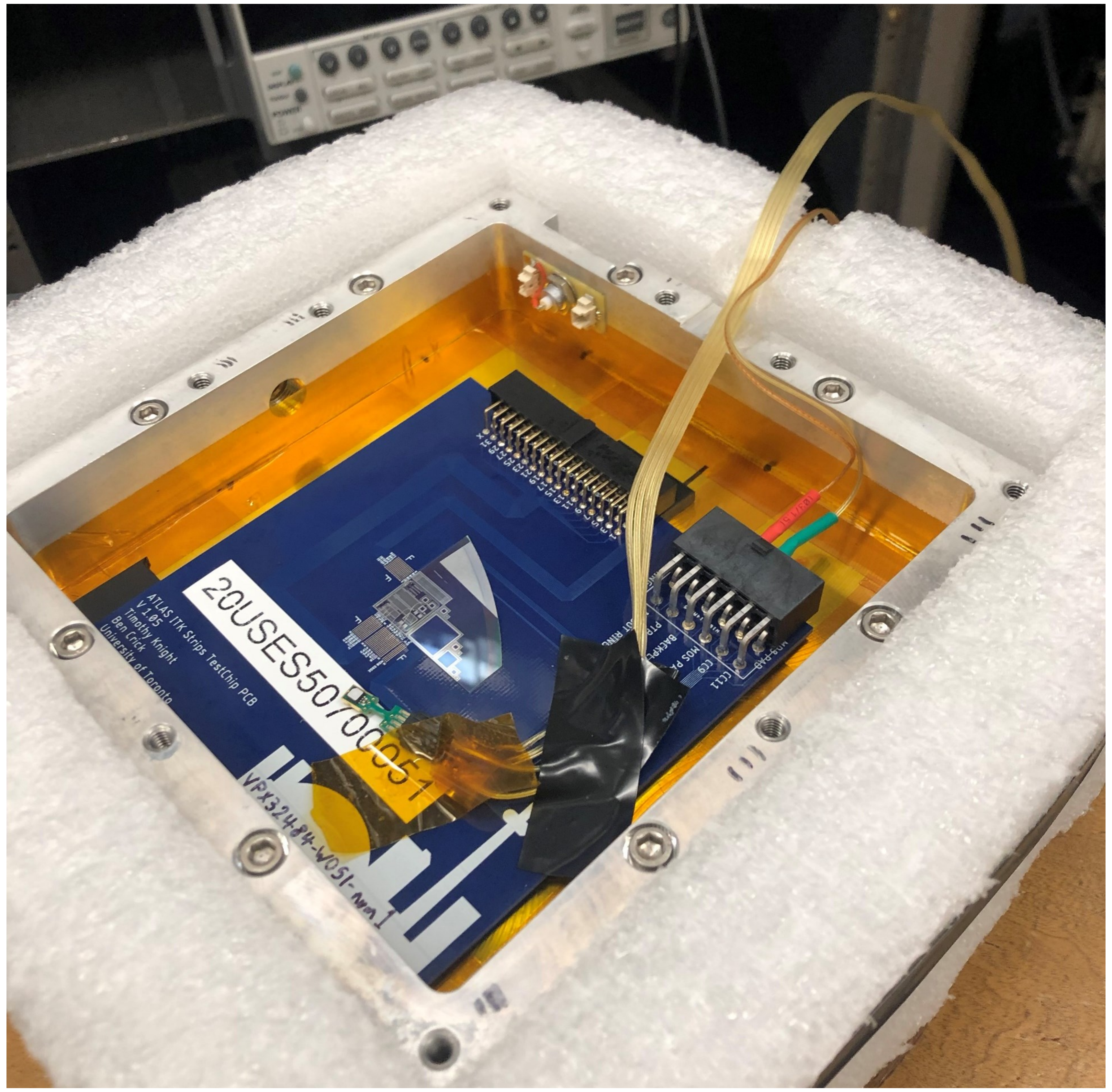


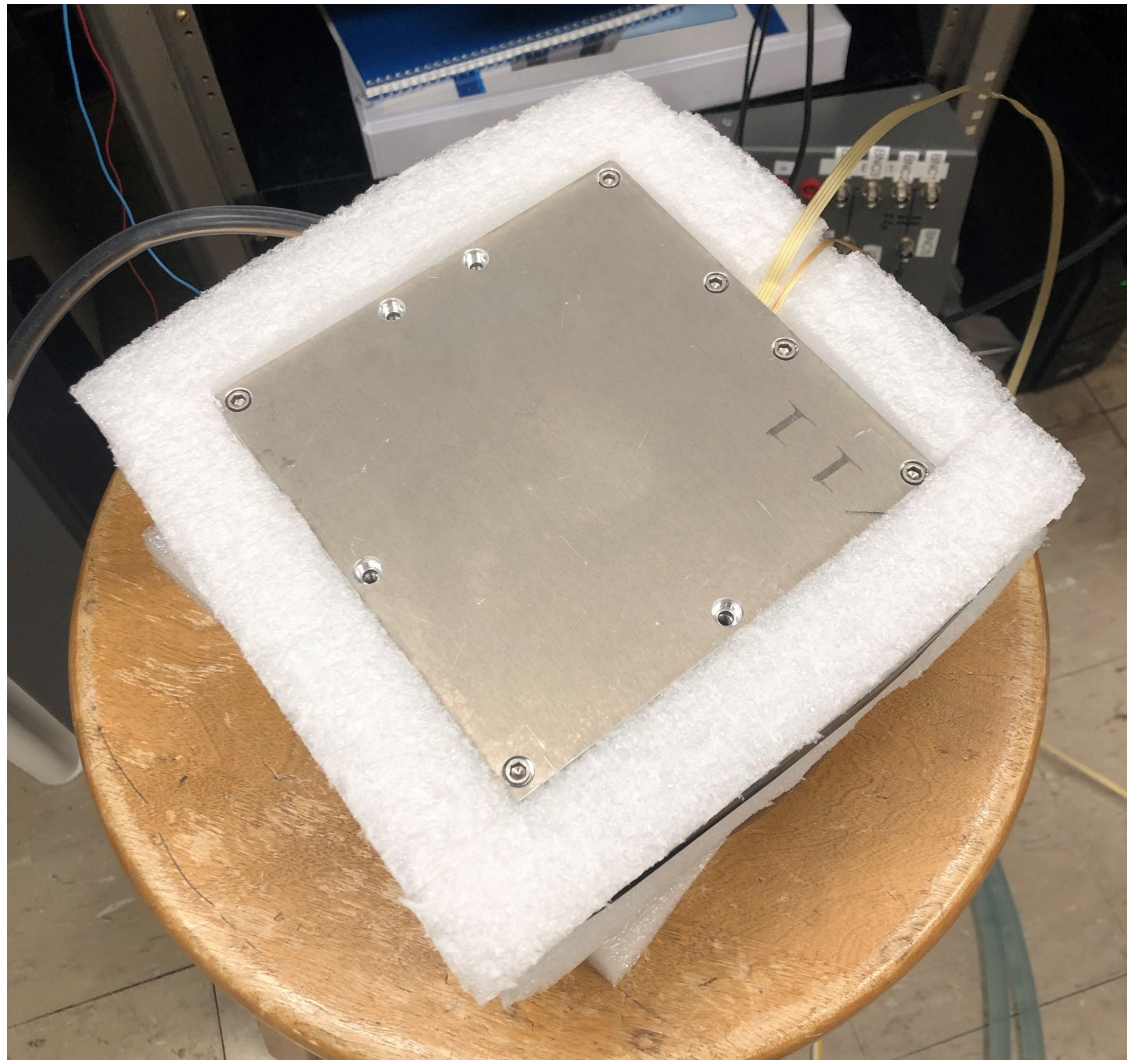
Approximate location of device on wafer

Setup – Cold Jig

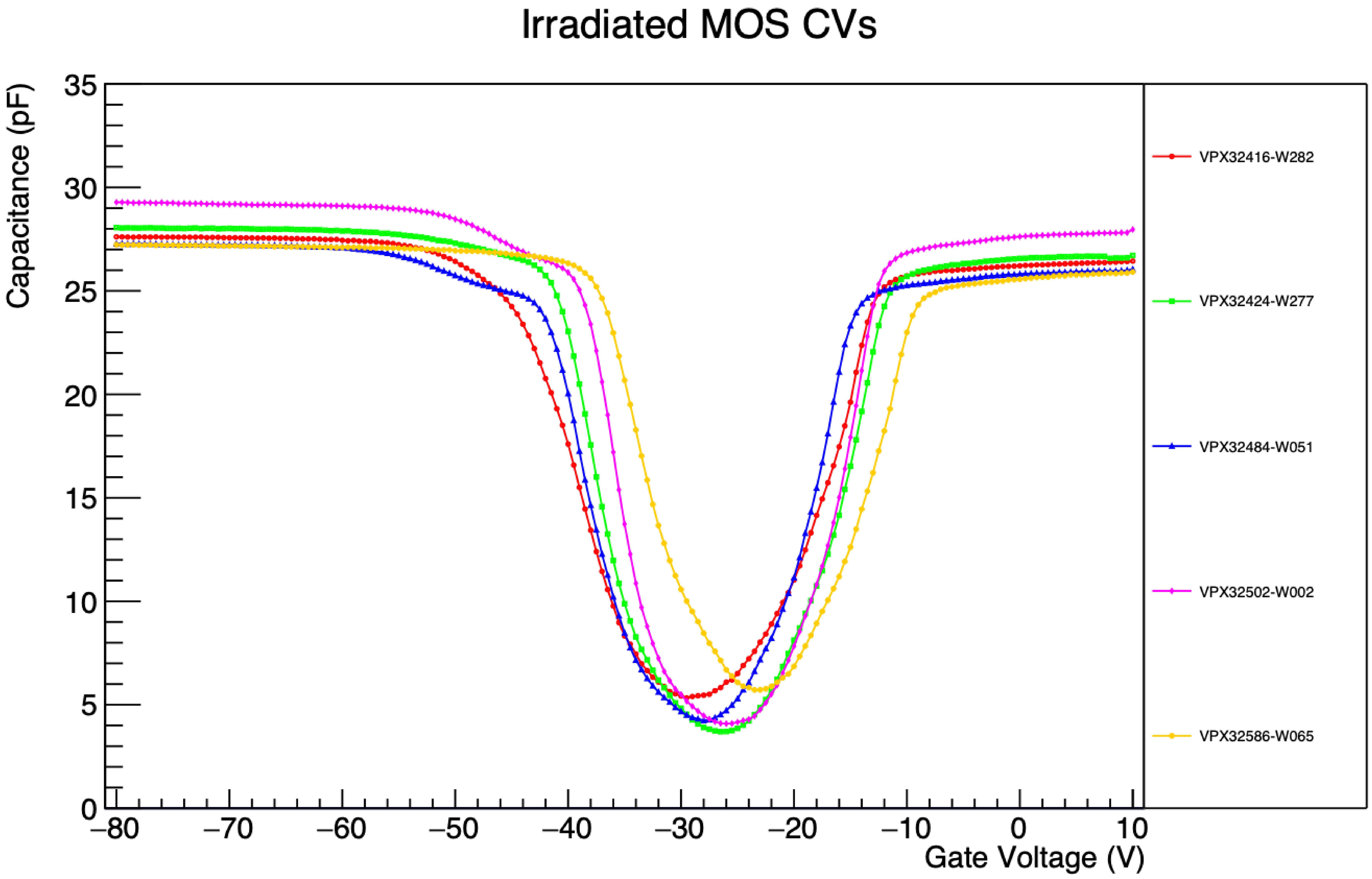
- Carleton cold jig can go to <-20C with RH <15%





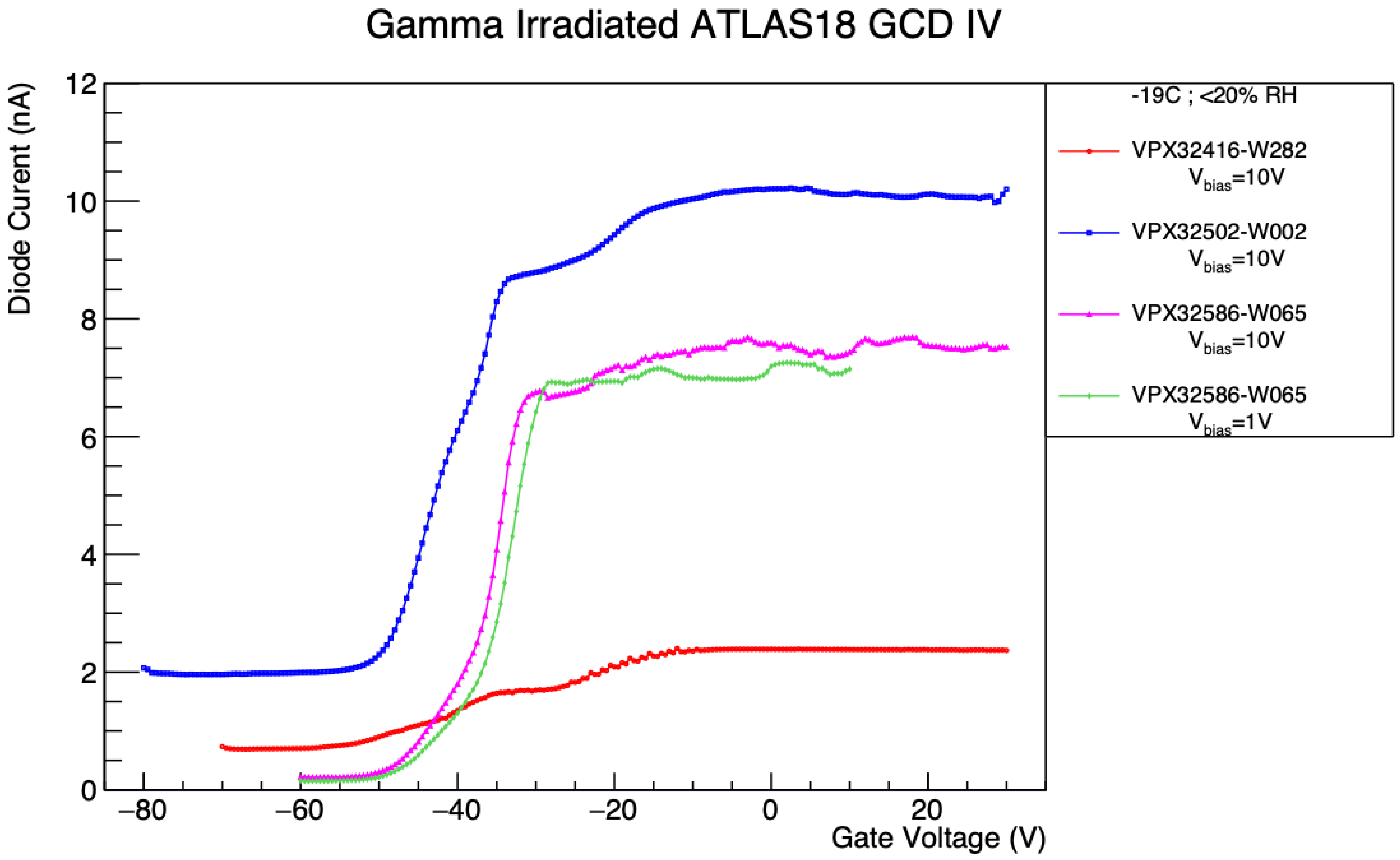


CVs of Irradiated MOS

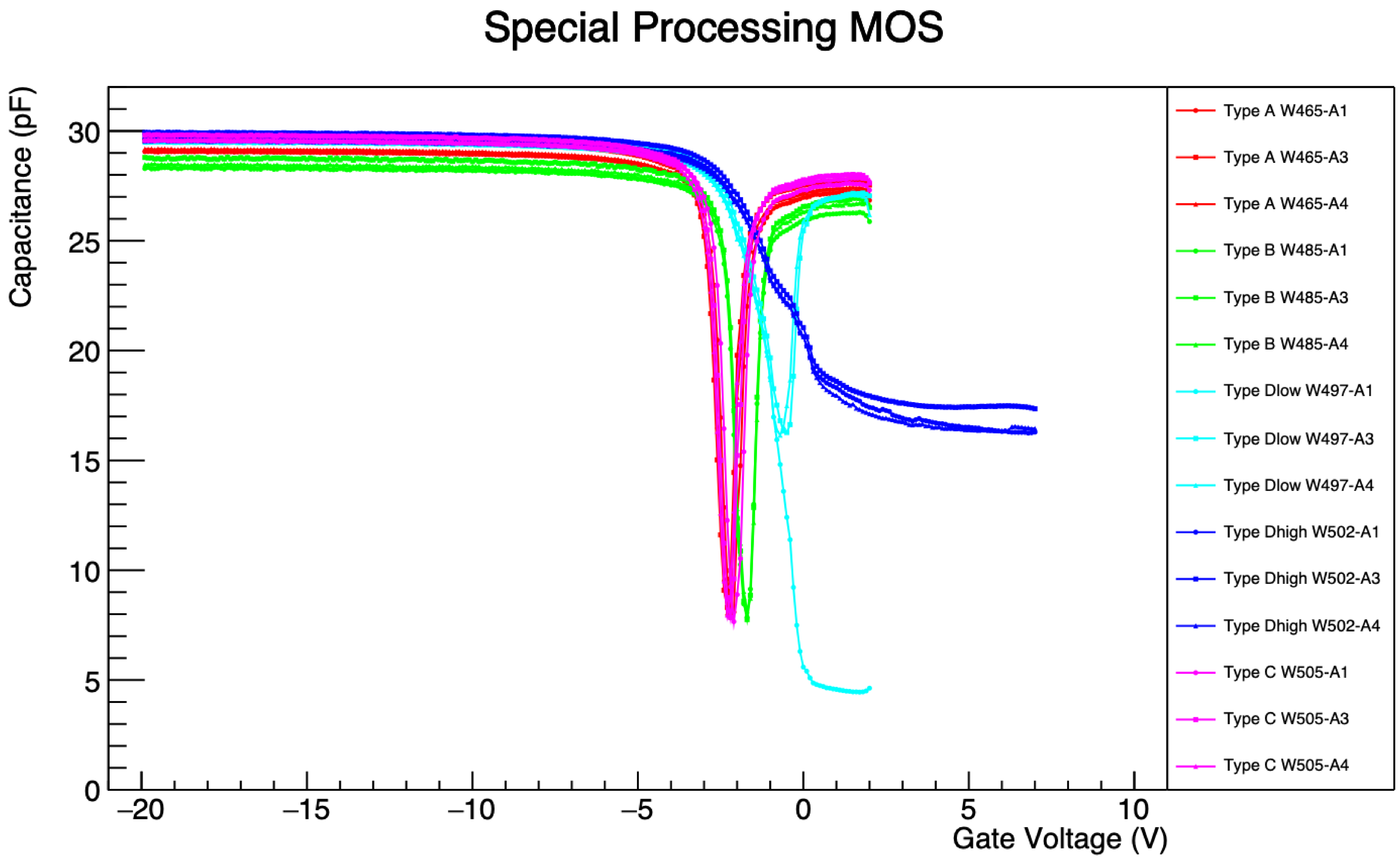


Gamma Irradiated GCD

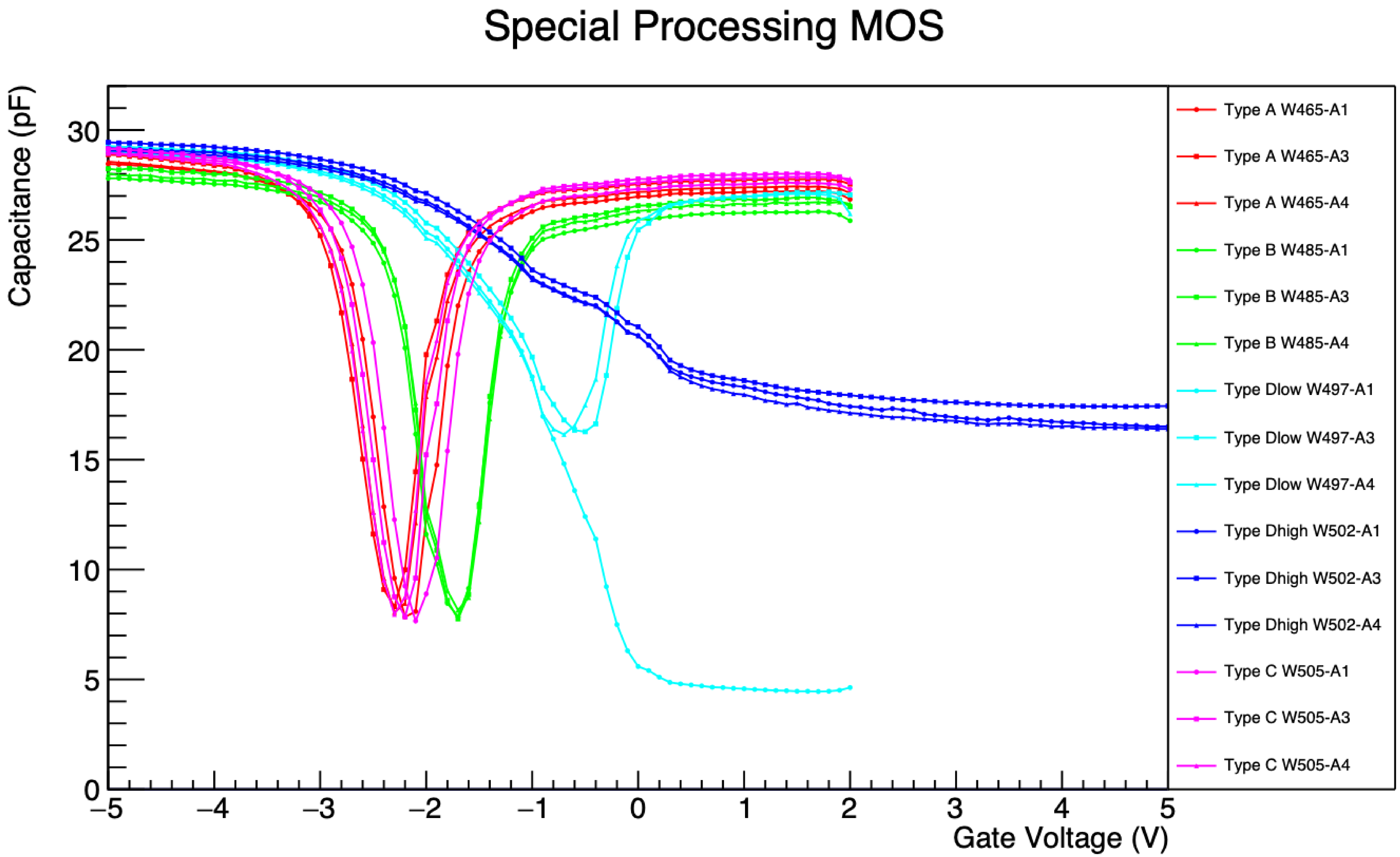
- Wire bonding is not always consistent (sometimes destructive)
- Same general shape as non-irradiated (V_{fb} shift)
- No visible onset of inversion



Full CV SP MOS



SP Wafers MOS Devices



B – Special Mask

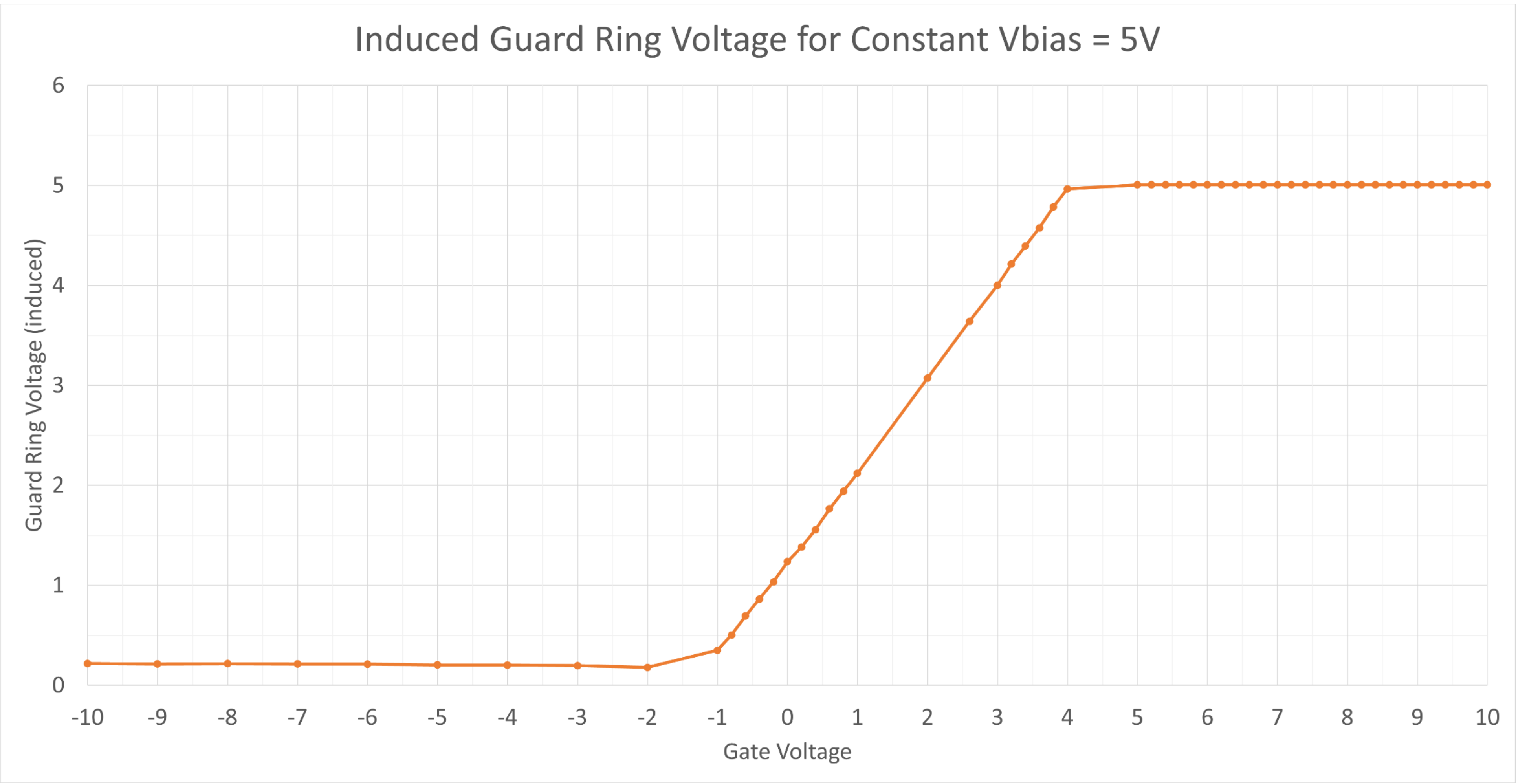
C – Thicker Pass.

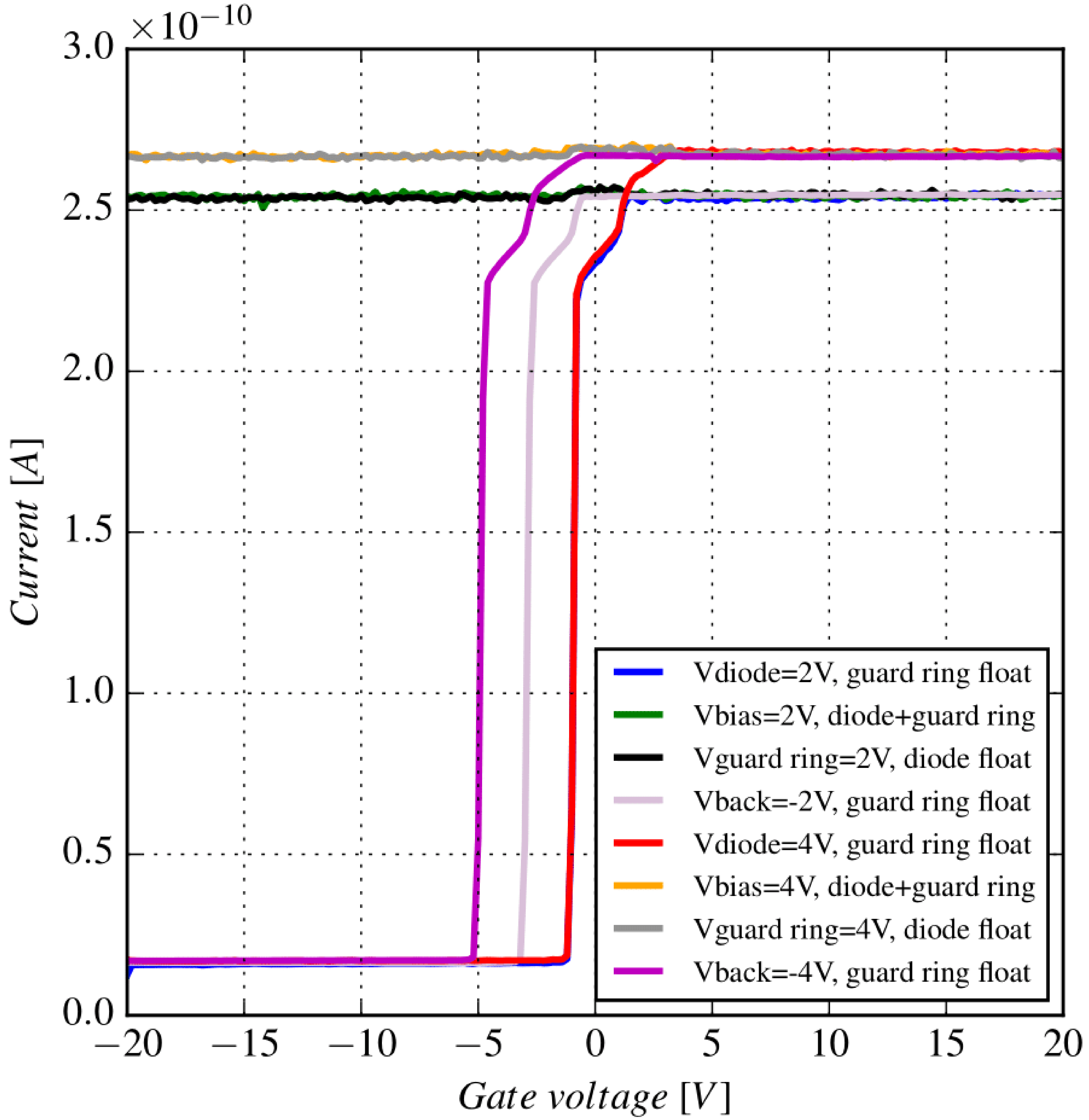
Dlow – P-spray low

Dhigh – P-spray high

More on GCD Design

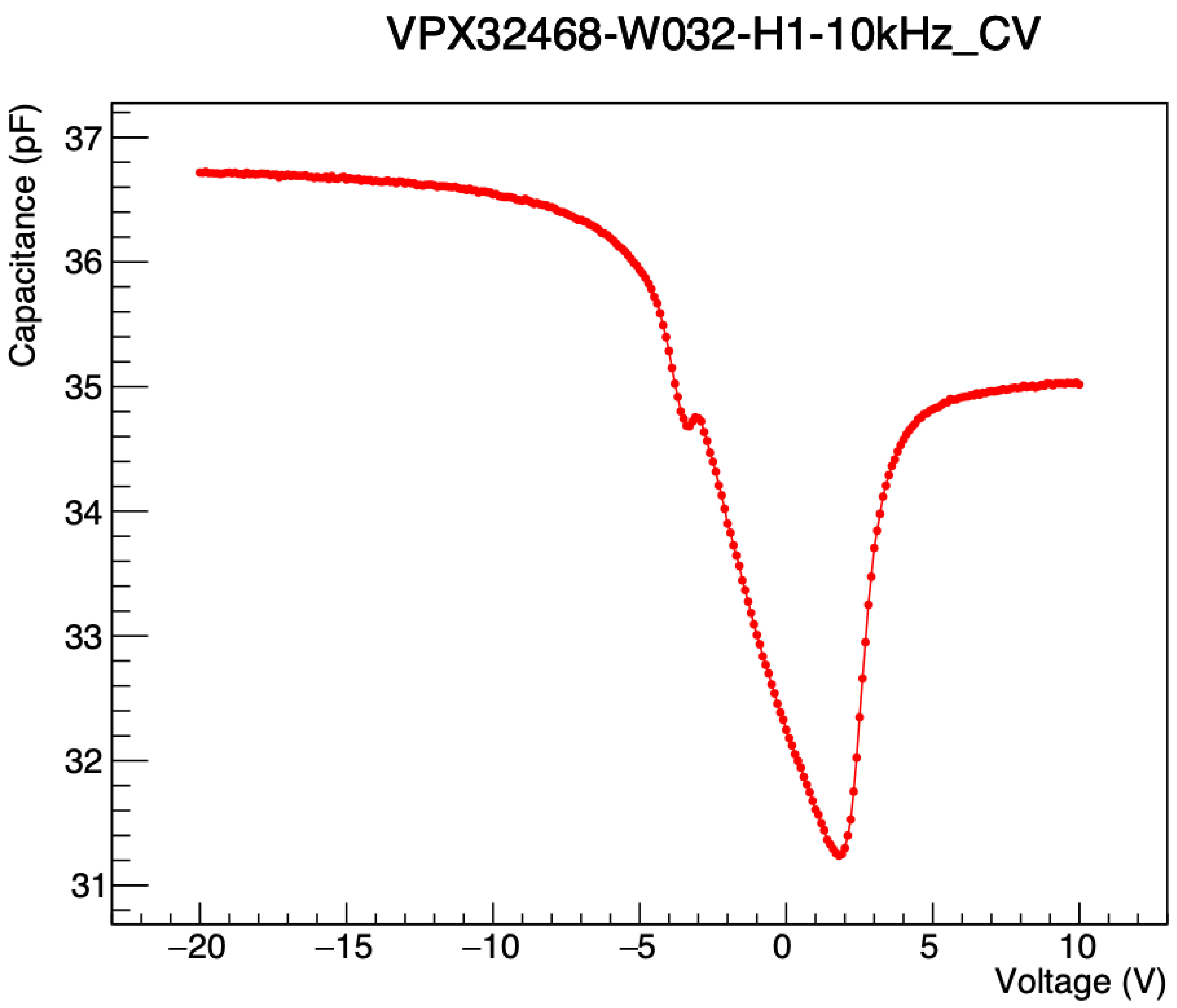
- Measurements by Ioannis (many thanks)
- High leakage whenever voltage is source to the GR, regardless of diode floating (green, black, yellow, grey)
- Always high leakage on inversion side -> Short between diode and GR



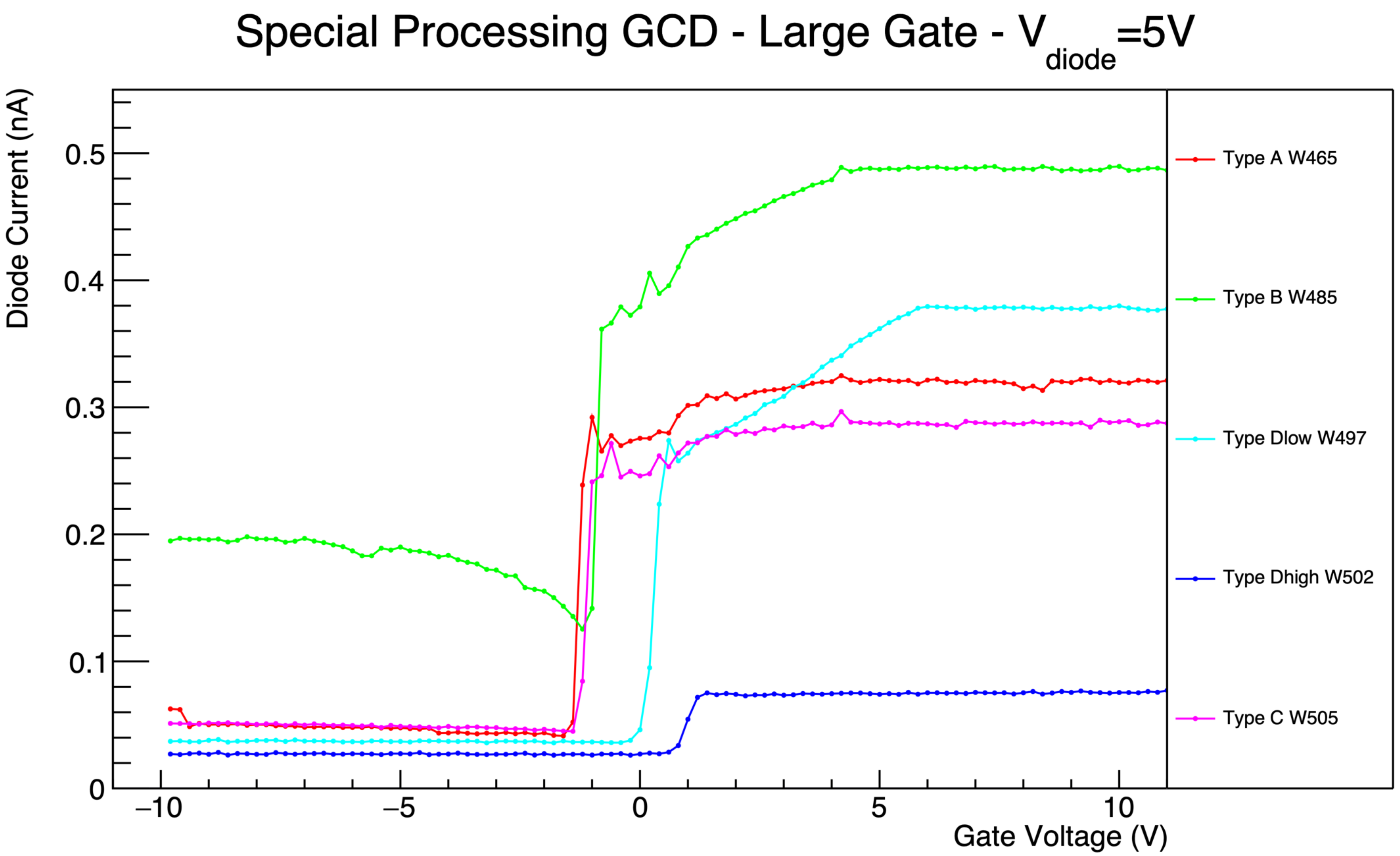


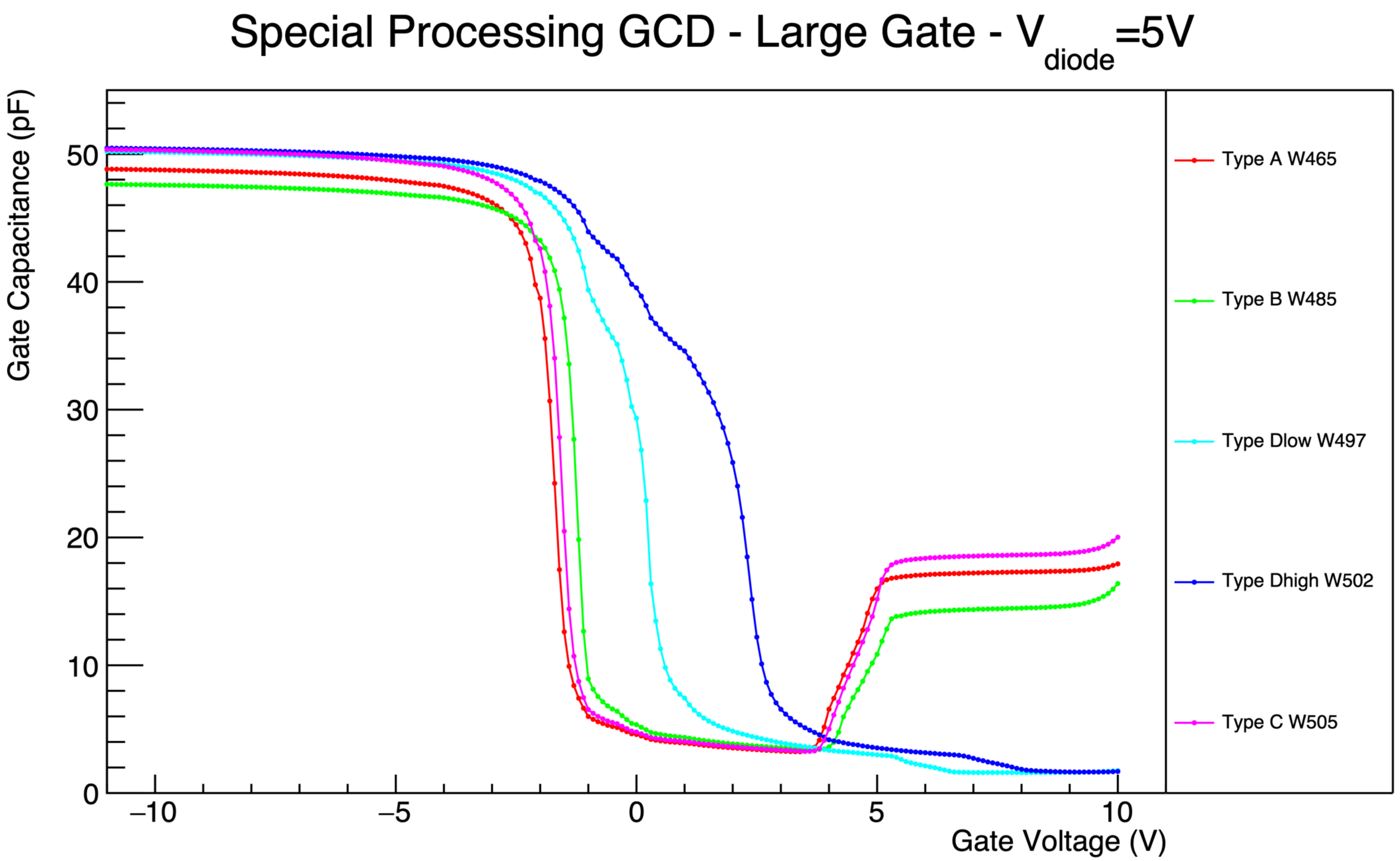
MOS Device with P-stop

- CV of MOS with p-stop
- High doping means shallow depletion depth
- Unable to extract V_{fb} without N_A
- Can still see C_{ox} and t_{ox} ; compare with regular MOS



SP Wafers GCD





- Again, IV cannot be used to extract surface recombination velocity
- CV used to establish where the onset of inversion should be

Procedure Recommendations and Thresholds

- MOS CV test parameters before irradiation: scan from +2V to -20V in 0.1V steps using 10kHz, 100mV AC test signal
- MOS CV test parameters after irradiation: scan from +10V to -80V in 0.5V steps using 1kHz, 500mV AC test signal
- Soft threshold recommendation for QA monitoring of MOS device: $C_{ox} > 25pF$, $t_{ox} < 767nm$, $V_{fb} > -5V$ (before irradiation), $V_{fb} > -40V$ (after irradiation)
- Possibility to use polysilicon gate to monitor the above parameters as well