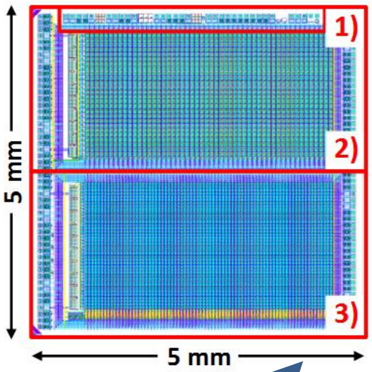
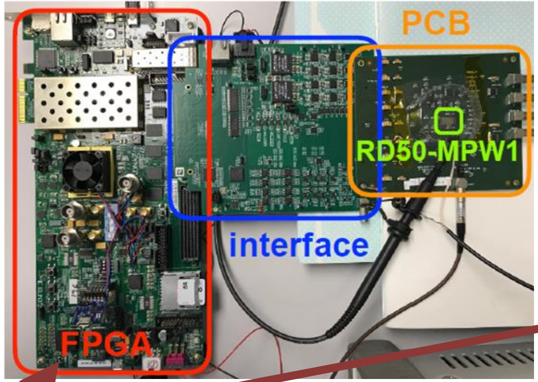
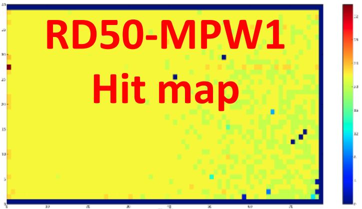
CERN-RD50 CMOS timeline

RD50-MPW1

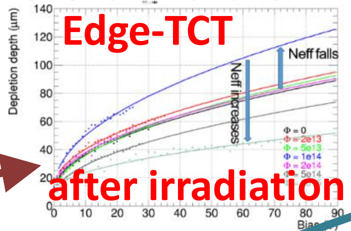


RD50 DAQ (Caribou)



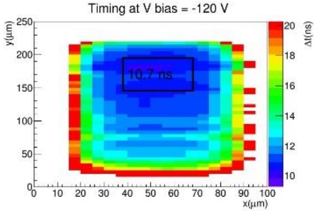


RD50-MPW1 Hit map

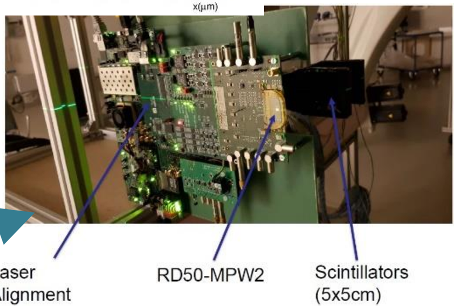


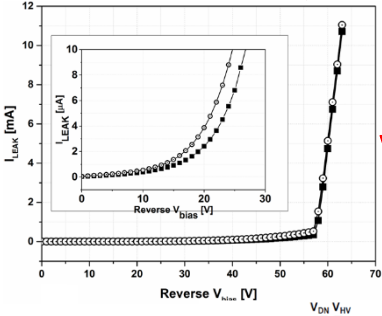
Edge-TCT

after irradiation



RD50-MPW2 Timing & test beams



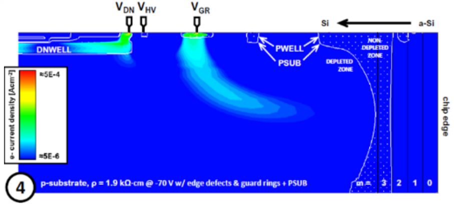


RD50-MPW1

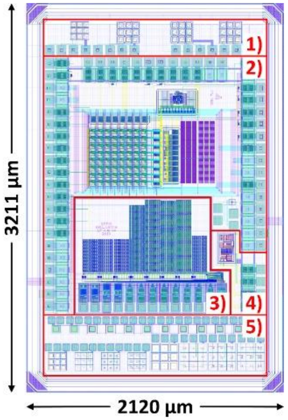
I_LEAK↑

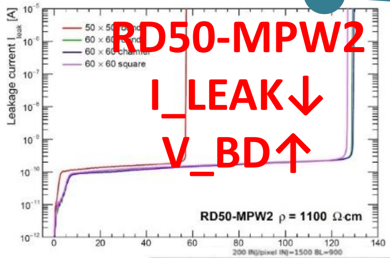
V_BD↓

TCAD



RD50-MPW2

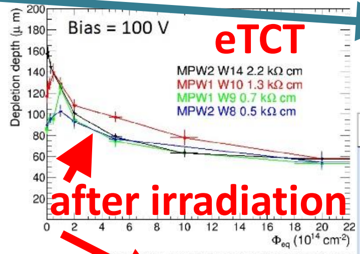




RD50-MPW2

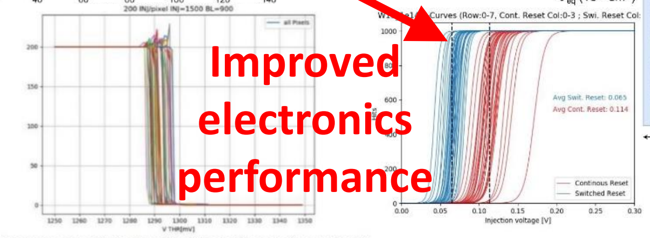
I_LEAK↓

V_BD↑



eTCT

after irradiation

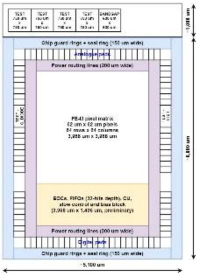


Improved electronics performance

S-curves for all pixels with threshold variation. Trim DA values adjusted. Injection amplitude 1500 mV.

Wafer 13, 1e14N_{eq}

RD50-MPW3



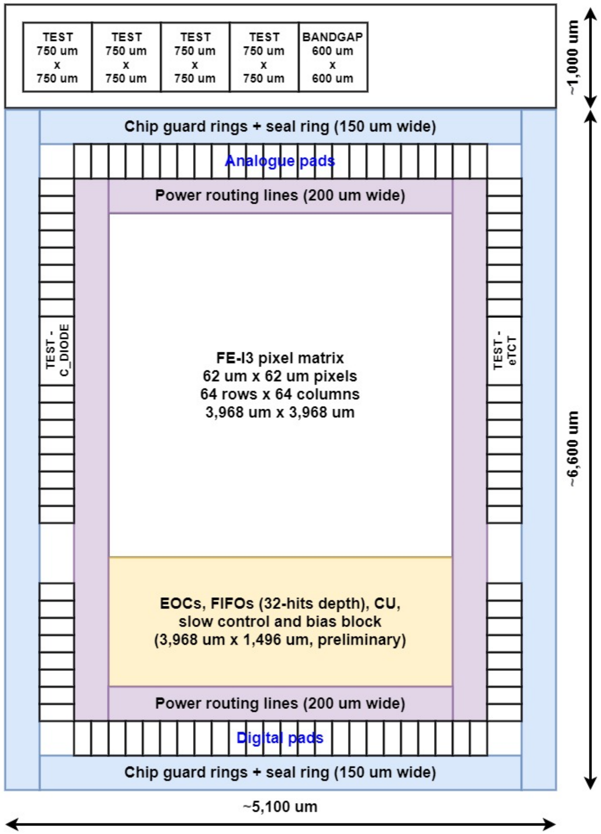
RD50-MPW3 – Motivation

RD50-MPW2

- Very successful chip, but with limitations
  - Reduced number of rows and columns (8 x 8)
  - No pixel digital readout to identify particle hits
  - Very simple TX readout → some measurements too slow or not possible

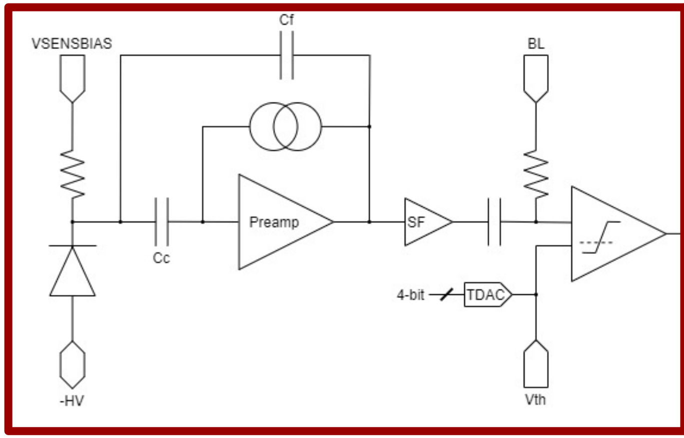
RD50-MPW3

- Larger and more advanced matrix to further study HV-CMOS sensors
  - 64 rows x 64 columns
  - With in-pixel digital readout (FE-I3 style)
  - With optimised peripheral readout for effective pixel configuration and fast data TX
  - With all the lessons learned from RD50-MPW1/2
- Chip submission in November 2021 through an MPW shuttle run
- Resistivities: standard, 1.9k and >2k Ω·cm

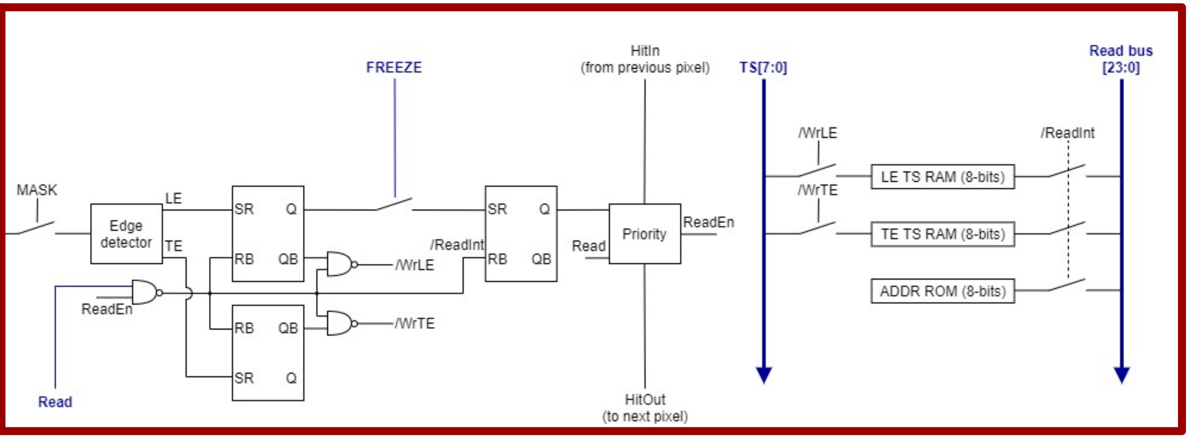


RD50-MPW3 – Pixel schematic

Analogue readout



Digital readout

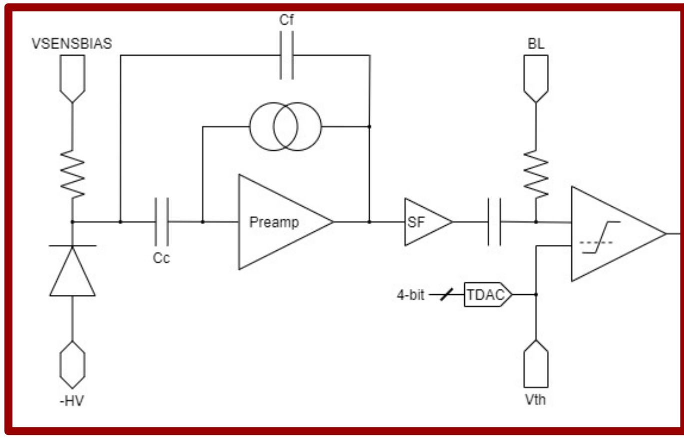


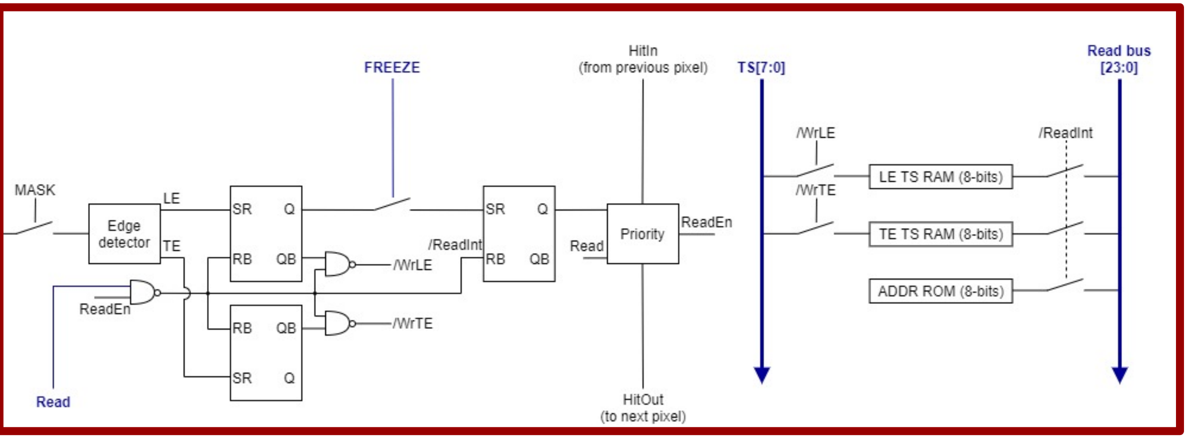
- **Analogue readout** from RD50-MPW2
- **Digital readout**, highly improved, from RD50-MPW1
- New in-pixel logic
  - To mask noisy pixels (MASK)
  - New priority circuit for less-area consuming alternative
  - Possibility to pause digitisation of new hits until readout is complete (FREEZE)
  - **8-bit SRAM shift register** for serial configuration
    - Pixel-trimming to compensate for threshold voltage variations (4-bits)
    - Flag to mask noisy pixels (1-bit)
    - Signals to enable/disable calibration circuit (1-bit), SF output (1-bit), COMP output (1-bit)

RD50-MPW3 – Pixel schematic

Analogue readout

Digital readout





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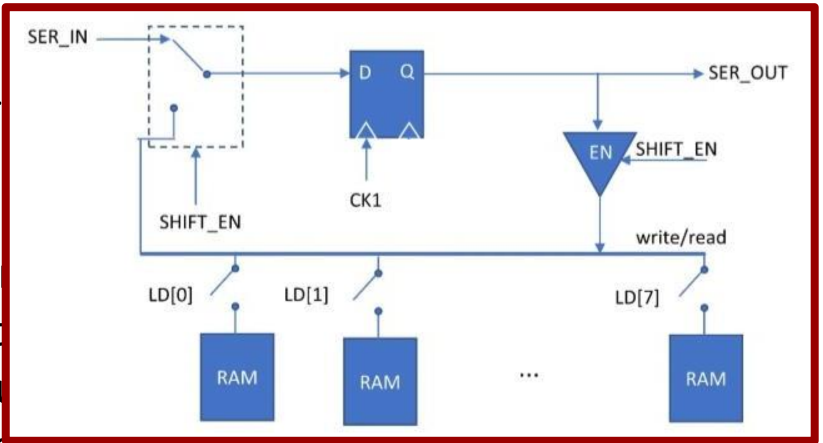
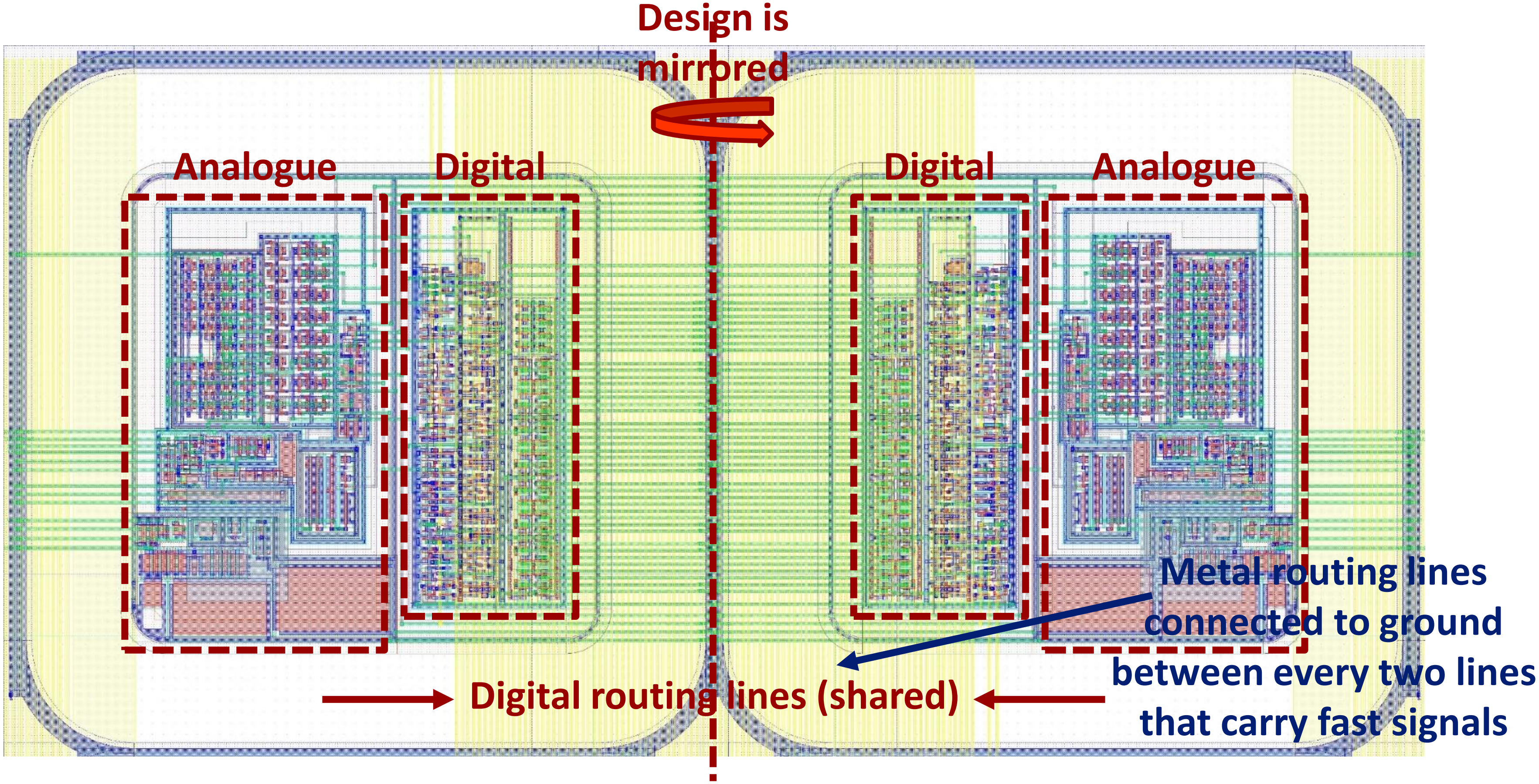


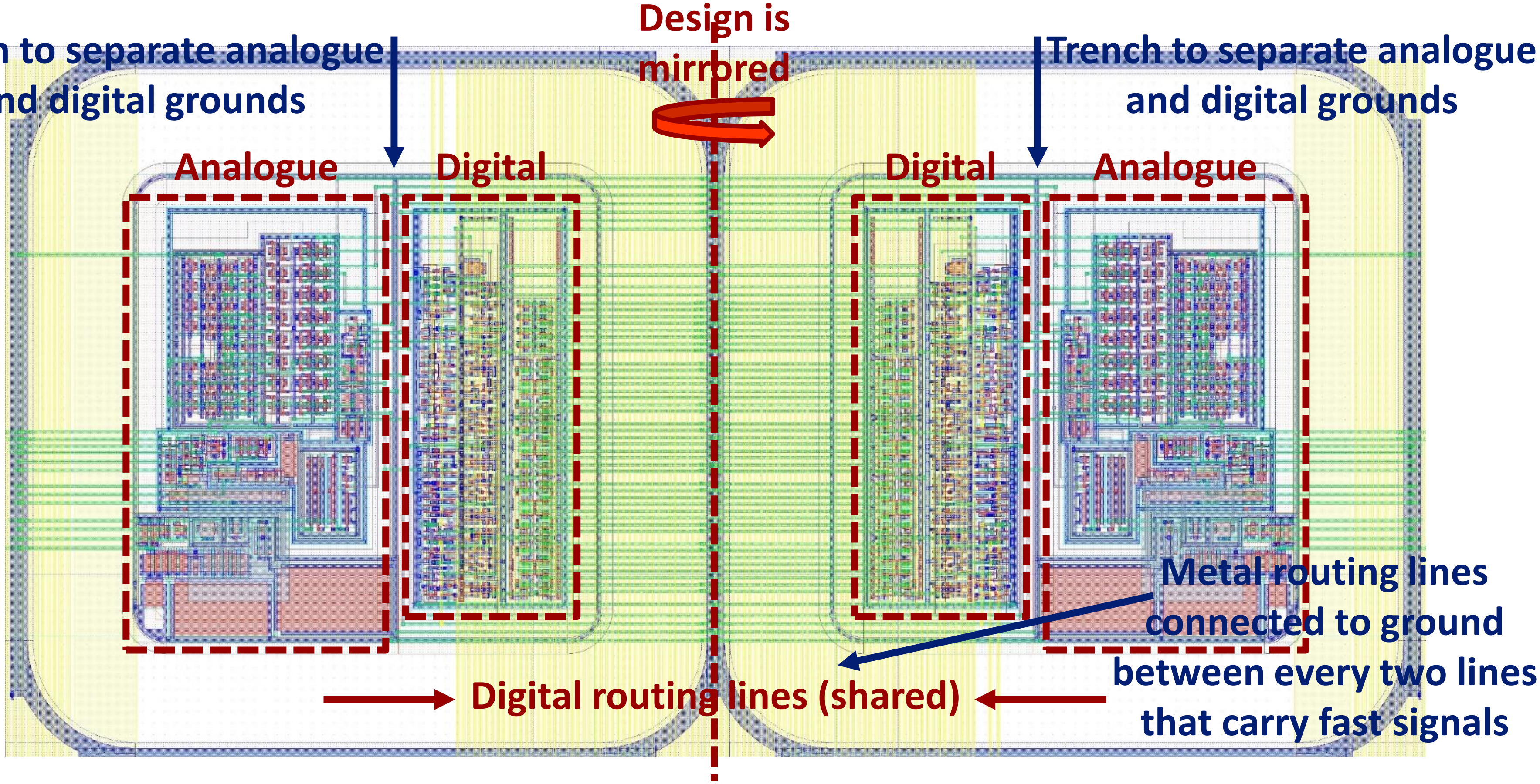
R. Casanova, 38th RD50 WS

RD50-MPW3 – Pixel layout



- <u>**Double column scheme to alleviate routing congestion and minimise crosstalk**</u>
  - Pixels within double column share many signals → ~ x0.5 less routing lines
    - Digital input/outputs (TS IN, TS OUT, ADDR), control signals (Read, Freeze, etc.)
- Pixel size is 62 µm x 62 µm

RD50-MPW3 – Pixel layout



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- Pixel size is 62 µm x 62 µm

RD50-MPW3 – EOC + readout + slow control

New EOC architecture - Components

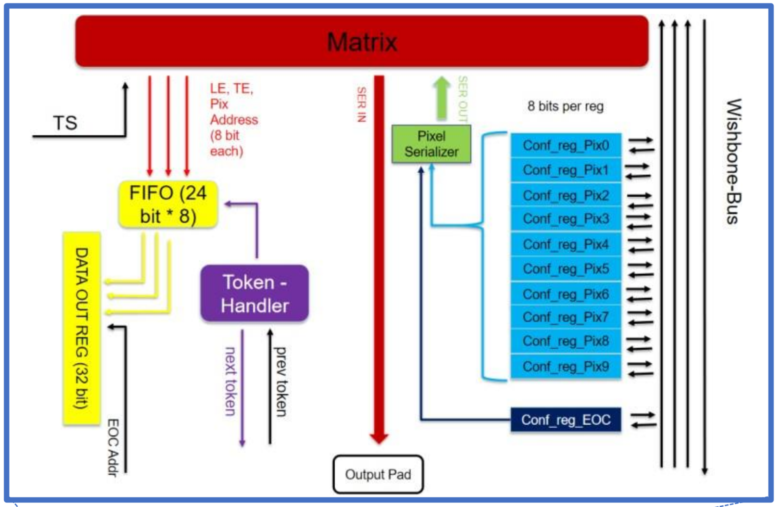
- FIFO stores hit data (LE TS, TE TS and ADDR)
- FSM reads double column
- Token mechanism to determine which EOC is read out

Readout

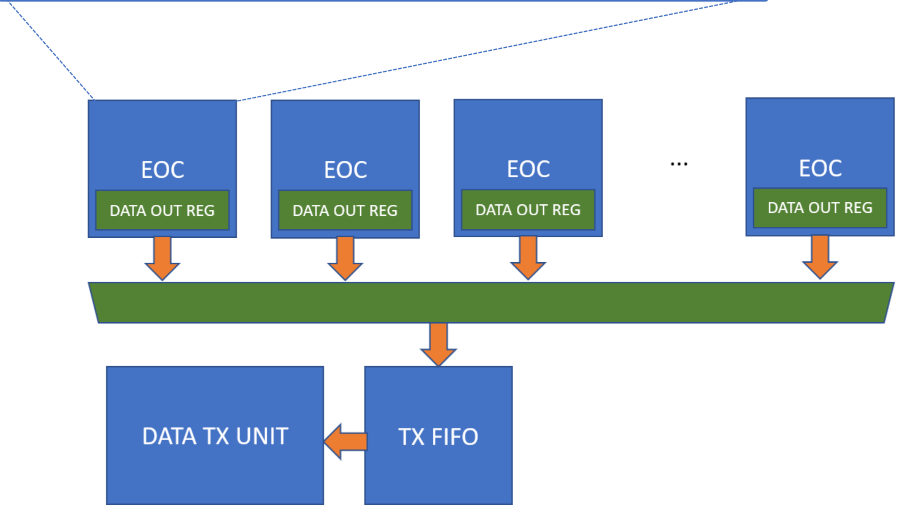
- Pixel is read out immediately after hit (if FIFO is not full)
- CU reads EOCs sequentially
- Data stored temporarily in TX FIFO
- Data TX unit with LVDS port @ 640 Mbps

Slow control

- Based on I2C protocol for external communication using internal Wishbone bus



P. Sieberer



CONTROL UNIT

R. Casanova, 38th RD50 WS

RD50-MPW3 – Status

Logistics

- Funding request
  - With 11 RD50 institutes
  - Submitted to and approved by RD50
- PO
  - Sent from CERN to the foundry
  - This is always an adventure…

Design & submission

- We have encountered a number of last minute issues
  - Design team is working very hard to solve them in due time
- Deadline to submit is Monday 22.11.21 (although the foundry has confirmed they can manage a few days delay)

CERN-RD50 CMOS – Milestones

- **RD50 prolongation request – May 2018**
  - **M1:** Characterization of the diodes and readout electronics of unirradiated and irradiated RD50-MPW1 samples (Q4/2018) → **Achieved**
    - **M1.2 (new):** Design and submission of RD50-MPW2 (Q1/2019) → **Achieved**
    - **M1.3 (new):** Characterization of unirradiated and irradiated RD50-MPW2 samples (Q1/2020 → Q3/2021) → **Achieved**
    - **M1.4 (new):** Design and submission of RD50-MPW3 (Q4/2021) → **Ongoing**
  - **M2:** Design and submission for fabrication of RD50-ENGRUN1 (Q4/2018)
  - **M3:** Characterization of unirradiated and irradiated RD50-ENGRUN1 samples (Q3/2019, Q3/2020)
  - **M4:** Characterization of irradiated backside biased RD50-ENGRUN1 samples for operation beyond 10^{16} n_{eq}/cm (Q4/2020)
  - **M5:** Studies of stitching process options (Q4/2021)
  - **M6:** Characterization of unirradiated and irradiated stitched samples (Q4/2022)