# Progress in CMOS SPADs and digital SiPMs for fast timing applications

Claudio Bruschini and Edoardo Charbon

Francesco Gramuglia, Emanuele Ripiccini, Andrada Muntean

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* École Polytechnique Fédérale de Lausanne

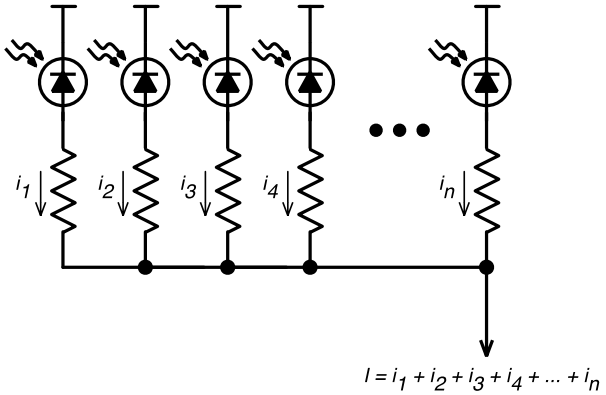
# Outline

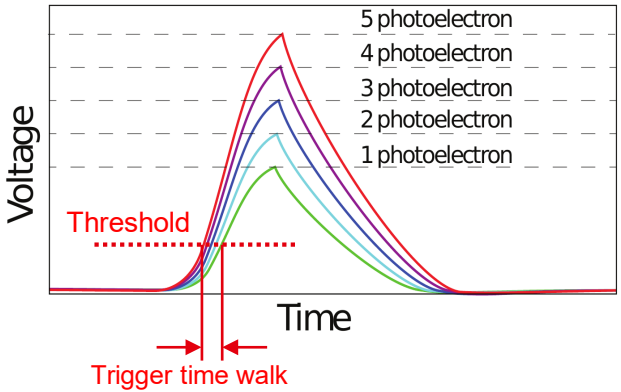


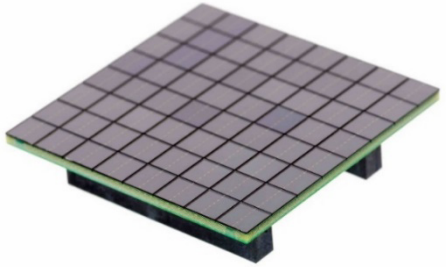


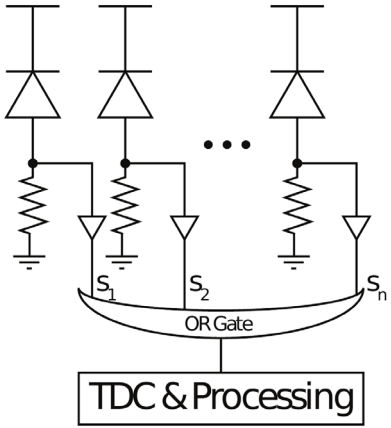
- Introduction
- Sub-10 ps FWHM SPADs
- 3D-stacked multi-digital SiPMs
- Conclusions

# Analog vs. Digital Silicon Photomultiplier

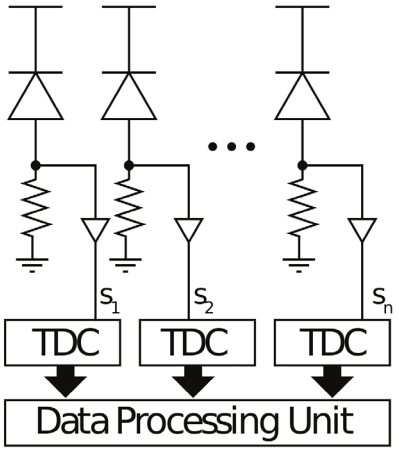


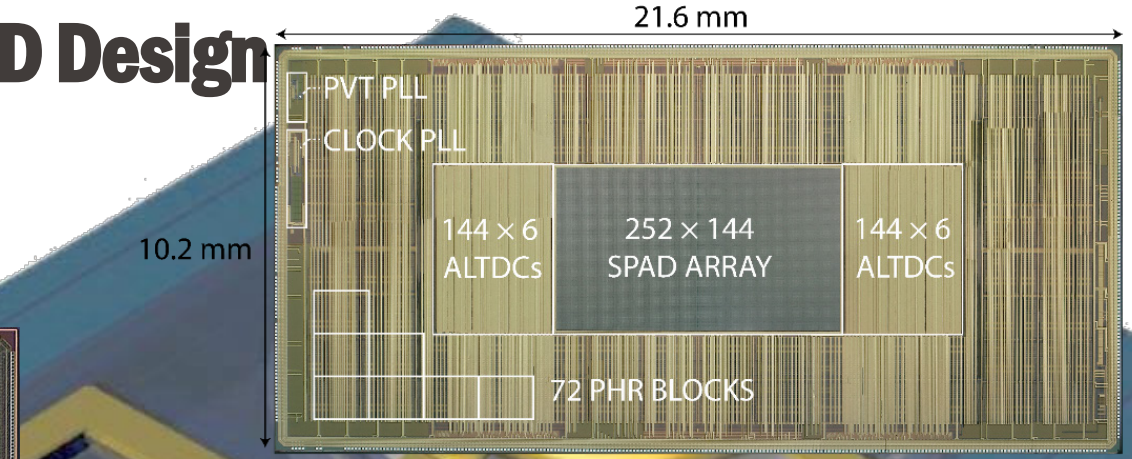


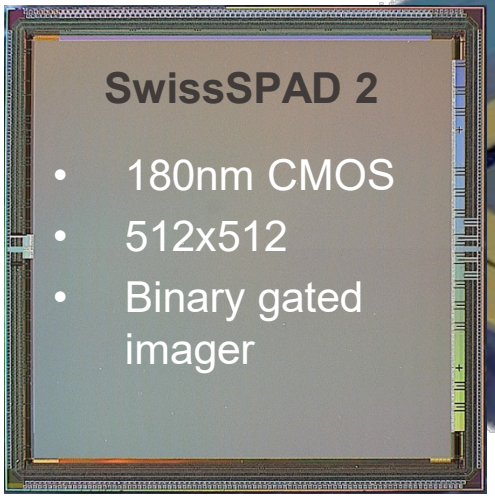

Standard dSiPM




Ideal dSiPM

# AQUA – SPAD Design Examples



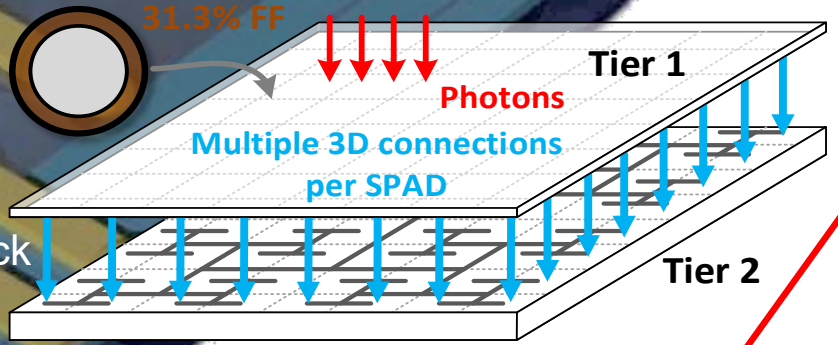



**SwissSPAD 2**

- 180nm CMOS
- 512x512
- Binary gated imager

- 180nm CMOS
- 11.2 Gbit/s output data bandwidth

**Mantis**




- 45nm/65nm CMOS 3D stack

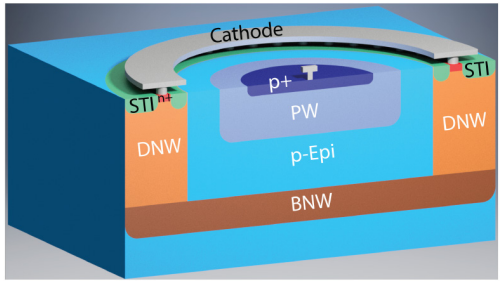
- First 3D stacked direct time-of-flight sensor in CMOS

# Introduction – Timing in SPADs and SiPMs

# Routes to high timing precision

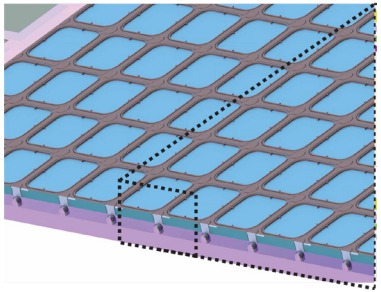
## SPAD Devices

- Design & optimization
- Enhance PDP and jitter
- Move to smaller nodes



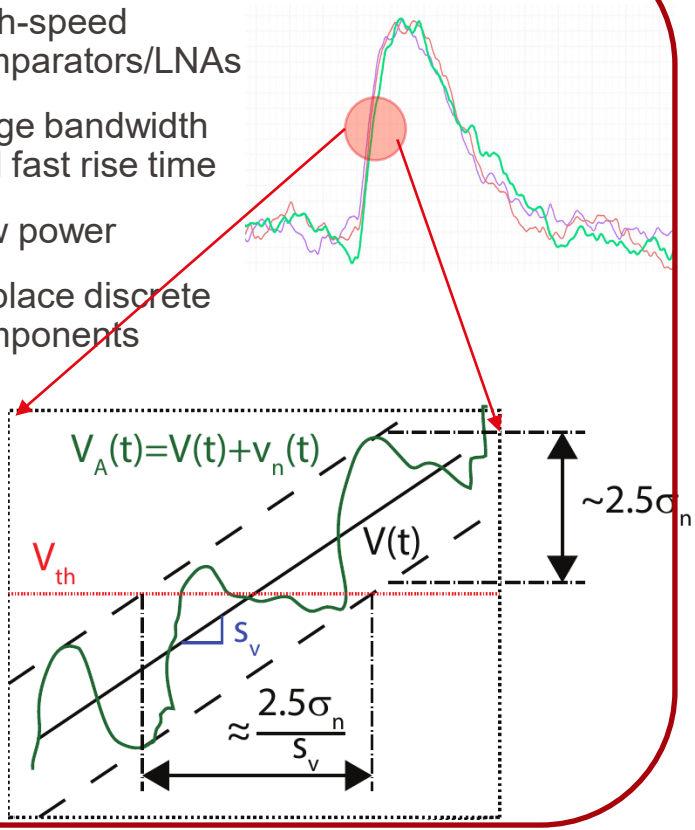

## Sensor architecture, intelligence & technology

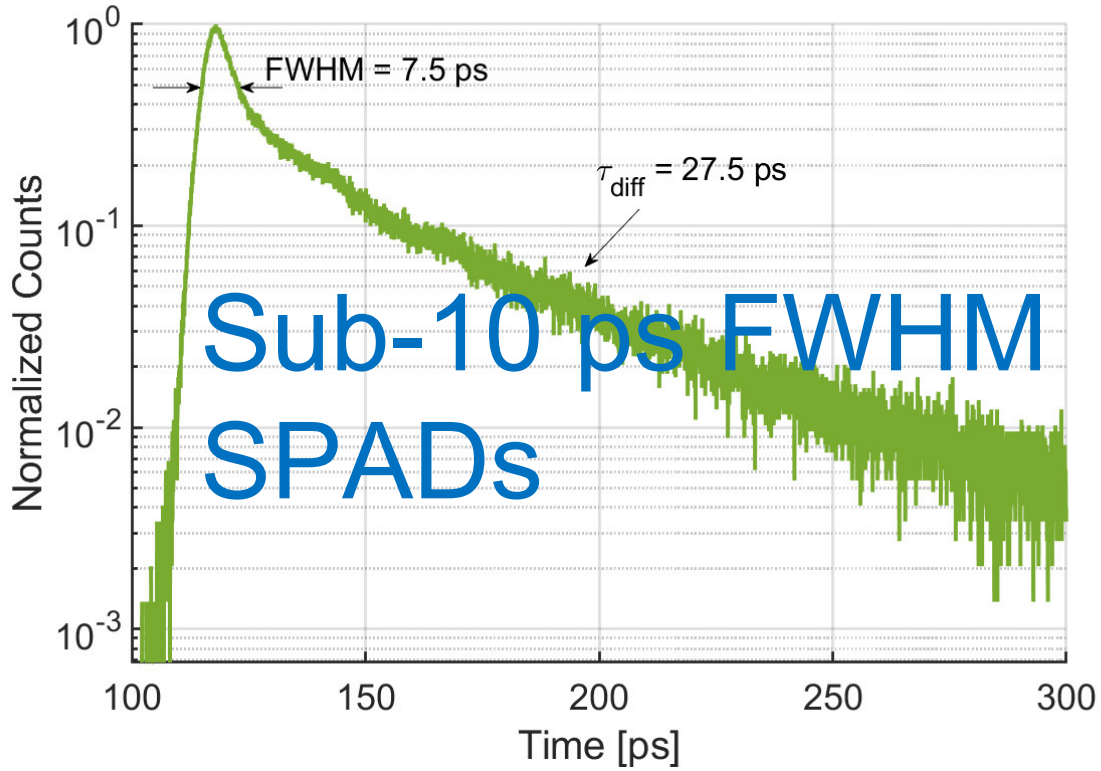
- Increase granularity -> clusters (lower capacitance load)
- Bring TDCs on-chip
- Exploit multiple time-stamps (order statistics)
- 3D-stacked SPAD arrays



## Front-end electronics

- High-speed comparators/LNAs
- Large bandwidth and fast rise time
- Low power
- Replace discrete components

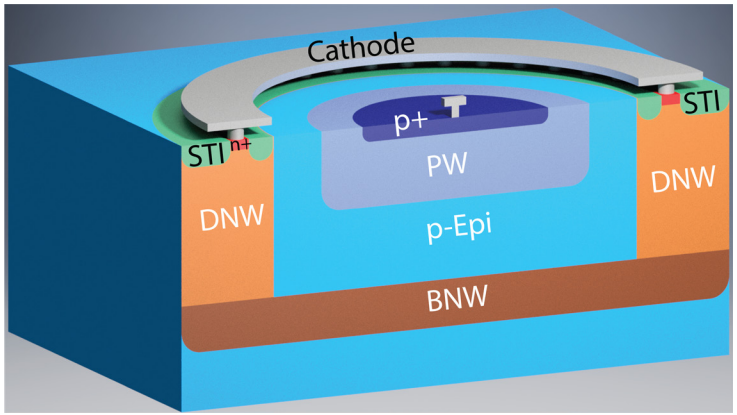



FWHM = 7.5 ps
$\tau_{diff}$ = 27.5 ps
Sub-10 ps FWHM SPADs
Normalized Counts
$10^{0}$
$10^{-1}$
$10^{-2}$
$10^{-3}$
100
150
200
250
300
Time [ps]

# SPAD structure

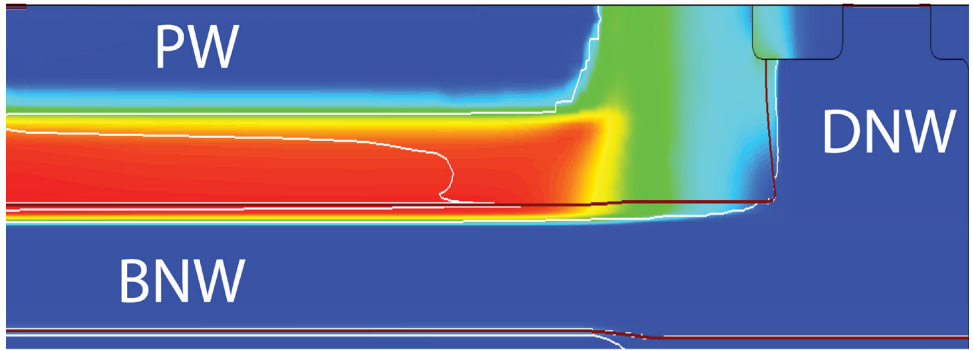


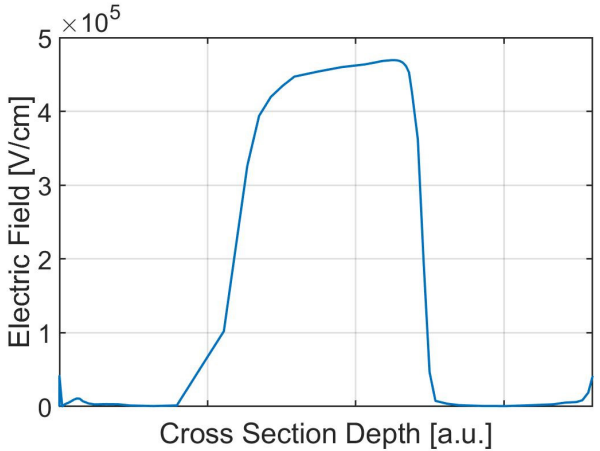





SPAD

- 180 nm CMOS technology
- P-I-N structure
- Substrate-Isolated type
- P-well anode, buried N-well cathode
- HV provided through a deep N-well

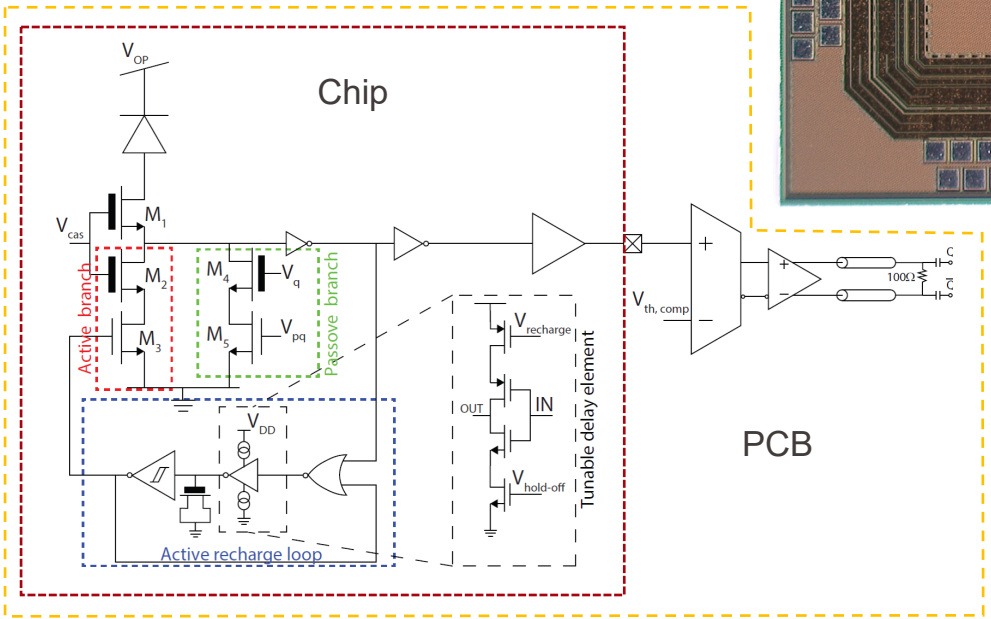


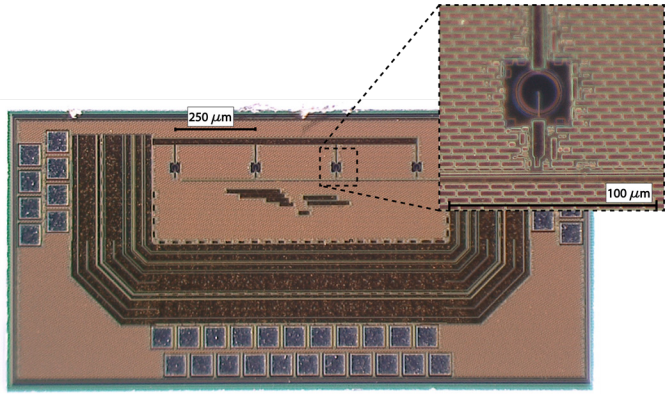




F. Gramuglia, *et al.*, “A low-noise CMOS SPAD pixel with 12.1 ps SPTR and 3 ns dead time”, IEEE JSTQE, 2021.

# SPAD & chip structure and read-out PCB

## No pre-amplifier




Size: ~149.6 μm$^2$

Chip:

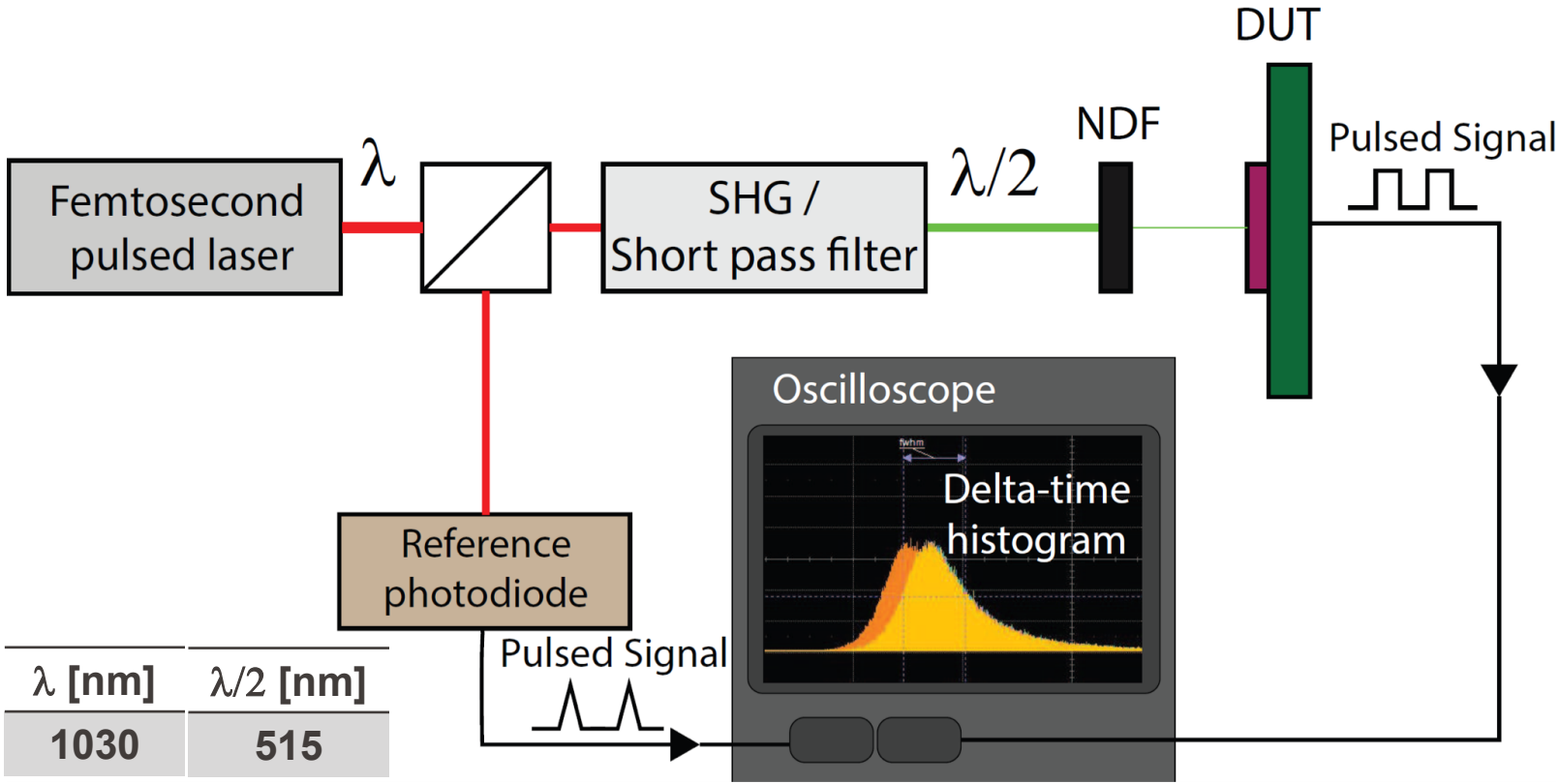
- 25 μm diameter CMOS SPAD
- Passive quenching and active reset circuit
- Tunable dead time (down to 3 ns)

System-on-board:

- Single external power supply source
- All voltages provided through DACs controlled with serial protocol, reduced cable noise
- Si-Ge comparator for 50 Ohm coupling
- High signal slew rate (≥ 1.6 V/ns)

- Lindner, *et al.* IEEE EDL 2018, F. Gramuglia, *et al.*, JSTQE 2021

# Optical Setup




| λ [nm] | λ/2 [nm] |
|---|---|
| 1030 | 515 |
| 1560 | 780 |

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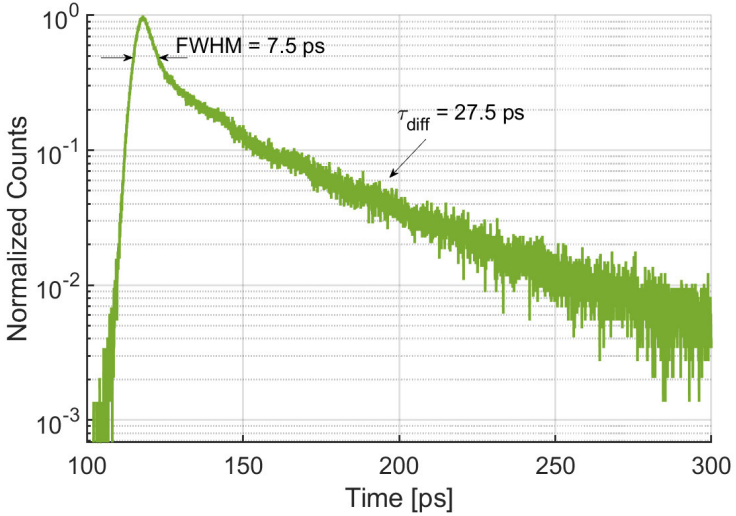
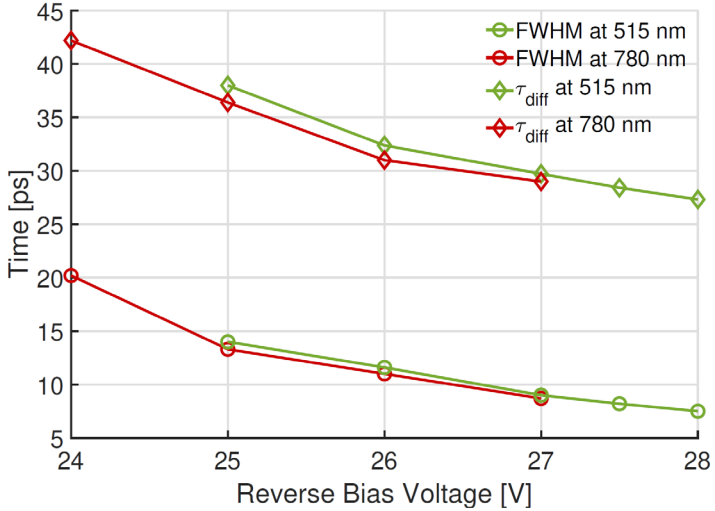
# Optical measurements (SPTR)




- **Jitter of 7.5 ps FWHM at 6.5 Vex for green light, diffusion tail: $\tau$ = 27.5 ps**
- **Jitter of 8.5 ps FWHM at 5.5 Vex for red light**

***(First results @NSS-MIC 2021: 12.1 ps FWHM)***



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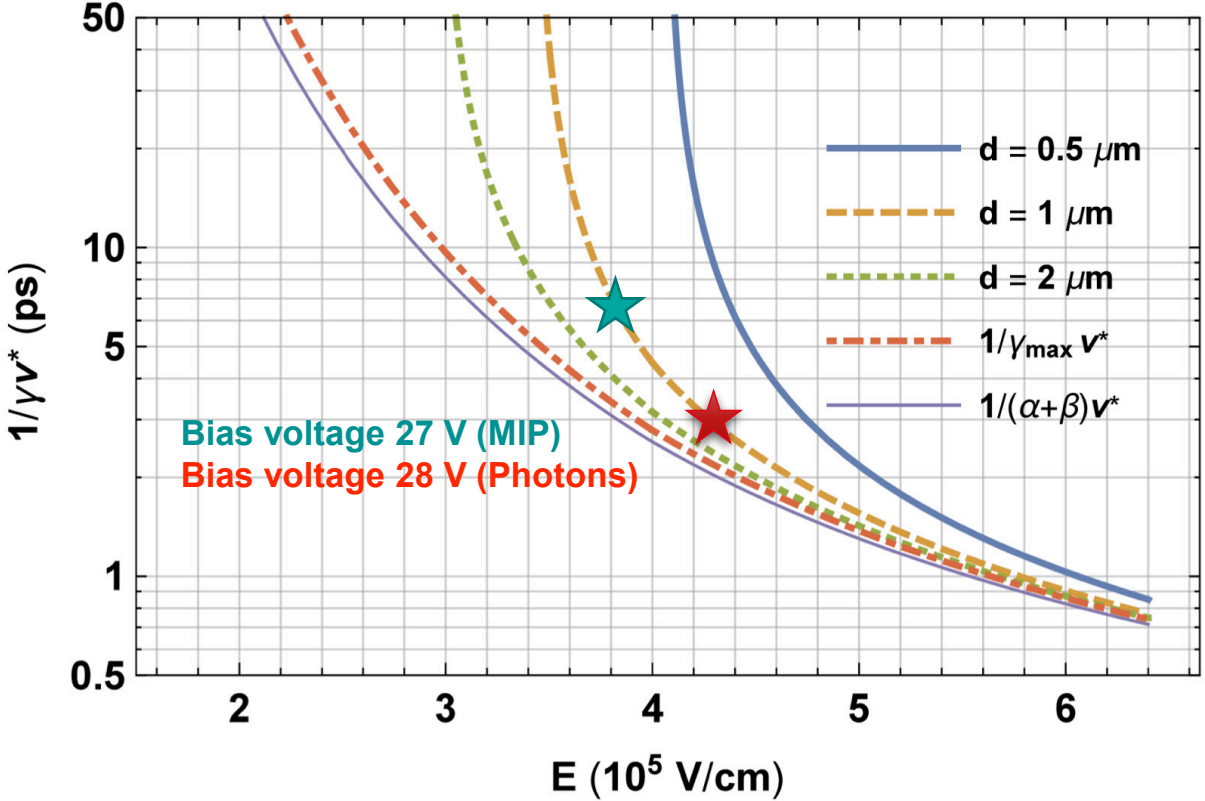
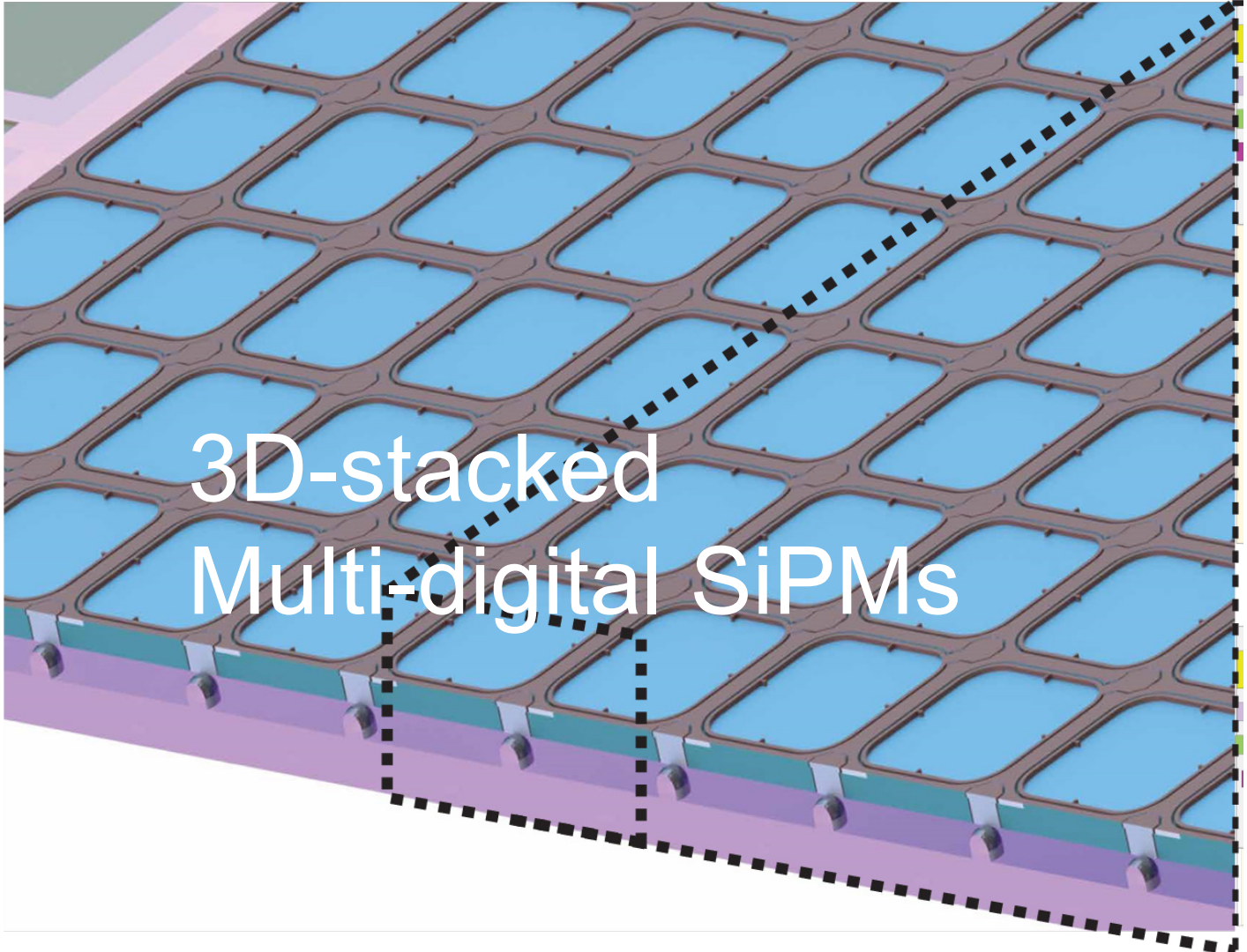
# Time resolution with SPADs

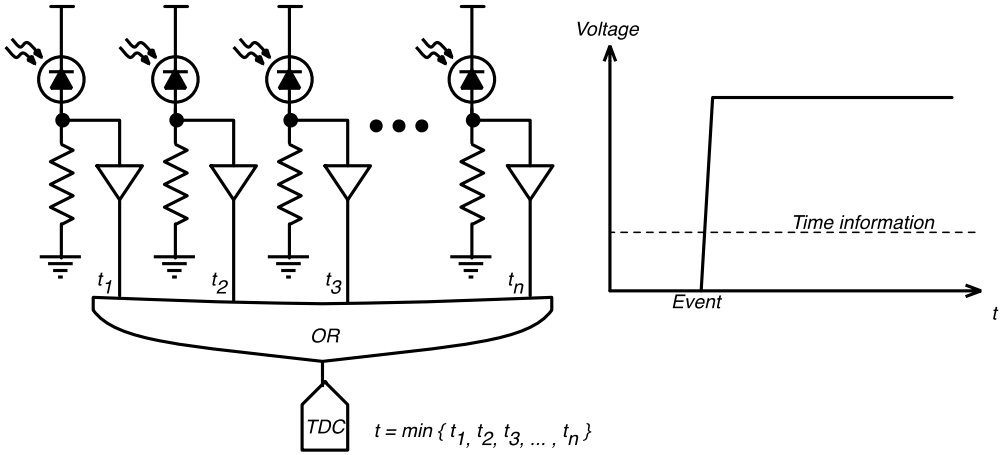



W. Riegler, P. Windischhofer, P. Time Resolution and Efficiency of SPADs and SiPMs for Photons and Charged Particles. *Nucl Instr Methods Phys Res Section A: Acc Spectrometers, Detectors Associated Equipment* (2021)

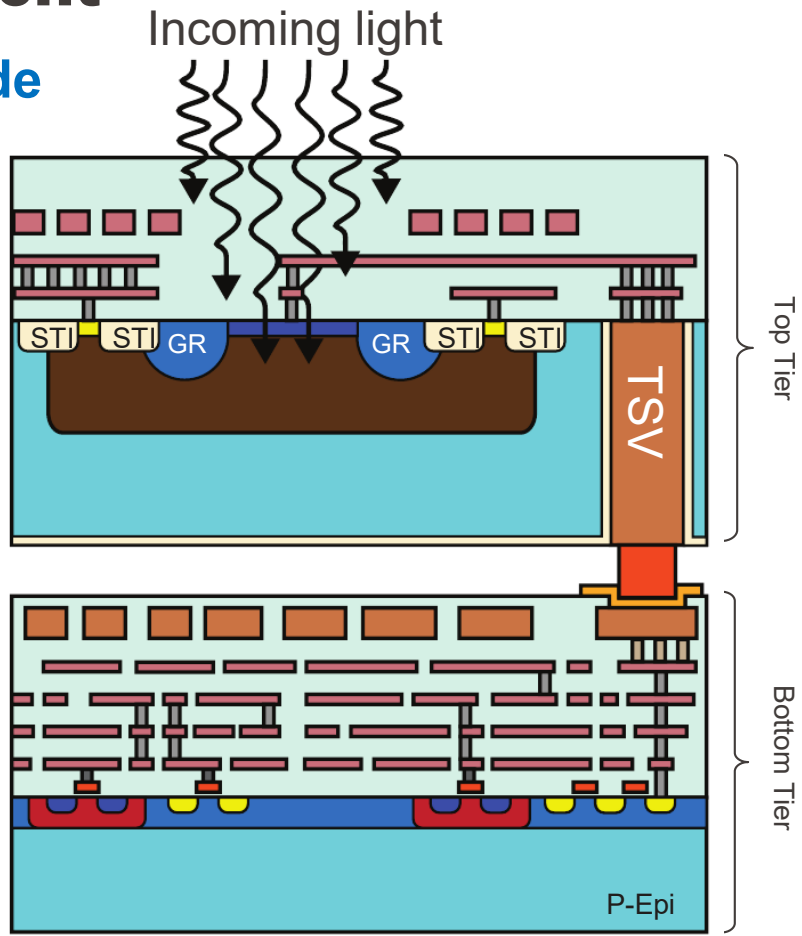

3D-stacked
Multi-digital SiPMs

# Detector Concept Development

## Digital SiPM



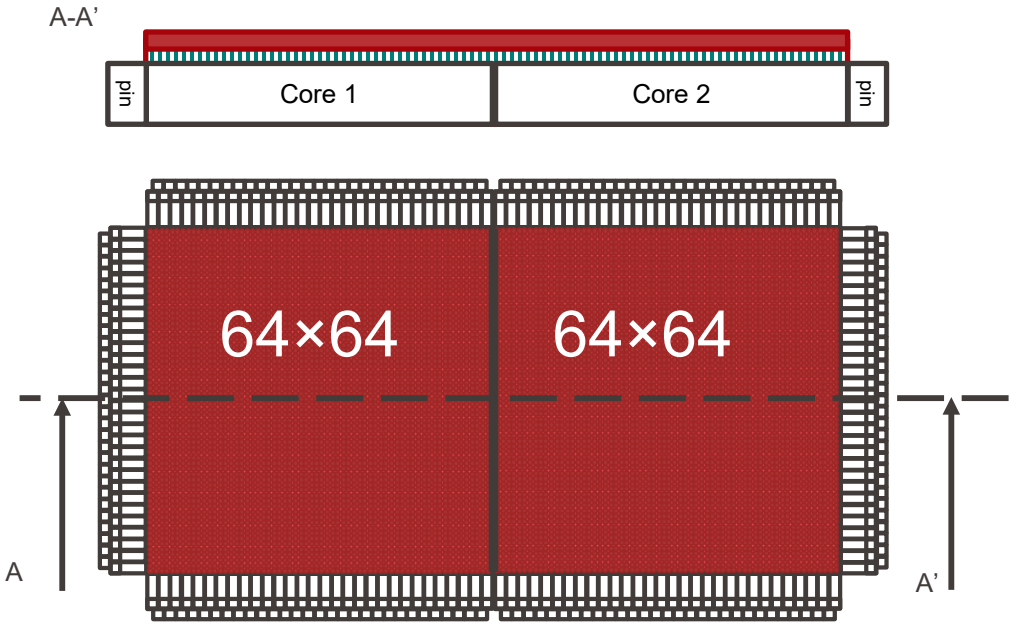

## 3D front-side illuminated



# Chip Architecture

## Multi digital SiPM:

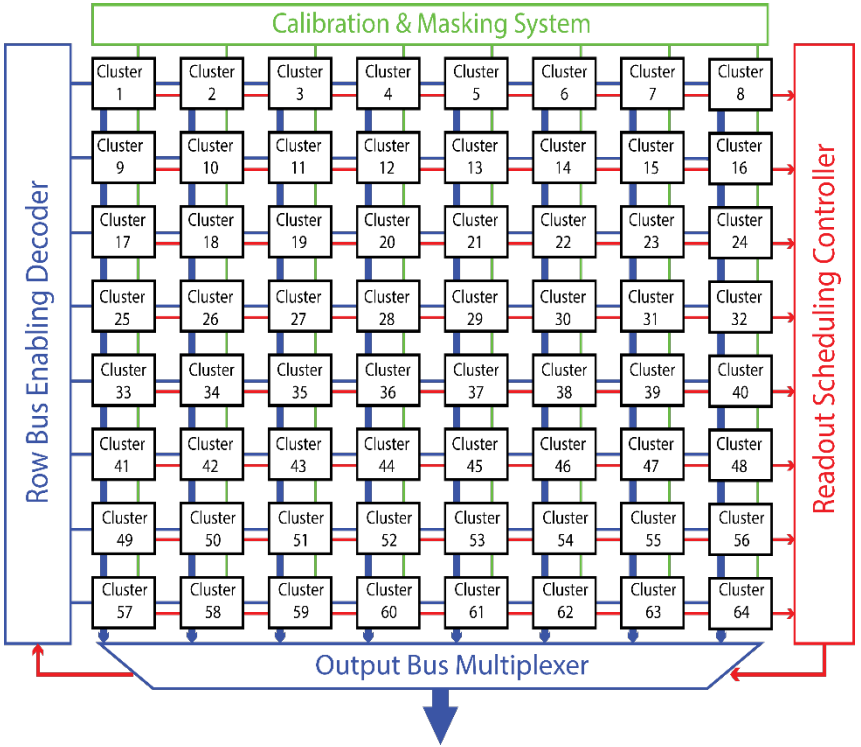
- 2 cores
- 64 clusters per core
- 64 SPADs per cluster
- Array of 8192 SPADs (2×4096)



# Chip Architecture

## Multi digital SiPM:

- 64 clusters per core
- 64 SPADs per cluster
- Random access readout architecture
- Single SPAD masking
- TDC calibration
- Fixed priority scheduling system



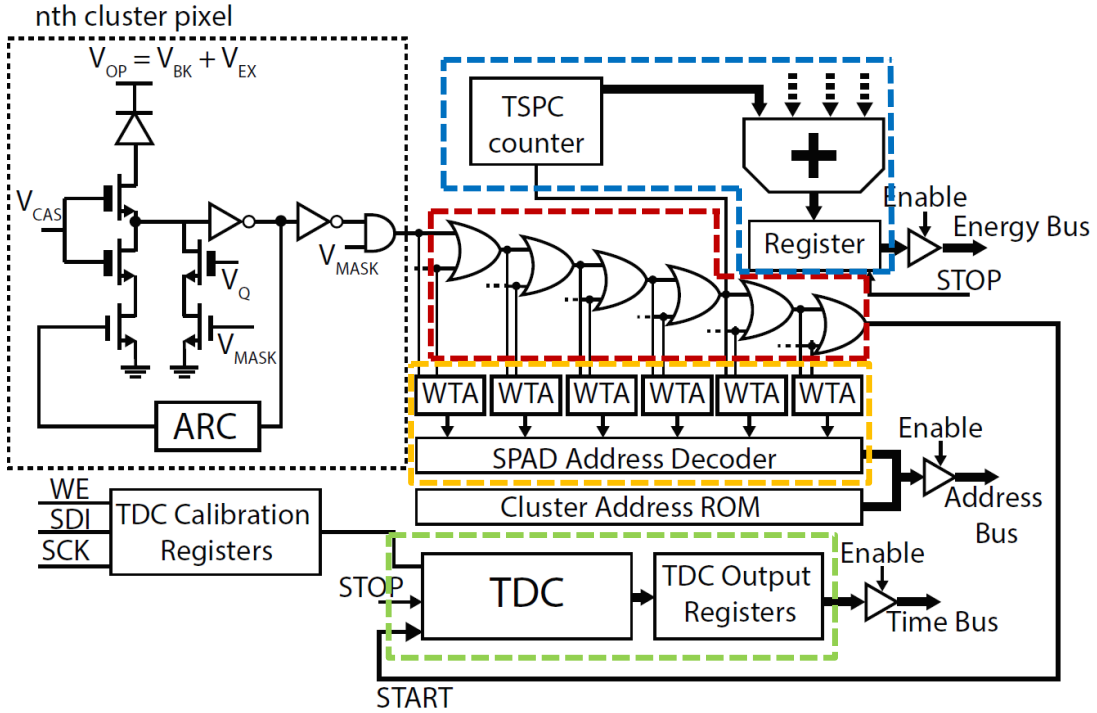
# Pixel & Cluster Architecture

**Pixel:**

- Cascode-based passive quenching to allow higher $V_{ex}$
- Active recharge circuit (ARC)
- Single SPAD logic masking

**Cluster:**

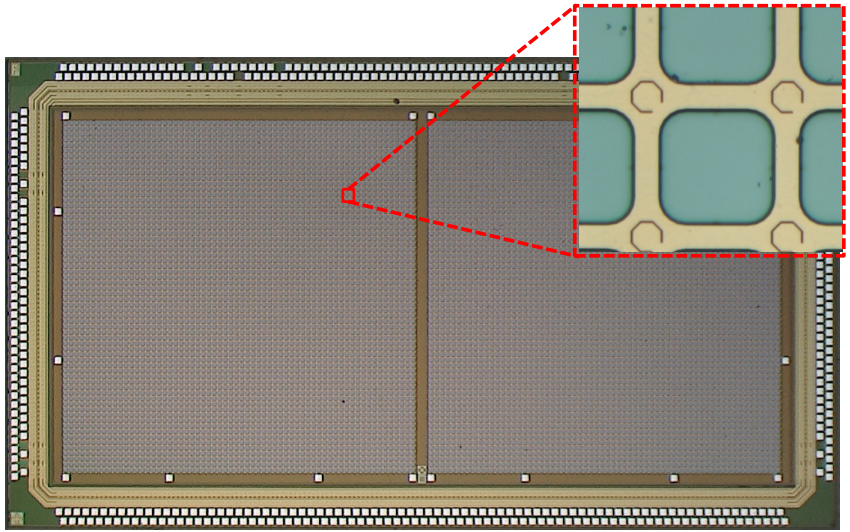
- OR-tree for data propagation
- Single shared TDC
- Photon counting capability
- Fired SPAD address calculation
- Shared bus access through high impedance buffers

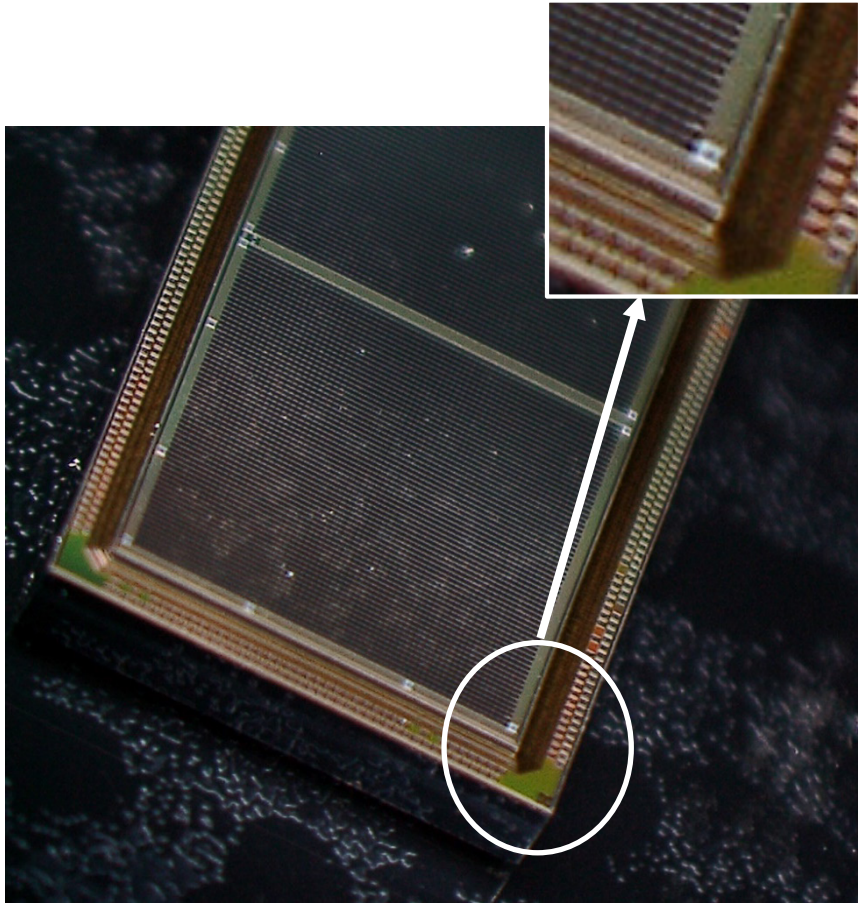


# Blueberry TOF Sensor

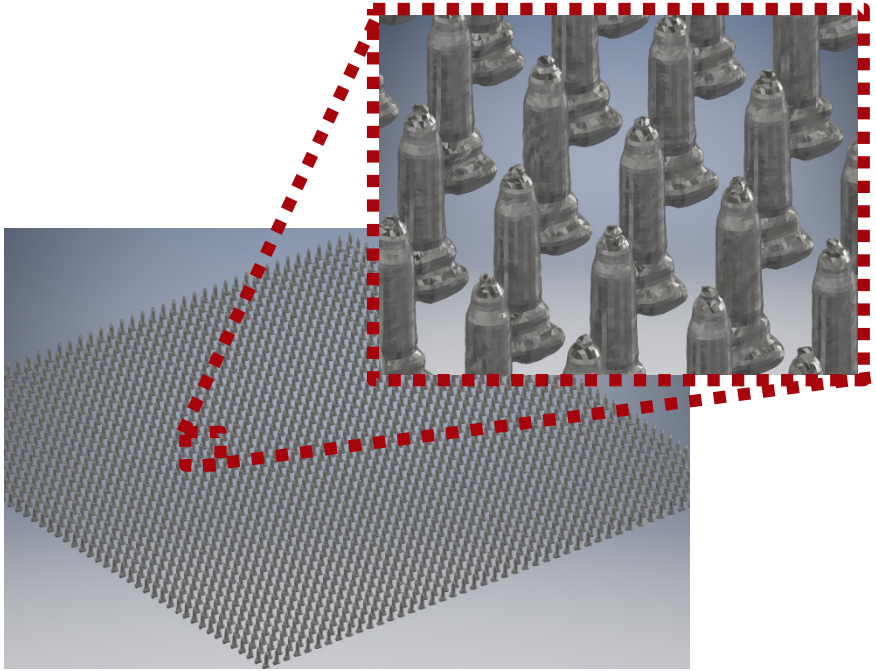
## 3D Stacked Chip:

- Array size: ~ 7.5×4.2mm$^2$
- Number of SPADs: 8192
- Technology node: 180nm CMOS

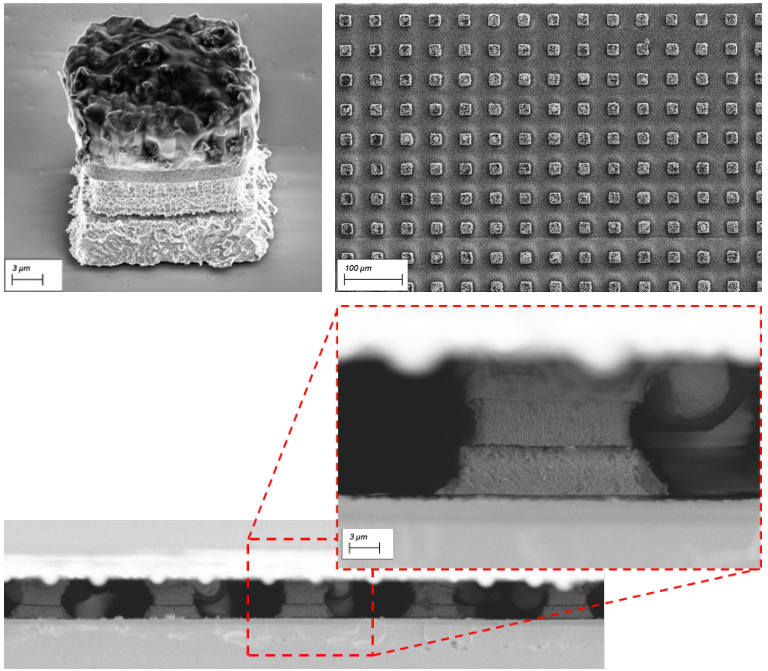




# Imaging Inspection

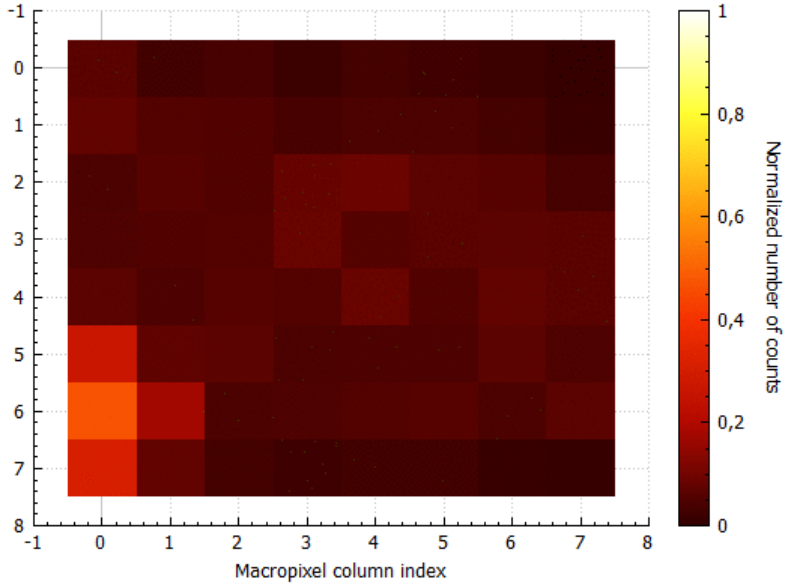


- X-Ray tomography
  - Voxel 1.42 µm
  - Not destructive inspection of TSV structure on large area

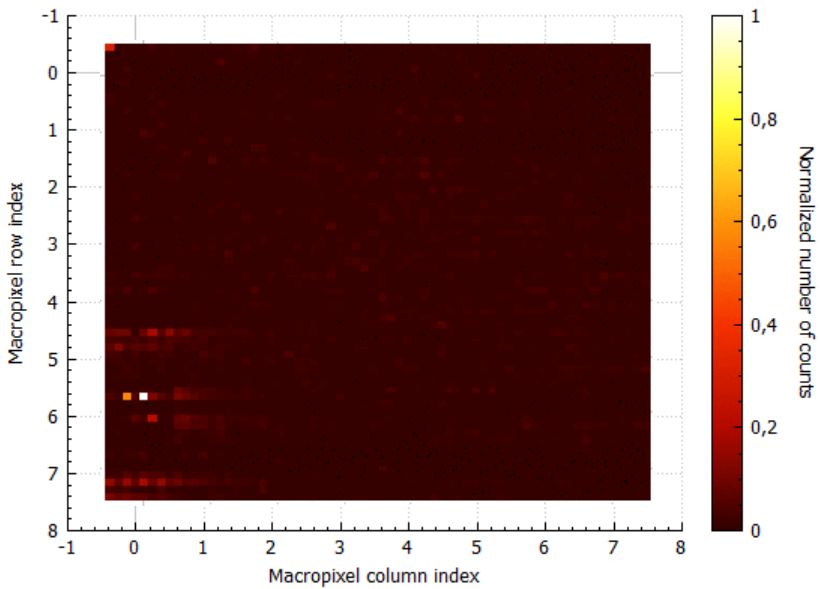



- SEM images of Microbump detail before (top) and after (bottom) 3D bonding

# DCR vs Integration Time




Intensity map built with the output of the photon counting system




Map of the pixel that fired first each frame during the acquisition

Process yield estimation ~90%

# Conclusions

# Summary & Conclusions

Optimized CMOS SPADs in 180 nm technology:

- 7.5 ps FWHM jitter demonstrated – noise reduction and front-end optimization are essential at the 10 ps level
- Tunable dead time down to 3 ns, PDP: 55%, AP: 0.12%, DCR: 0.23 cps/μm$^2$
- Can also detect minimum ionizing particles (MIPs) @ 6.4 ps sigma

Development ongoing in 55 nm BCD technology:

- 30 ps FWHM demonstrated, tunable dead time down to 1.5 ns
- PDP: 62%, AP: 0.13%, DCR: 2.6 cps/μm$^2$
- Amenable to 3D back-side illumination integration
- Potential for lower power consumption & reduced area

# Summary & Conclusions

Blueberry 3D-stacked FSI MD-SiPM:

- Experiments on dedicated test structures
  - TDC:
    - LSB = 15ps
    - DNL = [-1;2.57] LSB
    - INL = [-10;5.76] LSB (**uncalibrated**)
    - $P_{peak}$= ~1.4 mW/TDC
    - $P_{tot}$= ~130mW (expected)
- Preliminary results on the whole structure were shown
  - Demonstrated basic functionality of the chip
  - DCR over temperature

More comprehensive testing is ongoing

# Acknowledgments & Sources


- **Sub-10 ps FWHM SPADs**: Francesco Gramuglia, Ming-Lo Wu, Myung-Jae Lee, Claudio Bruschini, Edoardo Charbon
  - JSTQE(28) 2021, Frontiers in Physics(10) 2022
- **3D-stacked digital SiPM** (“Blueberry”): Francesco Gramuglia, Andrada Muntean, Carlo Alberto Fenoglio, Esteban Venialgo, Myung-Jae Lee, Scott Lindner, Makoto Motoyoshi, Andrei Ardelean, Claudio Bruschini, Edoardo Charbon
  - NSS-MIC 2021, IISW 2021
- **MIP detection**: Francesco Gramuglia, Emanuele Ripiccini, Carlo Alberto Fenoglio, Ming-Lo Wu, Lorenzo Paolozzi, Claudio Bruschini, Edoardo Charbon
  - Frontiers in Physics(10) 2022