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FPGA acceleration of the CMS DNN based LLP Jet Algorithm for the LHC High-Luminosity upgrade

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The CMS experiment at the Large Hadron Collider (LHC) at CERN adopts the LLP (Long-Lived Particle) Jet Algorithm, to search for new physics by tagging hadronic jets which stem from exotic long-lived particles. The LLP Jet Algorithm is a multiclass classifier based on a state-of-the-art Deep Neural Network (DNN). The jet tagging model's forward inference stage employs 12 convolutional layers and 5 dense layers to produce predictions from over 600 input parameters. Its DNN based architecture is highly computationally intensive, thus not meeting real-time latency constraints for data selection systems when implemented on a CPU; while a hardware accelerated FPGA implementation would meet real-time requirements. The motivation for exploring hardware acceleration for the LLP Jet Algorithm is further justified by the projected upscale in particle collisions and hence in data collection and processing requirements due to the planned High-Luminosity LHC upgrade. This work presents an FPGA acceleration of the LLP Jet Algorithm, exploring the use of kernelization to divide the algorithm into self-contained units, allowing simple orchestration of dataflow within the network and reuse of multiplication units enabling reduced hardware resource utilization, thus yielding performance enhancements by over an order of magnitude in the most computationally expensive sections of the network.

Primary author: OURIDA, Tarik

Co-authors: LUK, Wayne; Mr BHAT, Niranjan (Imperial College London); BARBONE, Marco (Imperial College (GB)); BAINBRIDGE, Robert John (Imperial College (GB)); TAPPER, Alex (Imperial College London)

Presenter: OURIDA, Tarik

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