PICv2 and BISv2 for HL-LHC Design and Status

Jan Uythoven on behalf of
A. Antoine, A. Apollonio, T. Cartier-Michaud, R. Johnson, O. Jullian Parra, M. Kalinowski, C. Martin, K. Osman, I. Romera Ramirez, R. Secondo

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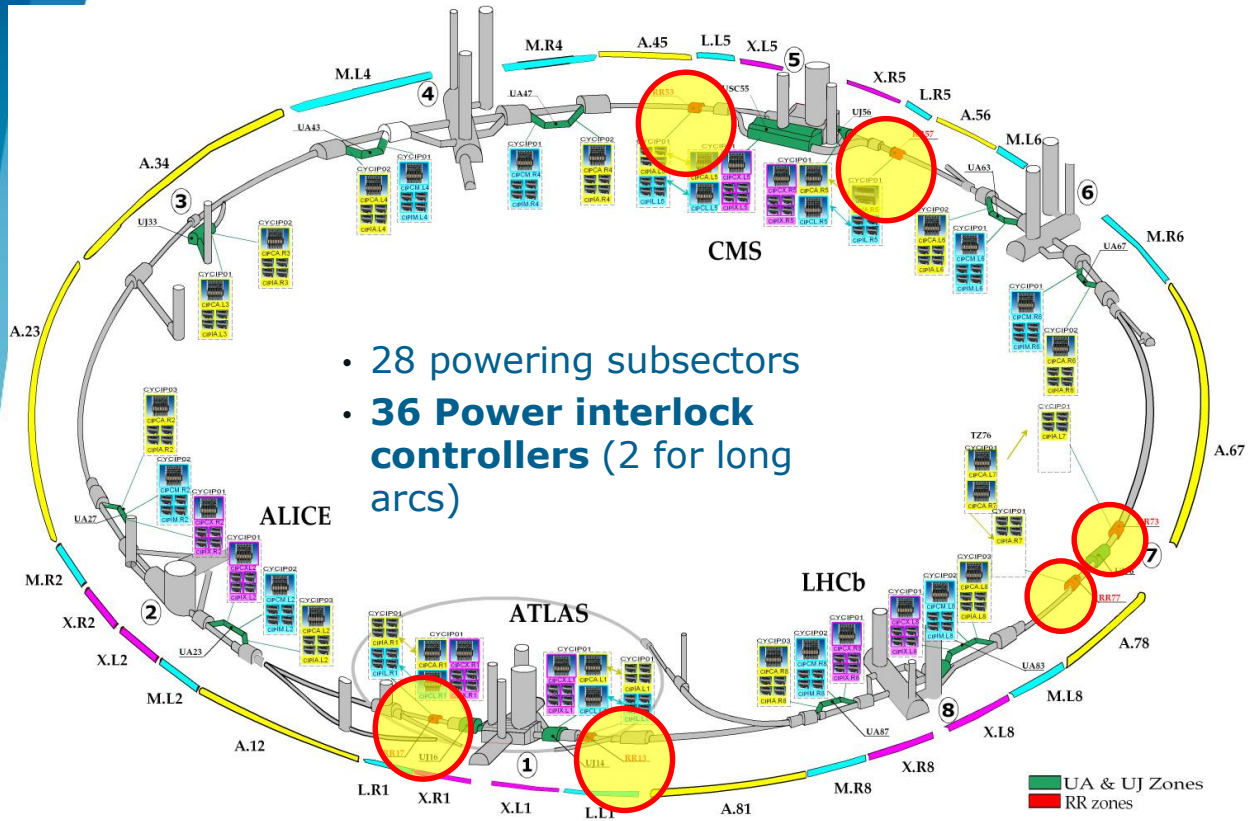
Introduction

- Power Interlock System v2 (PIC)
  - Protection of the superconducting magnet circuits
  - Affected by increased radiation levels due to HL
  - Status, plans
- Beam Interlock System v2 (BIS)
  - Backbone of the Machine Protection System of the LHC
  - Stop beam when needed
  - Status, plans

- Both projects are sponsored by the CONS program and by the HL-LHC project (WP7 Machine Protection & Availability)



- 28 powering subsectors
- **36 Power interlock controllers** (2 for long arcs)

- PIC is designed to:
  - Ensure the correct powering conditions for the superconducting magnet circuits
  - Request a beam dump via the Beam Interlock System in case of failure of a connected circuit
  - 10 out of 36 PICs are in a radioactive environment, namely the RRs at point 1, 5 and 7

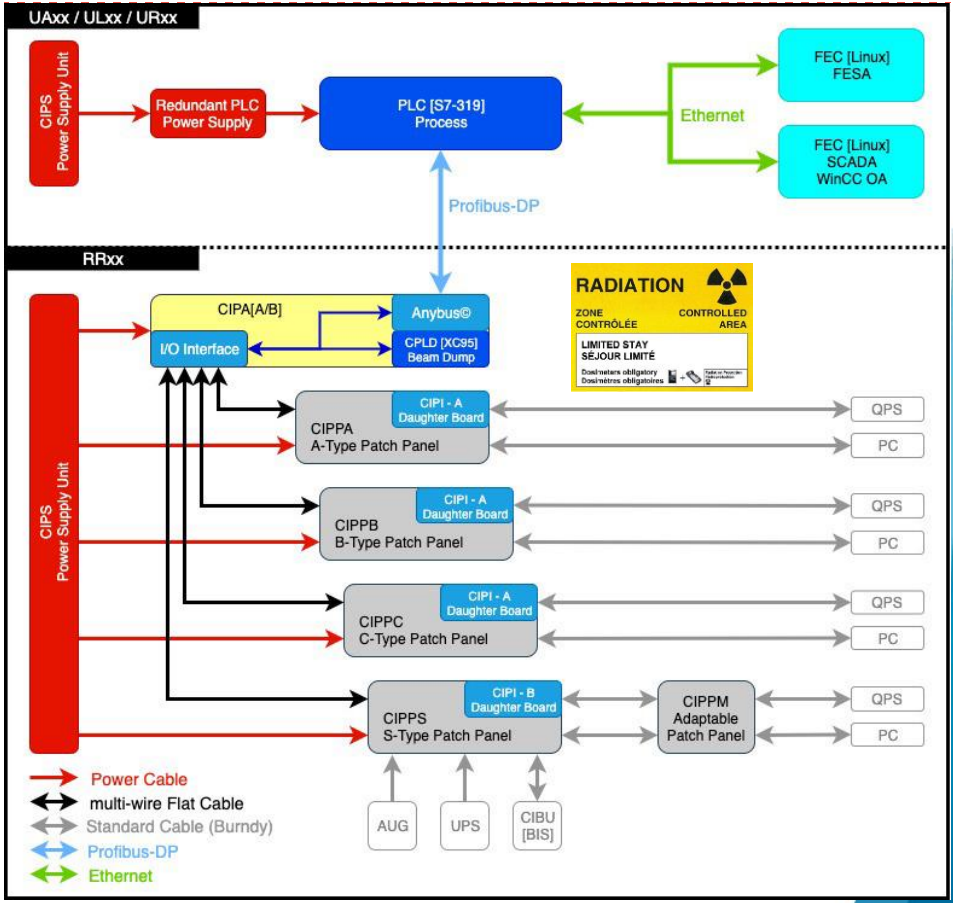
PICv1

14 years of operation

- System installed in 2006 and in operation since 2007.
- No interlocking failure recorded.
- Very high availability which is better than the prediction of <1 false dump / year
- Operational observations:
  - 5 radiation-induced dumps: issue solved after relocating the 9 affected PLCs installed in UJ14, UJ16 and UJ56.
  - Beam dump triggered by BLM after losing the Power Permit 60 A due to a communication error, highlighting a wrong SW interlock logic implementation in WinCC OA.
  - 2 spurious Quench loop instabilities (not due to the PIC)
  - General:
    - 1 broken Anybus board (CIPAA)
    - 1 broken Siemens power supply
    - Few broken AC/DC TRACO modules (redundant, no operational stops)

PICv1
Control Architecture

- CIPS (2x)
  - Provides all voltage sources with redundancy for all components except the PLC which has its own redundant power supply.
- PLC
  - Process execution.
- CIPA
  - Collects all the I/Os to expose them to the integrated CPLD and to the PLC via a PROFIBUS-DP fieldbus.
- CIPPx
  - Interface the PIC with all other systems (QPS, PC, AUG, UPS, BIS).
  - To note: CRYO signal is based on a PLC-PLC communication.
- CIPI
  - Provides the powering sources of some current loops, gathers the cables presence info and manages the connection to the BIC.
- FECs
  - GUI: SCADA (WinCC OA)
  - Dedicated FESA class for the GPM function.



PICv2 Motivations

- Extend the lifespan of the PIC into the HL-LHC era by addressing the obsolescence of critical components in the system design.
- Make the system compatible with the increased radiation levels in the RR areas
- Optimise the PIC based on the past experience, considering performance (reaction time) and diagnostics, and improve maintenance of the software

HL-LHC Specifications for PICv2

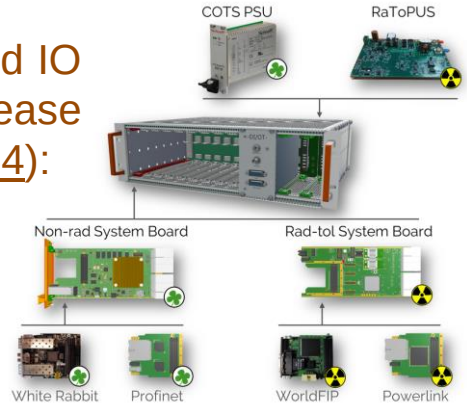
- Relocation of the 12 PLC CPUs of the sectors 1 and 5:
  - from UL14, UL16 to UR15,
  - from USC55, UL557 to UR55.
- New configuration of the PICs of the insertion regions and matching sections in point 1 & 5.
- Integration of new Trim Power Converters for the 11T Magnets.
  - No request for additional functionalities.

	Circuits for HiLumi	Magnet Type	Number of circuits per IP side	Total number of circuits	I_nominal (7 TeV) [kA]	I_ultimate [kA]	L per circuit at nominal current [mH]	R per circuit [mΩ]	Collaborations	References
Inner Triplet	Triplet Q1, Q2a, Q2b, Q3	MQXFA / MQFXB	1	4 (IR1/5)	16.23	17.5	255.4	0.15	US-HiLumi	EDMS no. 2114564
	Trim Q1	-	1	4 (IR1/5)	2	2	69	1.35	-	
	Trim Q1a	-	1	4 (IR1/5)	0.035	0.035	34.5	227.08	-	
	Trim Q3	-	1	4 (IR1/5)	2	2	69	1.2	-	
	Orbit correctors Q1/2 - Horizontal/Inner	MCBXFB	2	8 (IR1/5)	1.58	1.69	58.4	2.38	Ciemat	
	Orbit correctors Q1/2 - Vertical/Outer	MCBXFB	2	8 (IR1/5)	1.43	1.53	124.8	2.42	Ciemat	
	Orbit correctors Q3 - Horizontal/Inner	MCBXFA	1	4 (IR1/5)	1.584	1.702	107.1	1.99	Ciemat	
	Orbit correctors Q3 - Vertical/Outer	MCBXFA	1	4 (IR1/5)	1.402	1.502	232.3	1.98	Ciemat	
	Superferric, order 2	MQSXF	1	4 (IR1/5)	0.174	0.197	1530	18.12	INFN	
	Superferric, order 3, normal and skew	MCSXF / MCSSXF	2	8 (IR1/5)	0.099	0.112	213	54	INFN	
	Superferric, order 4, normal and skew	MCOXF / MCOSXF	2	8 (IR1/5)	0.102	0.115	220	54	INFN	
	Superferric, order 5, normal and skew	MCDXF / MCDSXF	2	8 (IR1/5)	0.092	0.106	120	54	INFN	
	Superferric, order 6	MCTXF	1	4 (IR1/5)	0.085	0.097	805	54	INFN	
	Superferric, order 6, skew	MCTSXF	1	4 (IR1/5)	0.084	0.094	177	54	INFN	
D1	Separation dipole D1	MBXF	1	4 (IR1/5)	12.11	13.231	24.84	0.41	KEK	
D2	Recombination dipole D2	MBRD	1	4 (IR1/5)	12.33	13.343	27.46	0.18	INFN	
	Orbit correctors D2	MCBRD	4	16 (IR1/5)	0.394	0.422	920	1.36	CERN	
Q4	Individually powered quad Q4 (4.5K)	MQY	Same Circuit Paramters for Q4, Q5, Q6 and Correctors in IR1/5 as in the LHC							ECR EDMS no. 2083813
	Orbit correctors Q4 (4.5K)	MCBY								
Q5	Individually powered quad Q5 (4.5K)	MQML								
	Orbit correctors Q5 (4.5K)	MCBC								
Q6	Individually powered quad Q6 (4.5K)	MQML								
	Orbit correctors Q6 (4.5K)	MCBC								
Q10	Individually powered quad Q10 (1.9K)	MQML	2	8 (IR1/5)	5.39	5.83	21	0.4	CERN	
	Orbit correctors Q10 (1.9K)	MCB	2	8 (IR1/5)	0.055	0.06	6020	45.8	CERN	
	Lattice Sextupole (1.9K)	MS	2	8 (IR1/5)	0.55	0.6	432	7.5	CERN	
Q5	Individually powered quad Q5 (4.5K)	MQY	2	4 (IR6)	3.61	3.9	74	0.4	CERN	
	Orbit correctors Q5 (4.5K)	MCBY	2	4 (IR6)	0.088	0.1	5270	34.4	CERN	

Hardware Design Options

1. New control architecture based on a PLC connected to a Distributed IO Tier crate (DI/OT) designed by BE-CEM-EDL to cope with the increase in radiation levels in the RR zones (L1) estimated at (EDMS 2302154):

Annual HL-LHC radiation levels	TID [Gy]	HEH [cm^{-2}]
RR13, RR17, RR53, RR57	25	$1.4.10^{10}$
RR73, RR77	4	2.10^{9}

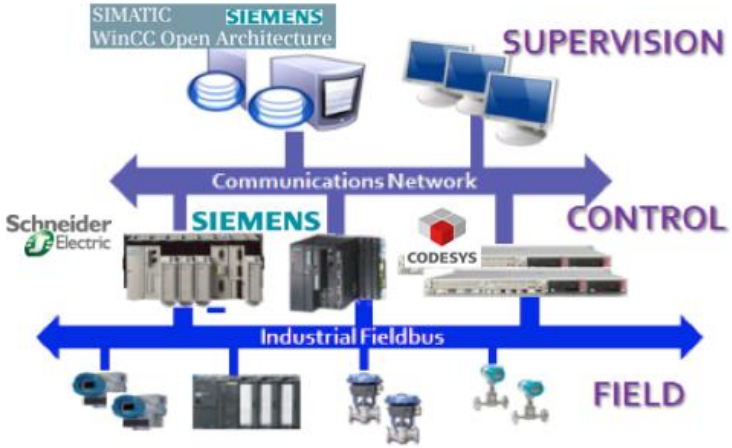


2. If a relocation of the PIC electronics out of the RR is feasible (cabling), a full industrial control architecture based on PLCs with high speed capability for the Beam dump function can be used instead

Decision shall be taken by the end of this year

PLC Software Design Options (in collaboration with BE-ICS)

1. Keep the current software by making it compatible with the CPUs currently available on the market.
2. Improve and optimize current software for ease of maintenance and future upgrades.
3. Design a new software based on UNICOS framework (**UN**ified **I**ndustrial **CO**ntrol **S**ystem) from BE-ICS.

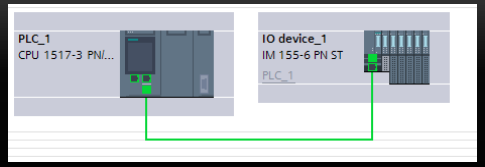


PICv2 Design Status

- A preliminary testbench based on the industrial control architecture solution has been produced
  - To check feasibility of a full industrial solution for the PICv2
  - To evaluate the response time of the system with different hardware and software configurations (not BIS connection, so far)
  - To ensure the PICv2 will perform at least as well as PICv1
  - Exclusively made of industrial components (Power supplies and optocouplers) and the new Siemens S7-1500 series

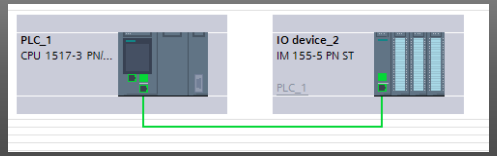
PICv2 Test Bench Setups

S7-1517 CPU with ET200SP Remote I/O over PROFINET



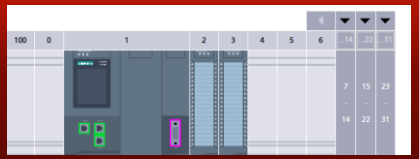
HW Setup 1

S7-1517 CPU with ET200MP Remote I/O over PROFINET



HW Setup 2

S7-1517 CPU with DI and DQ modules



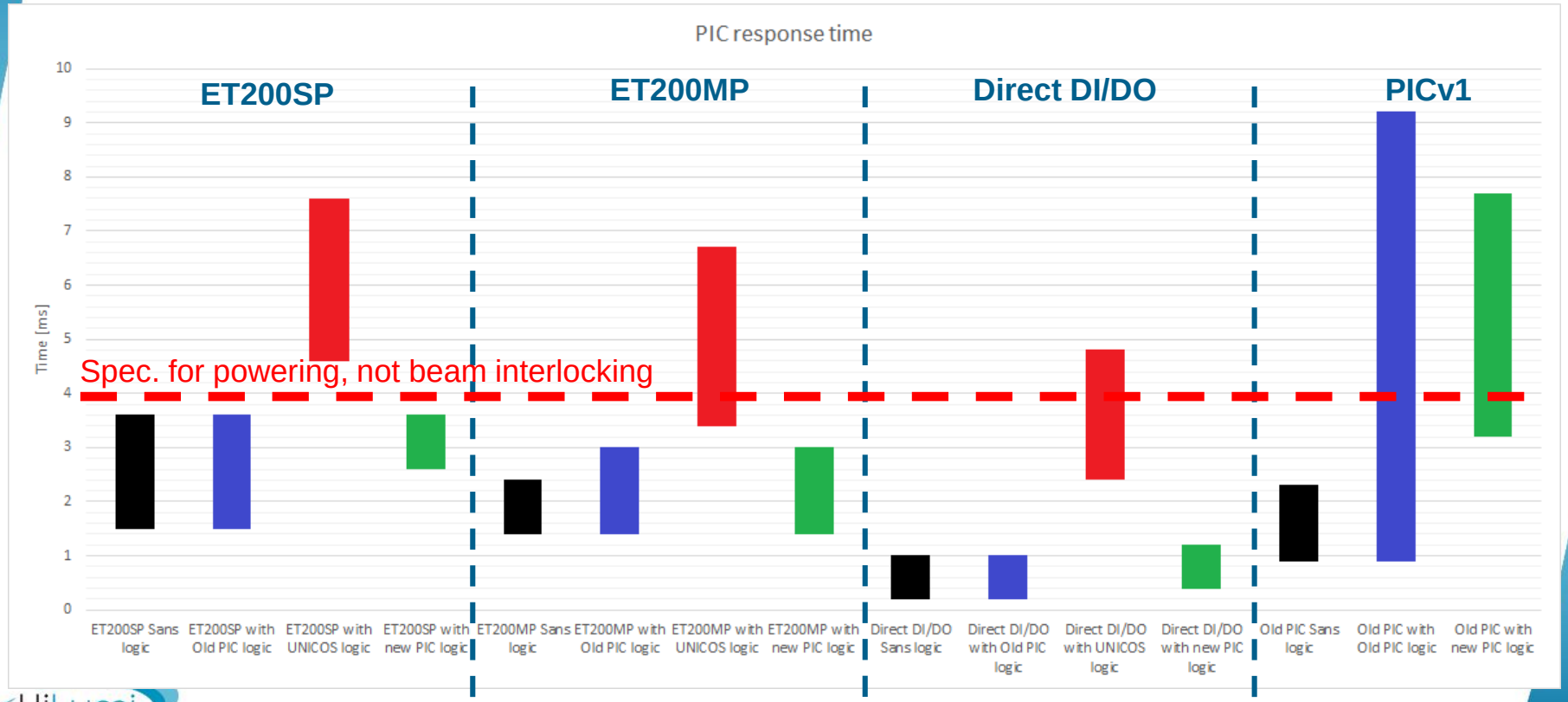
HW Setup 3

Tested Software	Comment
No logic	Only one Organisation Block (OB1) with 1 line of code setting Digital Output according to Digital Input position.
PICv1 logic	Current PIC logic migrated into the TIA portal and S7-1500 CPU.
Optimized PIC logic	Tailor made PLC code for the PICv2.
UNICOS logic*	UNICOS framework program generated using the UAB tool – “empty shell” without fully working logic.

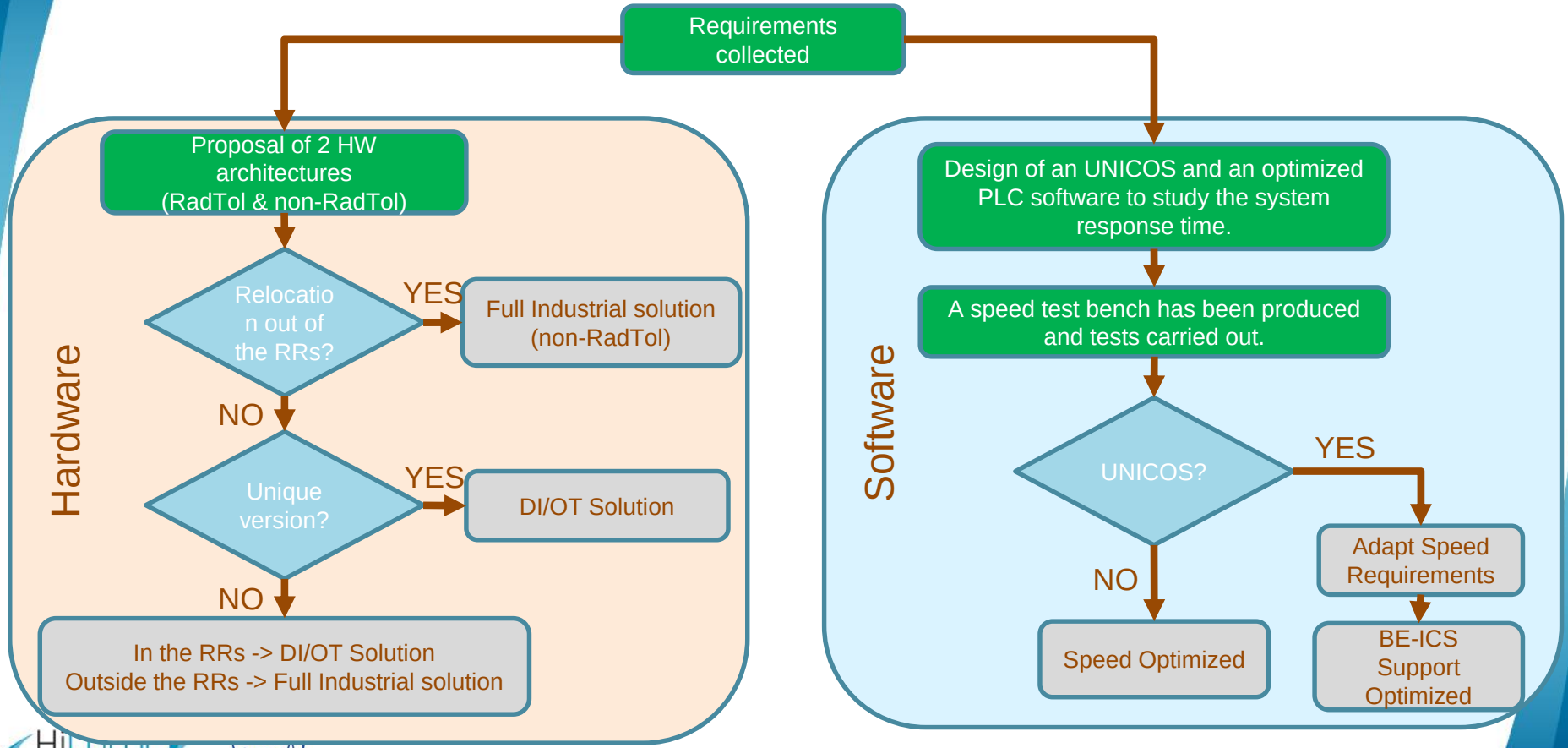
* UNICOS software is not easily translatable to S7-300 CPU and was not tested on PICv1 test bench.

PICv2 Industrial Solution – Response Time Results

No logic PICv1 logic UNICOS logic Optimized PIC logic



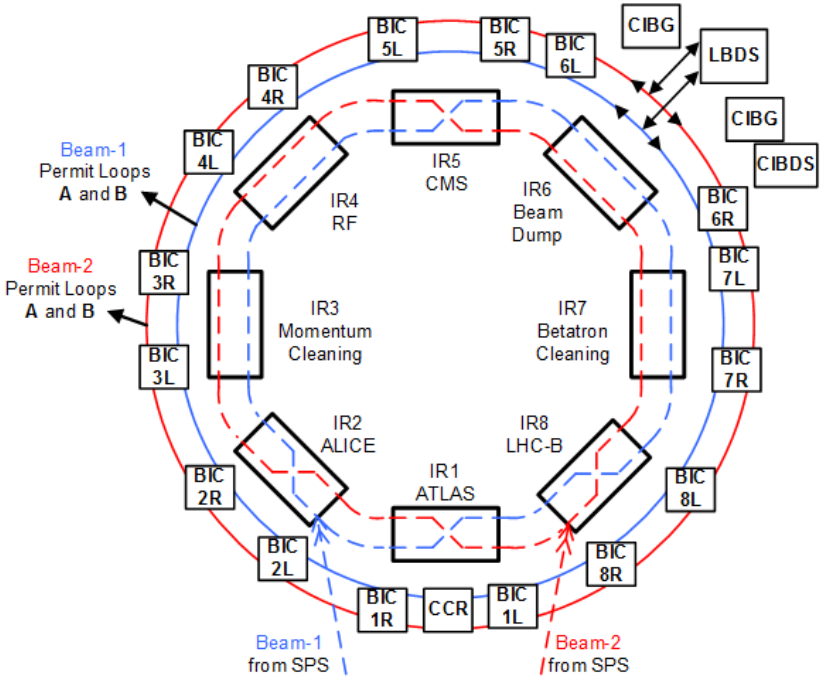
Project Strategy



Project Strategy – Timeline

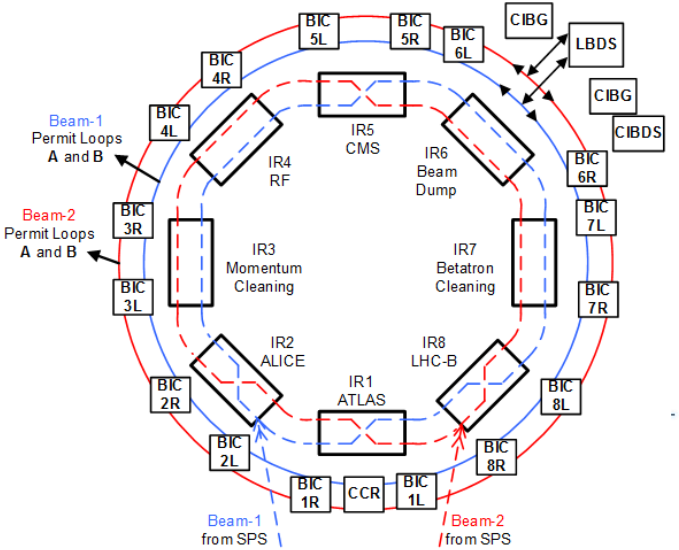
- End of 2021
  - Decision on the relocation of the PIC components outside the RRs
- 2022:
  - Delivery and commissioning of a first version of the PICv2 to the STRING
- 2023-2024
  - First operational experience in STRING and validation of the final version(S)
  - Production of all parts
- 2025-2026
  - Installation and commissioning in the LHC

The Beam Interlock System



The BIS in a nutshell

- The Beam Interlock System is a **highly reliable, fast and available** system which is designed to protect high energy accelerators from potential beam damage
  - Deployed in the **LHC, SPS, SPS to LHC Transfer Lines, SPS INJ, PSB EXT and LINAC4** (i.e. 50 BICs, 500 CIBU/Fs, tens of km of copper cables and optical fibres)
    - **Excellent dependability** since first deployment in 2006 and majority of faults transparent for operations (e.g. redundant PSU, CPU faults…)
      - **No blind failure during operation,** 1 detected during HWC due to non-conform user system



Layout of the LHC Beam Interlock System

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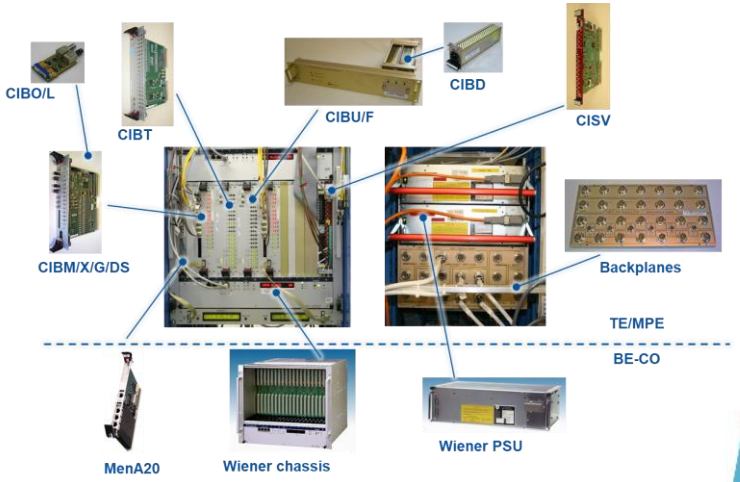


Typical LHC BIS crate and electronics boards

Motivation to upgrade the BIS

- **Obsolescence**
  - **Aging** – limited spares, new installations and support up to the end of HL-LHC
  - **Discontinuity** of electrical components – Xilinx CPLD XC9500 and FPGA Spartan 3
  - **Full occupancy** of FPGA logic cells – no space for implementing new features
  - **Wiener crate** – Crate with redundant power supplies not supported anymore

- **New requirements**
  - **Increased number of user inputs –** increase number of user inputs
  - **Enhanced linking of Beam Permit loops** – to mitigate risks due to beam-beam effects with fast failures
  - **Enhanced standardisation** - common interface between BIS and actuators (TE-ABT, BE-RF TE-EPC)
  - **FALSE frequency** to Beam Permit – request to mitigate glitches in DC operation

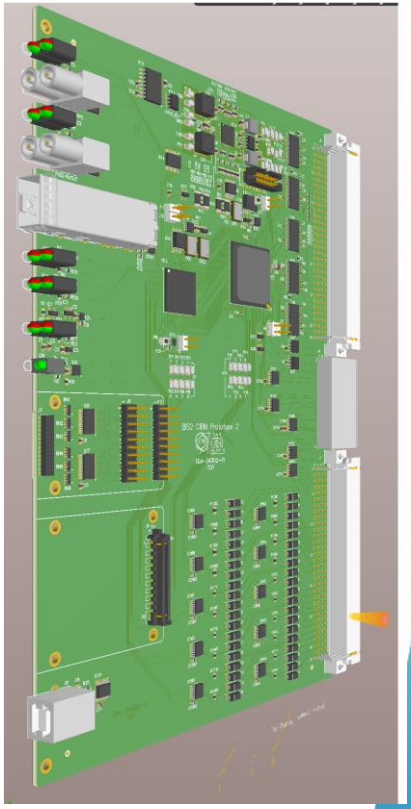
- **Maintainability**
  - **Optical transmission** - enhance power budget and provide remote diagnostics
  - **Timing interface** – improve interface to the timing system and the way timing events are used

Present BIS vs BIS 2v0

Requirement of Feature/Peripheral	BIS 1	BIS 2	Comments
Enhanced Optical Communications - SFPs	CIBO allows Beam Permit via Fibre only	SFPs allow BP via Fibre and Diagnostics	Tx/Rx Power, Tx Bias Current available, Temperature, Voltage, **BIS 1.23*
Bus backplane communication	VME64	VME64x	BE-CEM support for HL-LHC lifetime Other platforms considered: PXI, DIOT, uTCA
CIBU interfaces	Current loops and differential signals	Current loops and differential signals	Kept compatibility with CIBU v1
More User Permits per BIC	14	20	More User Permits = Greater Flexibility
Redesign CIBF – BIC Interface	CIBFu => CIBFc => BIC	CIBF => BIC	Fibres can interface directly to the BIS crate via CIBF Interface card (CIBFi)
Greater Redundancy in CIBM Path (per A and B channels)	1	2	Splitting A and B will reduce chance of blind failures
Better interface of Timing Events/Signals	CTRV => CIBU => BIC	CTRV => BIC	Timing signals no longer need to be interlocked via a CIBU
Reduction in Form Factor of BIC boards	3 slots per CIBM, 3 slots per CIBM Tester (12 total)	1 slot per CIBM, 2 slots for single LED Display (6 total)	All operation will be handled by the CIBM, New crates have 4 slots fewer
Better On-board Analytical Peripherals	Basic Analysis, UART	Temperature, RTC, UART, EEPROM, ADC	No longer require specific instance testers
Maintain or Improve Reliability	No Blind-Dumps, MTBF > 1'000 years	No Blind-Dumps, MTBF > 1'000 years	

New Hardware: CIBM 2v0 – Manager board

- 2nd prototype (EDA-04302-V2-0): design finished in November 2020 and **prototypes currently being tested in the lab**
- PCB layout and production done **in collaboration with BE-CEM-EPR**
- Includes both **monitor and critical** paths (Xilinx Spartan 7 and Artix 7, interface to VME64x bus, SFP for Beam Permit Loops, UART for diagnostics, RTC, Temperature sensors…)
- **Internal review** organised with MPE-EP before launching prototypes
- Prototype is fully functional and very similar to the **final CIBM in production**
- This design is used as a **template for other boards**



CIBM 2v0 - Electronics hardware

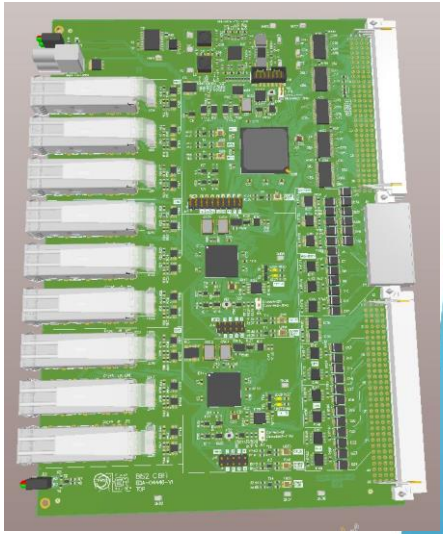
New Hardware:
CIBU 2v0 – User permit interface

- 2nd prototype (EDA-04288-V2-0): design finished in June 2021, **2 prototype boards**
  - Production and assembly **launched in collaboration with BE-CEM-EPR**
- **Improvements on availability**: enhanced remote diagnostic capabilities (i.e. monitoring of User Permit currents and voltage/current of redundant power supplies)
- **Improvements on maintainability and cost**: EEPROM with unique ID (pre-programmed from factory), real-time counters for reliability calculations and Igloo2 FPGA for diagnostics
  - Hardware **compatible with v1** (same hardware interfaces but different firmware)
- **Radiation tolerant design** – Electronic parts already tested at PSI and soon at CHARM

CIBU 2v0 – Electronics hardware

New Hardware:
CIBFi 2v0 – Optical interface on controller side

- 1st prototype (EDA-0446-V1-0): design **finished in September 2021**
  - PCB layout, production and assembly **done in collaboration with BE-CEM-EPR**
- Designed to receive User Permit **signals over long distances (up to 10 km)**
  - **Works in conjunction with a CIBFu** (optical interface on user side)
  - Allows to connect up to 3 CIBFu and **receive inputs from 3 users**
  - Equipped with **redundant XILINX Artix 7 FPGAs for critical path**
- Uses commercial **SFP (Small Form-factor Pluggable) transceivers**
- Possible use in SMP 2v0 for **direct transmission of SMP flags to BIS controllers**



CIBFi 2v0 – Electronics hardware

Radiation test campaigns at PSI

- CIBUs will be installed in radiation areas (e.g. RR alcoves) => **radiation-tolerant design required**

	Annual ($360\ fb^{-1}$) HL-LHC radiation levels			
	TID [Gy]	HEH [cm^{-2}]	Th. neut. [cm^{-2}]	1MeVn-eq [cm^{-2}]
RR13-17-53-57 Lo	15	$1 \cdot 10^{10}\ cm^{-2}$	$9 \cdot 10^{10}\ cm^{-2}$	$7 \cdot 10^{10}\ cm^{-2}$
RR13-17-53-57 L1	25	$1.4 \cdot 10^{10}\ cm^{-2}$	$1.2 \cdot 10^{11}\ cm^{-2}$	$7 \cdot 10^{10}\ cm^{-2}$

Source: HL-LHC Radiation level specification document, EDMS 2302154

- All CIBU electronic parts have been irradiated with a **200 MeV proton beam to a dose up to 500 Gy and fluences up to ~8.5x10^{11} p/cm^2** in order to meet HL-LHC R2E specifications (in collaboration with BE-CEM)

- **Radiation-sensitive components were identified,** and corrective actions will be implemented in the final hardware version:
  - **INA240A1D**: current sense amplifier (experienced latch-ups above 25 Gy)
  - **TPS3808G33DBVT** and **TPS3808G12DBVT:** Programmable delay supervisory circuit (died after 85 Gv, variable reset duration after 60 Gy)

CIBU Testbed and CIBM validation

- Hardware testbed **designed to verify and program the CIBU** production
  - **NI PXI platform** used as a General Tester Crate (GTC)
  - A **Test Controller Card (TCC)** has been designed to interface the GTC and the CIBU
    - Test sequences implemented in **LabWindows-CVI**

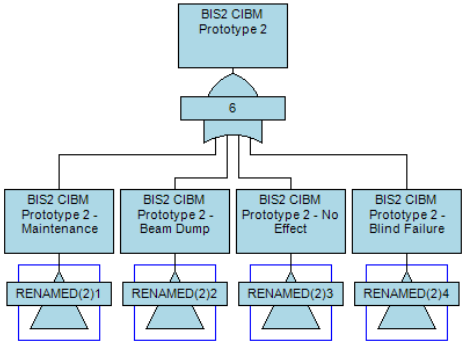
CIBU 2v0 Testbed platform

CIBM 2v0 validation in the lab

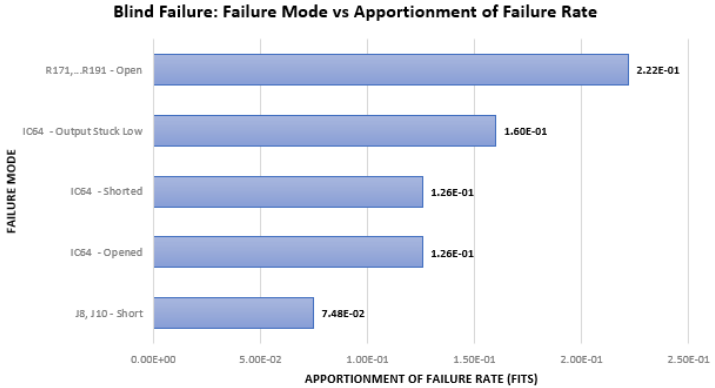
- **CIBM prototypes under validation** in the BIS lab
- **Firmware is completed** and functionality is working
- Communication between **CIBU and CIBM is validated**
- Beam Permit Loops and **critical functionality is validated**

Reliability calculations

- The **reliability targets** set for BIS v2 are unchanged:
  - False dump: 1 / Year
  - Blind failure: 1 / 1000 Years
- **Isograph** is used to calculate the failure rate of electronic cards based on component level analysis
- **FMECA** analysis carried out for assessment of failure effects of the individual components: false dump or blind failures
- **Completed for the CIBM and CIBU, ongoing for CIBFi**
- **Fault-tree analysis** to estimate the the overall probability of occurrence of the system failures & assess new architecture
- **AvailSim4** for advanced simulation of system monitoring and repair strategies, allowing for direct comparison of failure probabilities with reliability targets
- **Work ongoing**



CIBM Fault tree analysis generated by Isograph



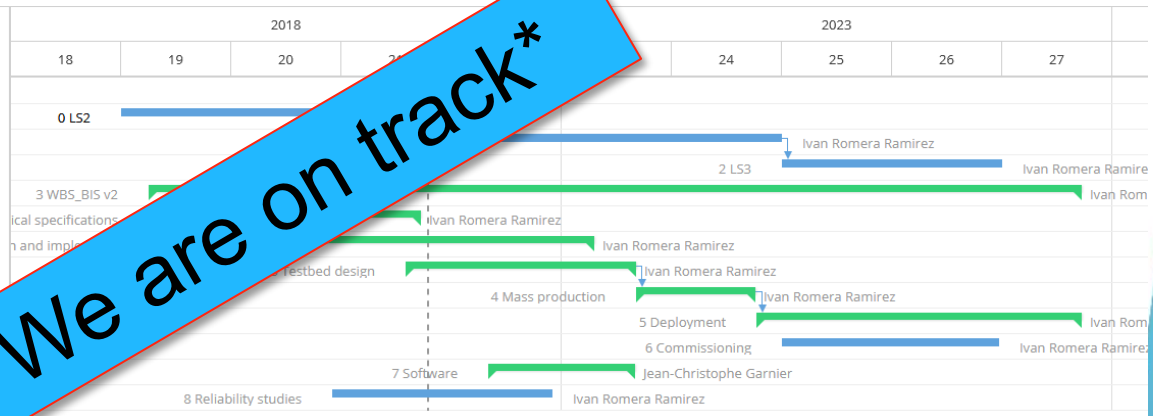
Plot Showing Failure Mode vs Apportionment of Failure Rate for Blind Failure of the CIBM

BIS 2v0 Planning

Gantt: BIS v2 Roadmap

Add ▾ | Delete ▾ | Edit ▾ | View ▾ | Data ▾ | Jump to Gantt Bar | Today | « » | Bird's-eye view ▾

Project/Version/Issue	Assignee	Units	Start date	Finish date
BIS v2.0 project				
0 LS2	Ivan Ro...	0%	1/Jan/19	7/May/21
1 RUN 3	Ivan Ro...	0%	10/May/21	31/Dec/24
2 LS3	Ivan Ro...	0%	1/Jan/25	1/Jan/27
3 WBS_BIS v2	Ivan Ro...	0%	1/Apr/19	20/Sep/27
1 Analysis and technical specificati...	Ivan Ro...	0%	1/Apr/19	21/Sep/21
2 Hardware design and implemen...	Ivan Ro...	0%	1/Jul/19	19/Apr/23
3 Testbed design	Ivan Ro...	0%	2/Aug/21	5/Sep/23
4 Mass production	Ivan Ro...	0%	6/Sep/23	4/Oct/24
5 Deployment	Ivan Ro...	0%	7/Oct/24	20/Sep/
6 Commissioning	Ivan Ro...	30%	1/Jan/25	2
7 Software	Jean-Chr...	0%	2/May/22	1/Se
8 Reliability studies	Ivan Ro...	0%	1/Dec/20	1/Dec/



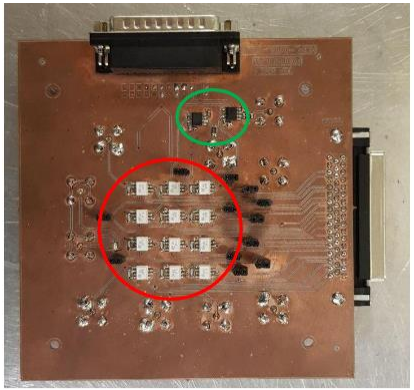
We are on track*

Conclusions

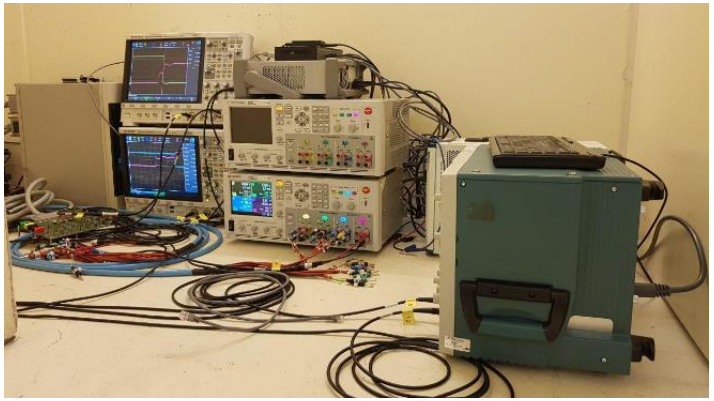
- PICv2
  - No new PIC functionalities in the scope of the HL-LHC
  - Decide on possible relocation of the PIC out of radiation zones by the end of this year
    - On track for first implementation in the String
    - The first speed test results of an industrial version of the PIC are very promising
- BISv2
  - Good progress with the design of prototypes (CIBM, CIBU and CIBFi) and testbeds
    - Related system Safe Machine Parameters V2 is also on track
  - Radiation test campaigns at PSI allowed to validate the electronic parts of the CIBU
    Additional tests are foreseen at CHARM in Q1-2022
    - Reliability analysis of the complete BIS system ongoing
  - On track for deploying BIS 2v0 in the SPS, LHC and its Transfer Lines in LS3
    - *Long delivery delays of electronics components are a worry

Spare Slides

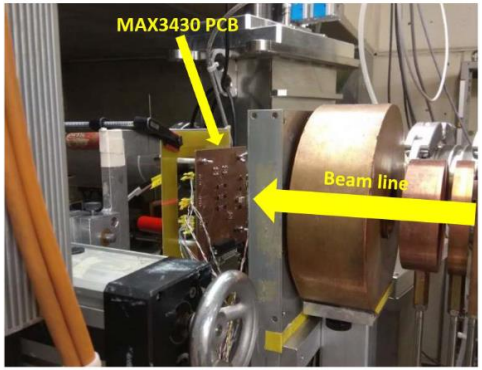
Radiation test campaigns at PSI



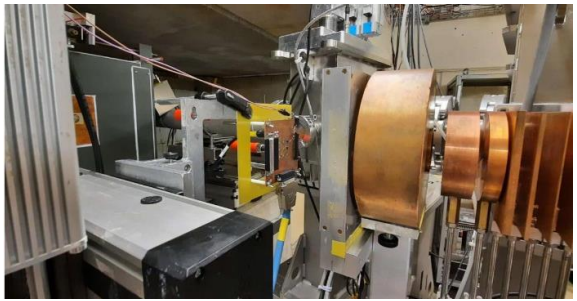
FOD060LR2 PCB tested at PSI



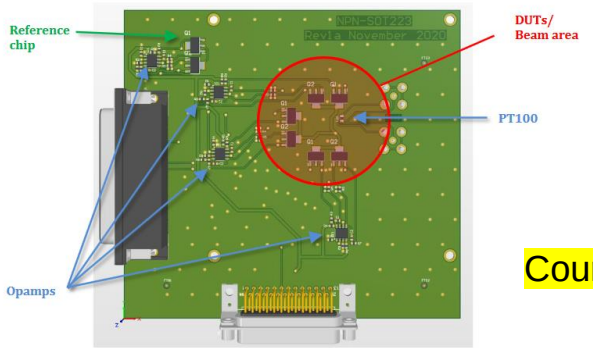
Instrumentation setup to collect data during tests



MAX3040ESA tested at PSI



AD7291 ADC test board on the beam line



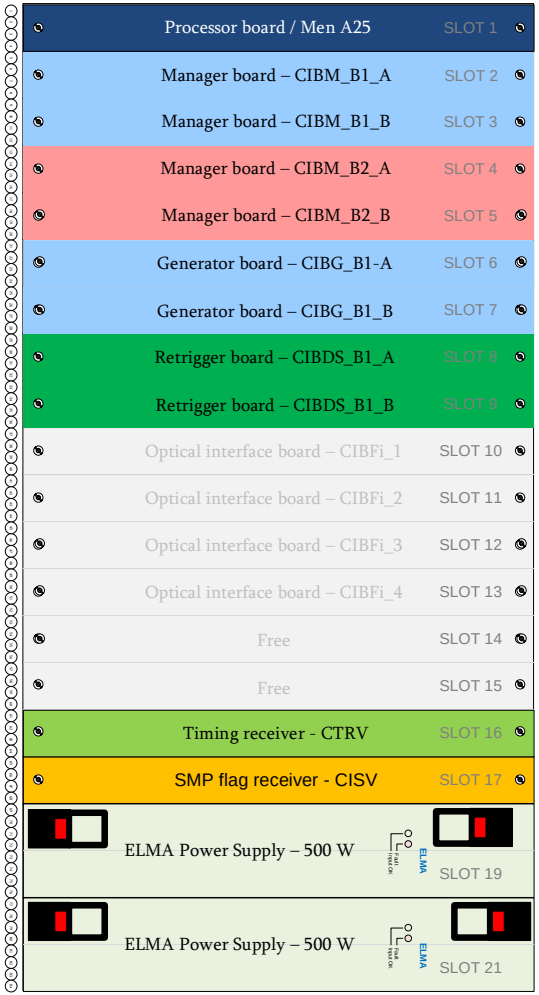
PZT2222AT1G DUT board

Courtesy BE-CEM

BIS vs BIS 2v0 layout

BIS 1v0 crate in UA63

BIS 2v0 crate in UA63



CIBM channel A and B fully split: full redundancy and integration of test and monitor board

Split CIBM channel A and B to maintain redundancy

Direct fibre interface

Direct CTRV conn.

Wiener 64X power supplies at the back, large

ELMA VME 64X power suppy at the front