Radiation Tolerant BLM ASIC Development

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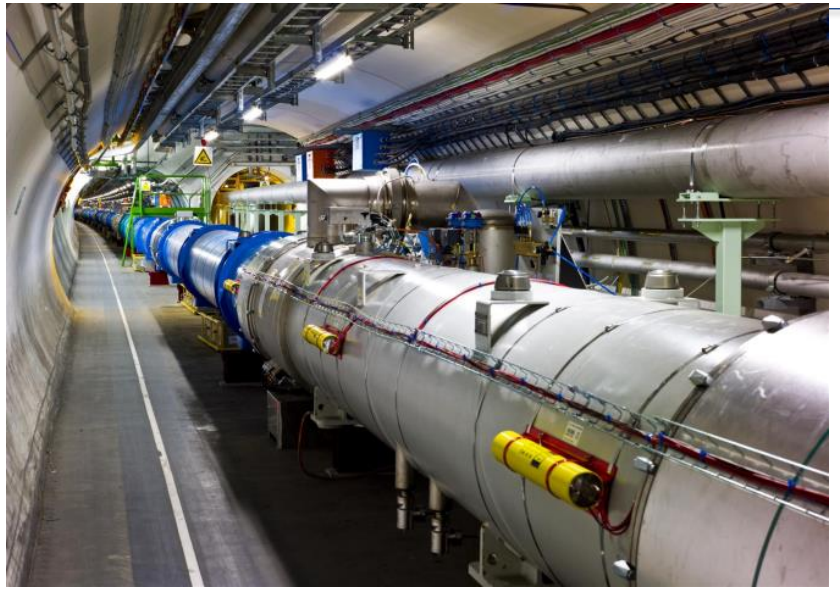
https://indico.cern.ch/event/1079026/

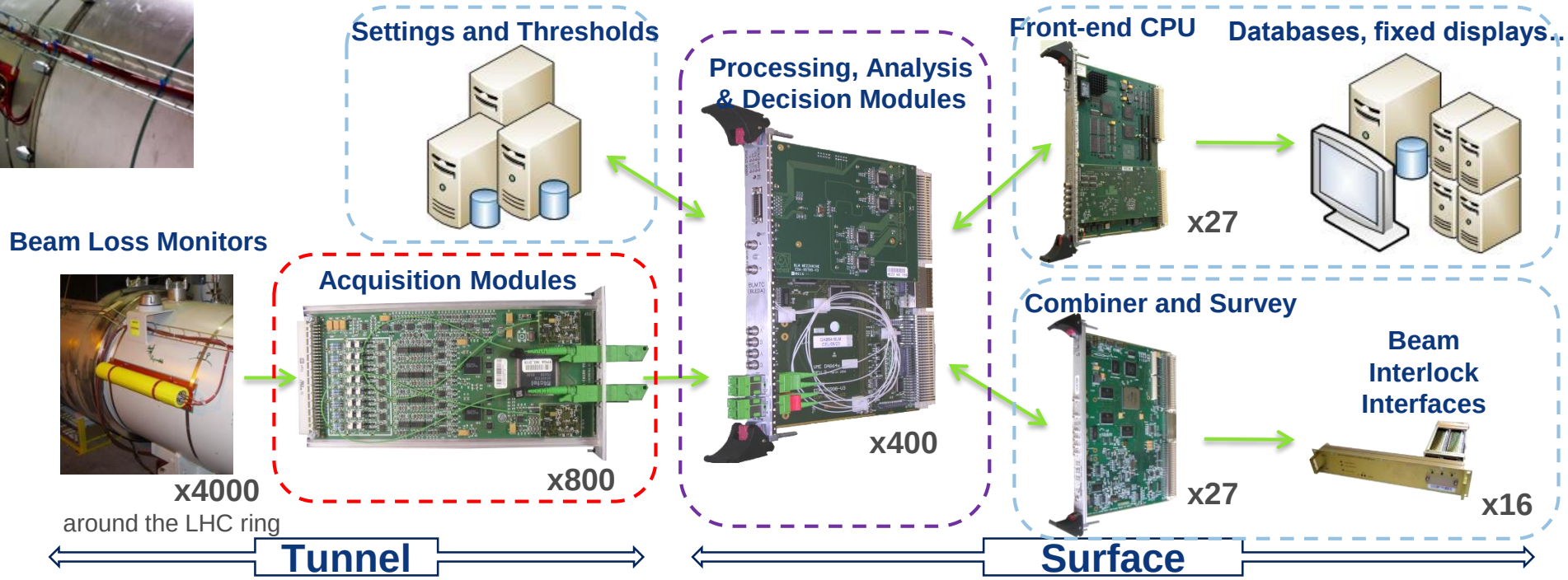
Overview

- System Overview
- Development
  - Status and Progress
  - Roadmap and future plans
- Future Deployment
- Conclusions

LHC BLM System Overview



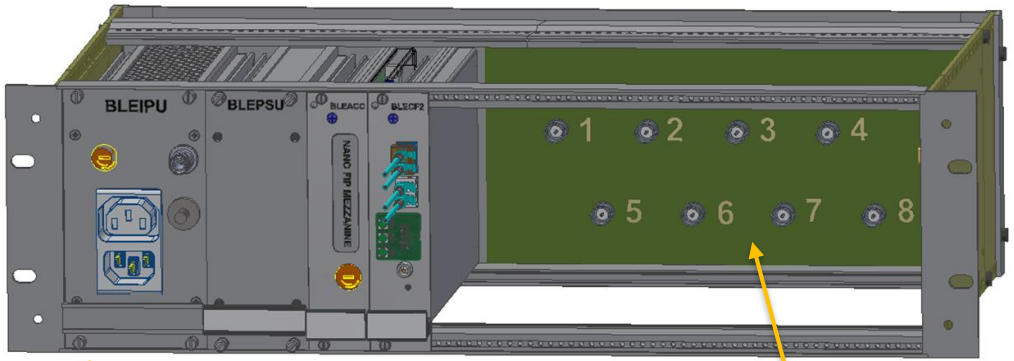
- Highly critical system for the protection of LHC
- Deployed all around the 27 km of the tunnel
- Speed, Reliability, Fail-safety is required
- Large amount of measurement data are published continuously



Development Progress

Acquisition Crate

- First functional version of the crate ready including power supplies and backplane
- Working on the remote control card (via nanoFIP) and acquisition modules



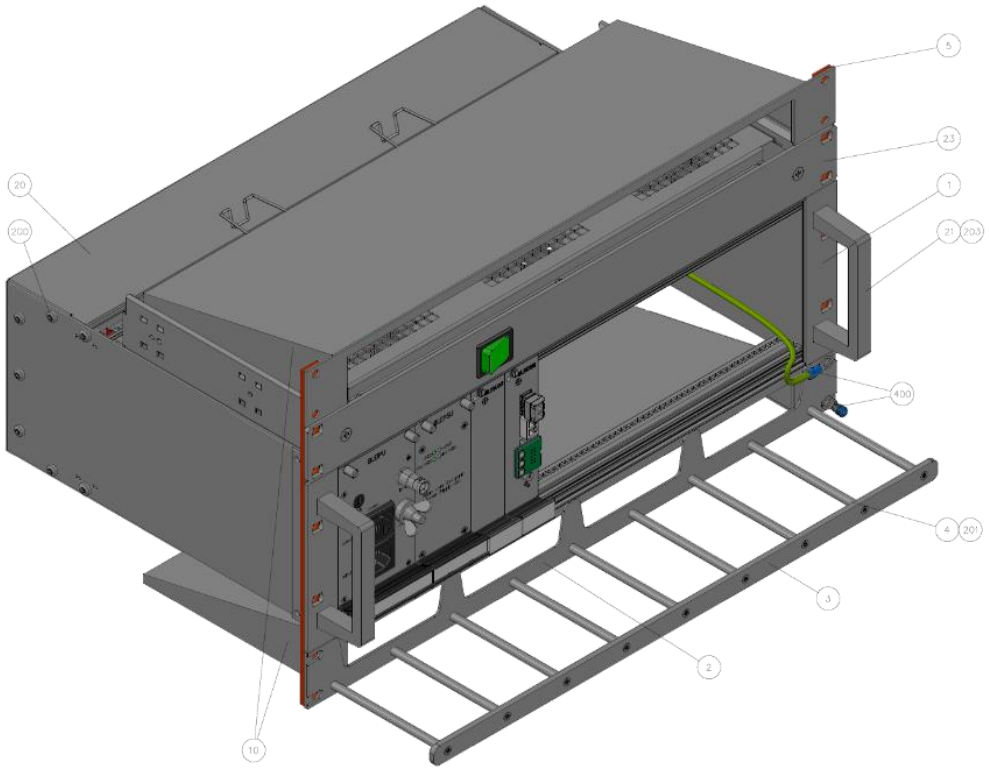
Input Power unit

Power Supply unit

Control unit

Acquisition unit

Channel connections



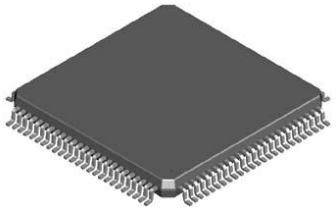
All connections from the front side
Electronics enclosed in a mini-rack

Acquisition Electronics

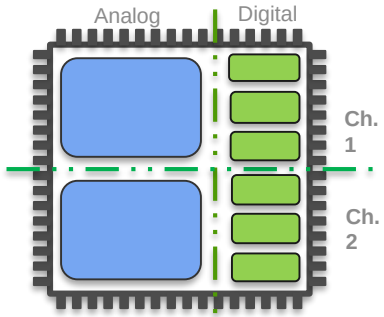
- Two distinct designs on-going
  - BLECF v2 (upgrade) with distinct components (COTS & ASIC)
  - BLMASIC encapsulating both analogue & digital functions in rad-hard ASIC
- Commonalities pursuit
  - Size and form factor, i.e. one cartridge of 6HP
  - Backplane connection and power scheme
  - Communication (lpGBT & SM-VTRx)
  - Acquisition frequency and range
- Additional advantages (TBC)
  - Interchangeable where necessary
  - Main processing blocks common

BLMASIC: Current-to-Frequency or Δ/Σ Converter

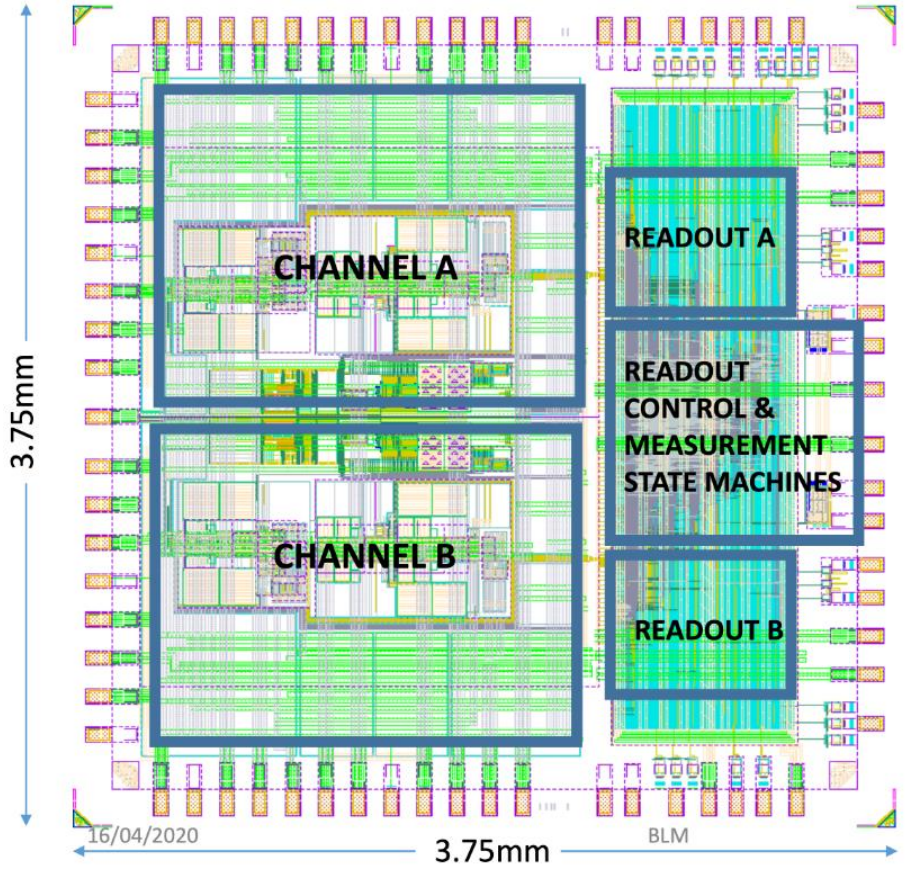
- Two analogue-to-digital converter circuits have been under investigation:
  - Current-to-Frequency (CFC) & Δ/Σ converter
  - v2 achieved linearity and low current measurement specs
  - Preliminary results from x-ray irradiation exceeds specs
- Next version (v3) is focusing on the CFC type only
  - Address ESD, power and minor digital part issues
- Some delays due to COVID-19
  - Dependency on foundries and packaging of the devices
- Fabrication completed for 200 units
  - Waiting return of the devices from the packaging company



Standard 64-pin Quad Flat Package (10x10 mm)

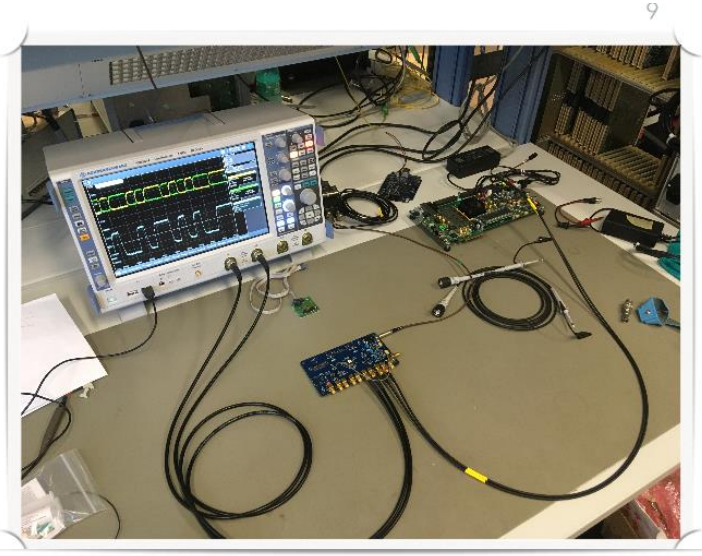


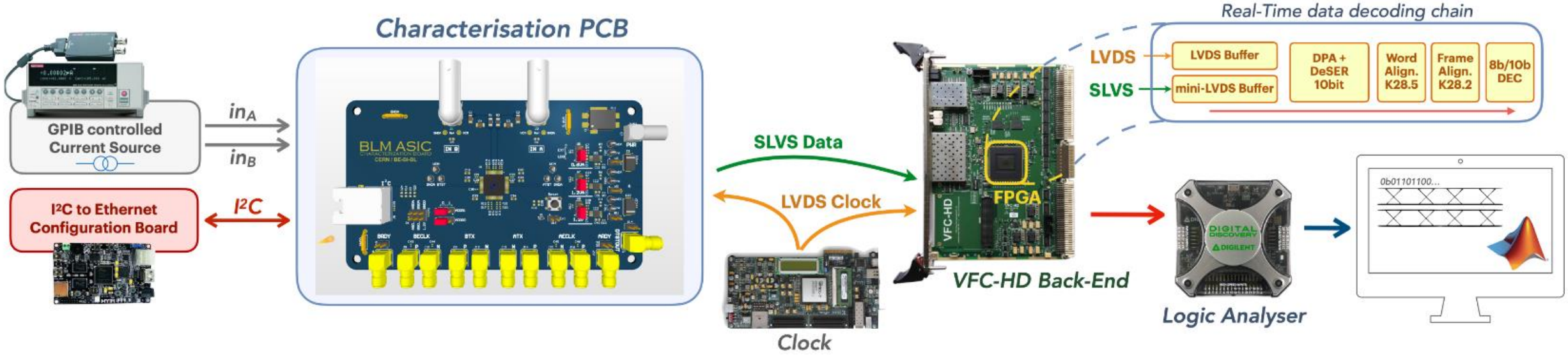
Two analog readout channels per chip (4x4 mm)



BLMASIC: Testbench

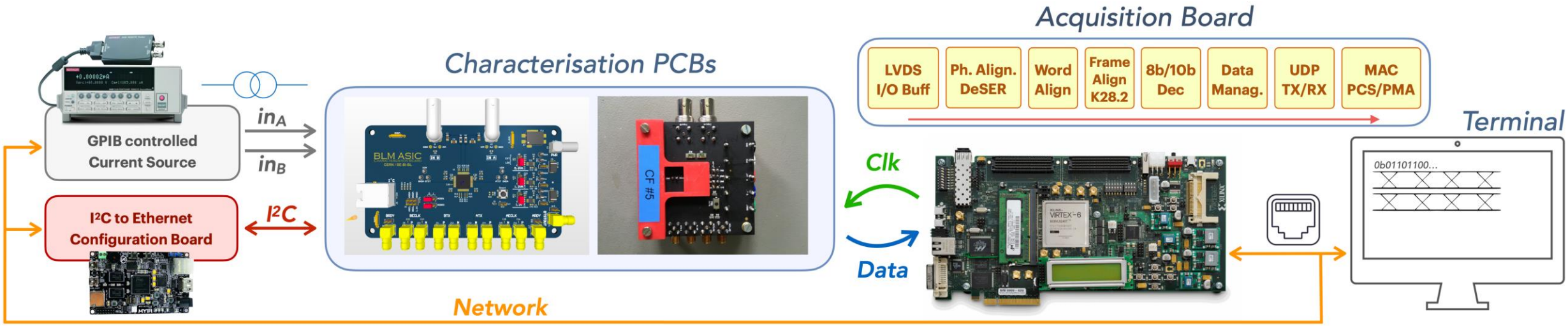
- ASIC performance validation
- Comparison between ASIC architectures
- Reliability tests
- Radiation hardness validation





BLMASIC: Validation

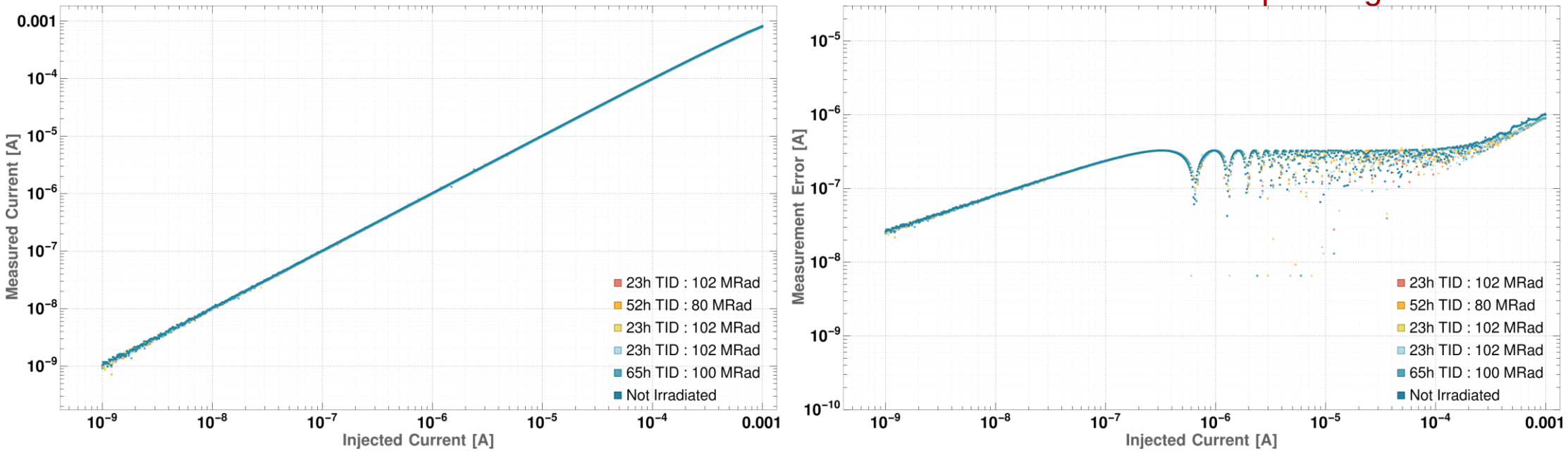
- The tests carried out reported performance well inside specifications
- The electronics noise is below 500fA
- The characterisation methodology procedures has been consolidated
- X-Rays test at TID of 1MGy does not reported conversion behaviour drifts



Latest Testbench Architecture

BLMASIC: first post-irradiation results (version 2)

100 µs Integration



- Conversion characteristic (left plot) and absolute errors (right plot)
- by a logarithmic current sweep of 500 values from 1 nA to 1 mA. The averaging time window is set to 100 μs.

Relative error :

- Below 10 % from currents greater than 3μA
- Below 1 % from 35μA to 1mA

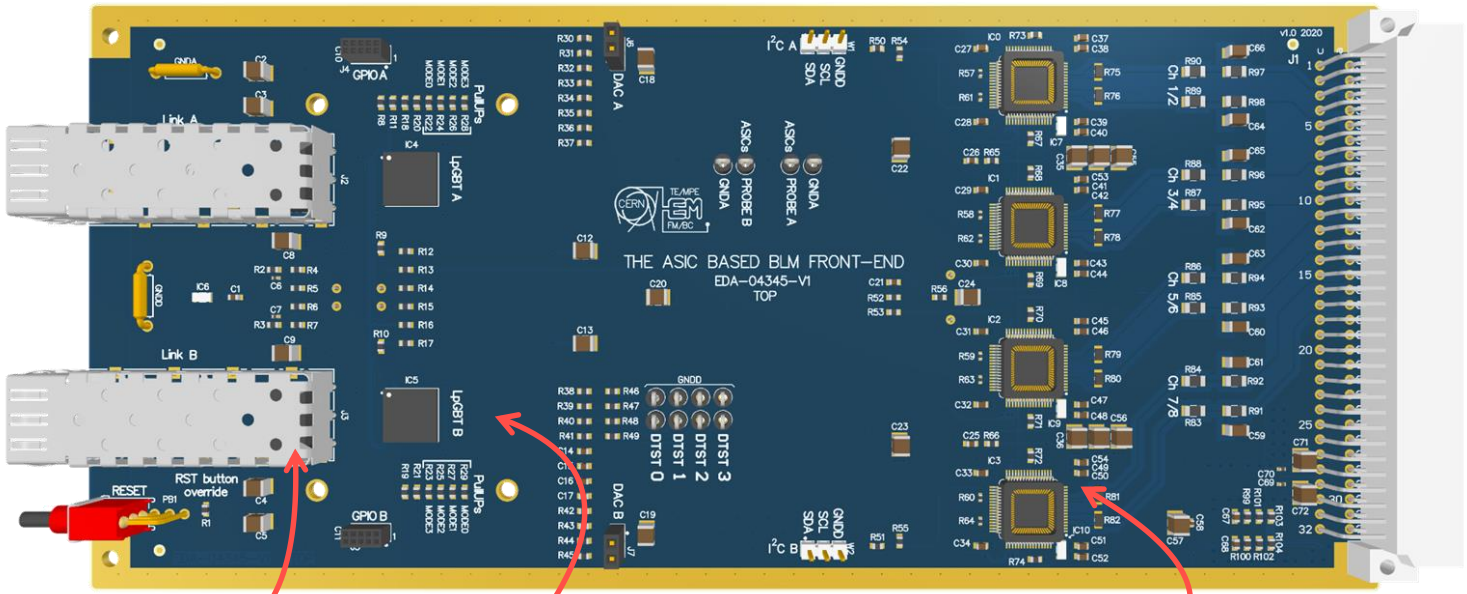
BLEIC: Printed Circuit Board Prototype (1/2)

New prototype PCB design complete

- Includes all functionalities expected from the final system
- Common digital parts, control and form with standard BLM acquisition board.
- Secured prototypes of the other custom parts, e.g. the SM-VTRx and LpGBT.

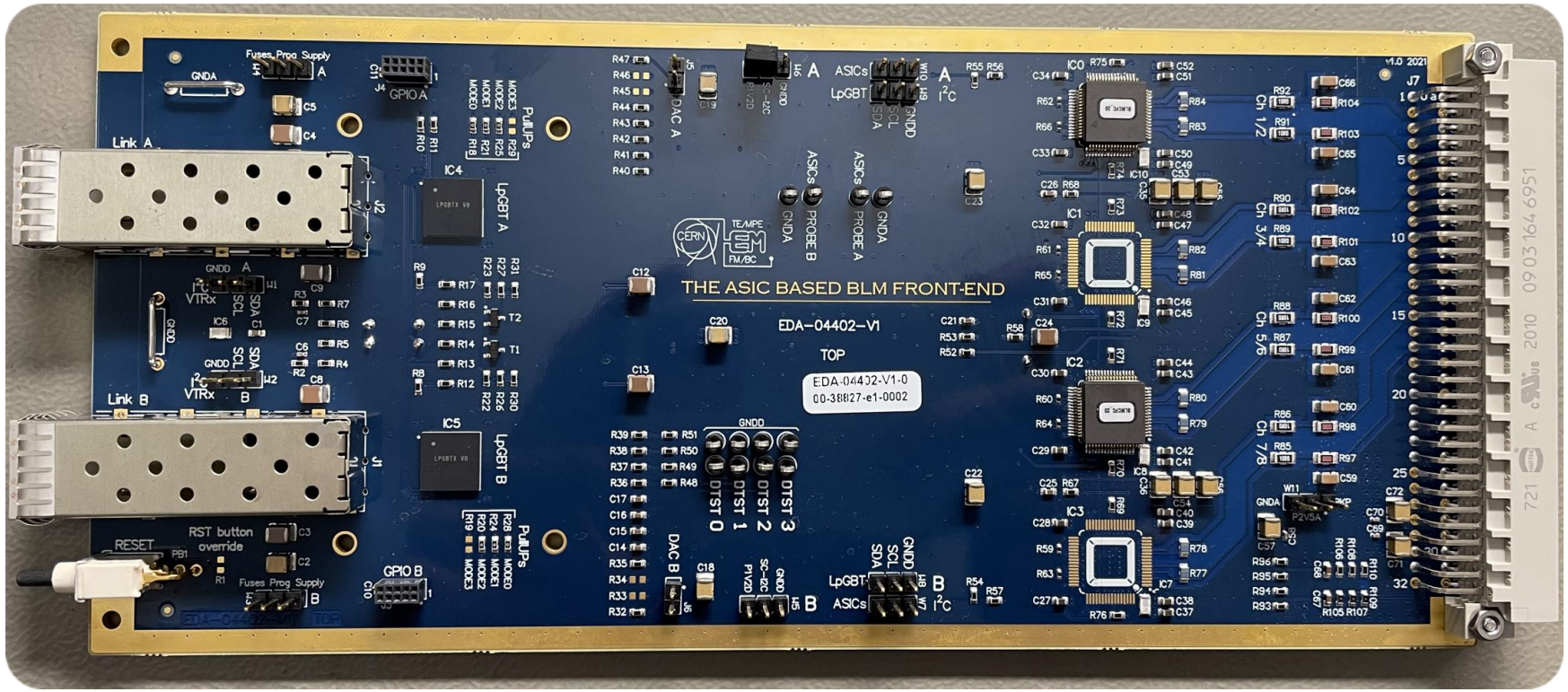
Prototype production completed and tested to be functional

- This board variant is able to accommodate both BLMASIC v2 & v3



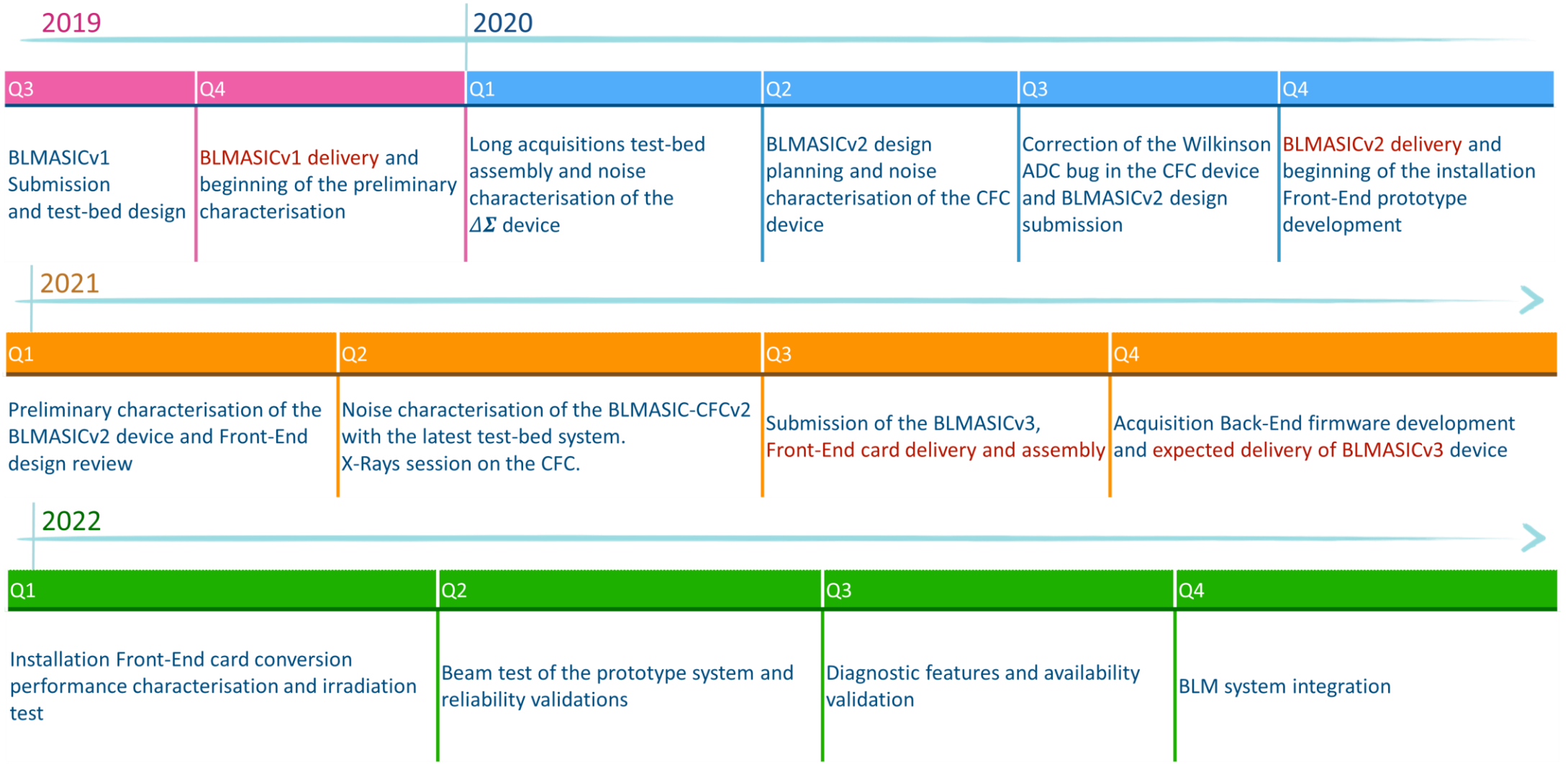
BLEIC: Printed Circuit Board Prototype (2/2)

- Components: < 400 pcs (COTS version of the board >2000)
- Cost: expected < 1 kCHF/unit (COTS version > 3 kCHF/unit)



Roadmap

Development Roadmap

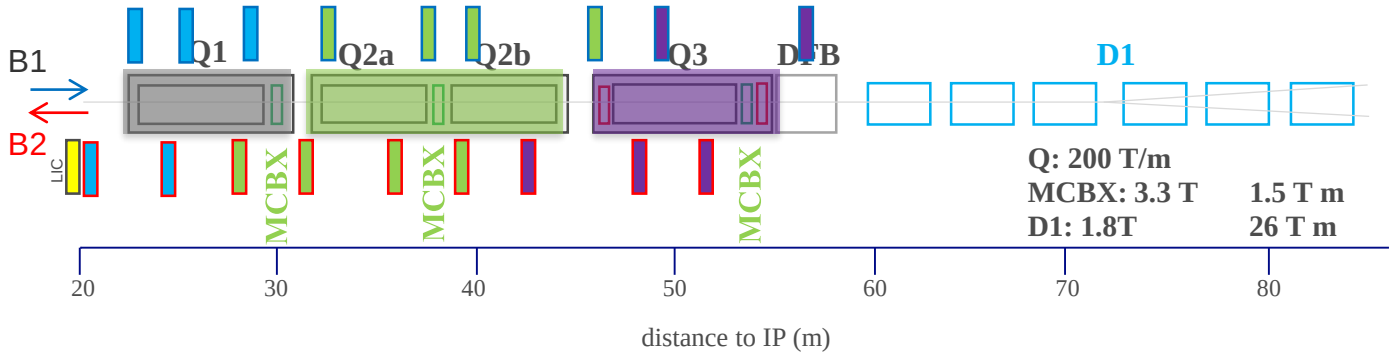


Future Deployment

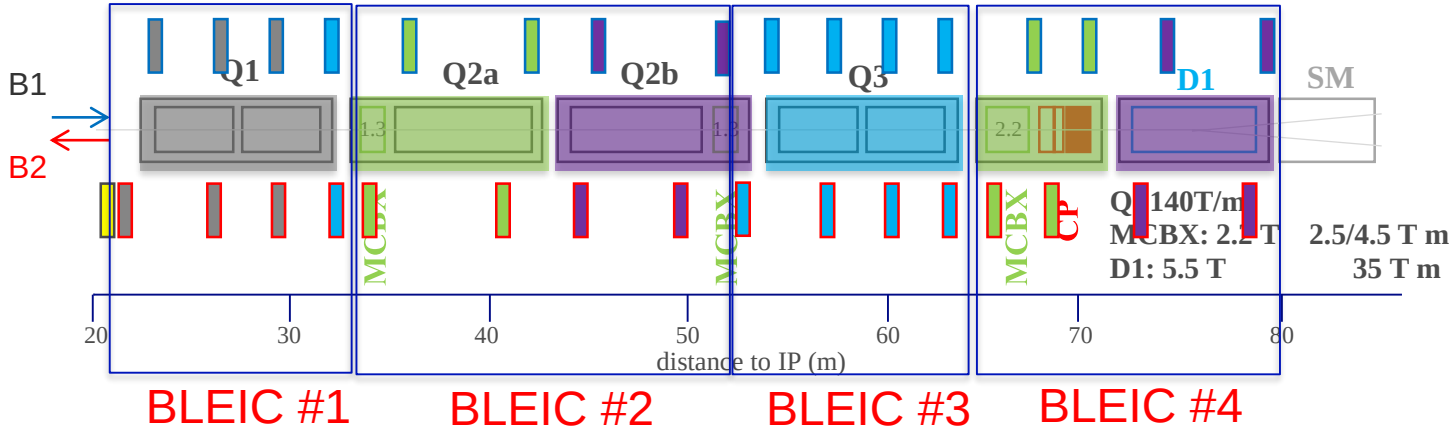
BLEIC: LS3 Triplet Layout BLM detectors

Work in progress together with WP15

LHC triplet layout



HL-LHC triplet layout



Proposal: BLECF // (BLEIC/2)

Half channel redundancy

Number of detectors: IP-side			
	Present System Run 3	HL-LHC Upgrade Run 4	New in Run 4
BLECF – standard	18	32	14
BLEIC – new	0	**16**	16
subtotal	18	48	30

Number of detectors: IP1 + IP5 (both sides)			
	Present System Run 3	HL-LHC Upgrade Run 4	New in Run 4
BLECF – standard	72	128	56
BLEIC – new	0	**64**	64
Total IP1+IP5	**72**	**192**	**120**

1 multiwire cable / module
1 BLEIC module = 8 channels

Conclusions

- Development progress is well advanced
  - Several parts already in functional prototype phase
  - Characterisation of ASIC version 2 showed encouraging results; more checks in the pipeline
  - Version 3 of ASIC focuses on the current-to-frequency method only
  - Latest version of the ASIC is expected in the next weeks
- Demonstrated advantages of ASIC based version of the acquisition electronics
  - Extremely compact PCB to host all functionalities
  - Lower costs and maintenance effort
  - Backwards compatible with the standard COTS version
- Main functionalities
  - Radiation tolerant electronics up to 1 kGy
  - 10 µs acquisition period & real-time processing
  - 8 orders of dynamic range (from few pA to 1 mA) measurements
  - On-board diagnostics and telemetry
  - Bidirectional communication with the acquisition electronics

Acknowledgements

- ADC & other rad-hard ICs:
  - Kostas Kloukinas
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HiLumi HL-LHC PROJECT

Thank you for your attention!

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