Title:

Design and characterization of depleted monolithic active pixel sensors within the RD50 collaboration

Author: C. Irmler, P. Sieberer, T. Bergauer on behalf of the RD50 CMOS Working Group

Abstract (1500 char)

The CERN RD50 CMOS working group is designing and characterizing DMAPS for use in high radiation environment fabricated in the LFoundry 150nm HV-CMOS process. The first iteration of this chip, the RD50-MPW1 suffered from high leakage current, low breakdown voltage and crosstalk. In order to mitigate these shortcomings, an improved version with improved pixel geometry was designed. The RD50-MPW2 consists of 8x8 pixels with analog frontend, but no digital periphery. The chip was delivered in early 2020 and extensively characterized within lab-measurements, an irradiation campaign and beam tests. To read out the chips the Caribou DAQ system is used with a custom chipboard as well as specific firmware and software modules. A third iteration of the chip, the RD50-MPW3, will be submitted to LFoundry end of October 2021 and is expected to be delivered in early 2022. It will keep the well working analog part of its predecessor, completed by an in-pixel digital logic and an optimized peripheral readout for effective pixel configuration and fast serial data transmission. The chip will comprise a matrix of 64x64 pixels arranged in 32 double-columns. In parallel to chip design and production, a digital model of RD50-MPW3 is being implemented in a FPGA and used to develop and verify the readout system of the future chip. We will present an overview of the RD50 HV-CMOS activities focusing on the measurement results of RD50-MPW2 chip, as well as the design and readout of the RD50-MPW3.