Design and characterization of depleted monolithic active pixel sensors within the RD50 collaboration

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CERN-RD50 CMOS Working Group:

- Program to study and develop monolithic CMOS sensors with
  - High granularity
  - High radiation tolerance
- Our program includes
  - ASIC design
  - TCAD simulations
  - DAQ development
  - Performance evaluation

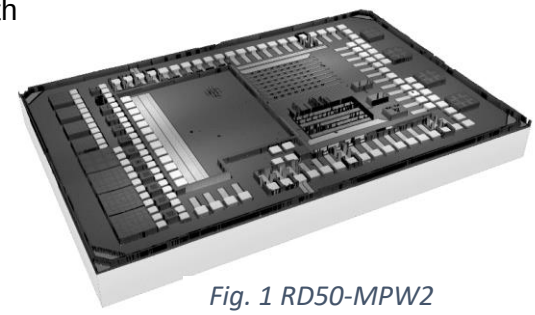

Fig. 1 RD50-MPW2

RD50-MPW1

- Process: LFoundly 150 nm HV-CMOS
- Resistivity: 600 and 1.1k Ω·cm
- Pixel size: 50 µm x 50 µm
- 40 rows, 78 columns
- Analog and digital in-pixel electronics
- FE-I3 like continuous readout

RD50-MPW2

- Resistivity: 10, 100, 1.9k and 3k Ω·cm
- Improved I_{leak} and V_{BD}
- Analog in-pixel readout only
- Pixel size: 60 µm x 60 µm
- 8 rows, 8 columns

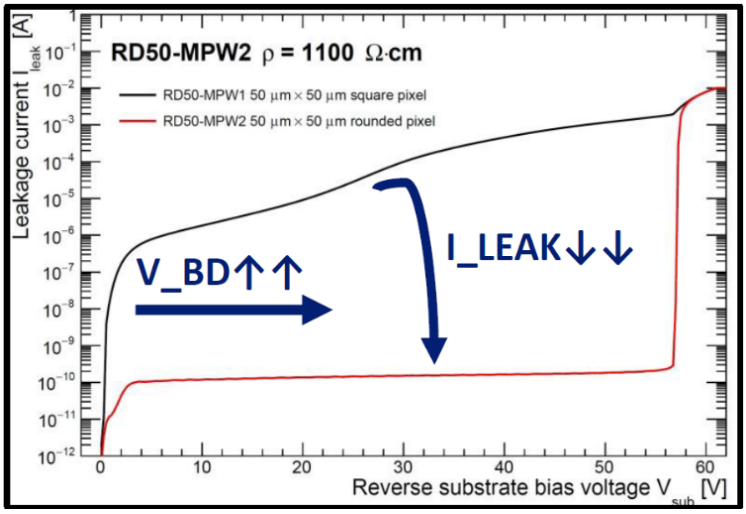

Fig. 2 IV curves of RD50-MPW1 and RD50-MPV2 chips

RD50-MPW3

- Fully equipped DMAPS with:
- Resistivity (planned): standard, 1.9k and >2k kΩ·cm
- Pixel size: 62 µm x 62 µm
- 64 rows, 64 columns
- In-pixel digital readout (FE I3 style)
- Optimized digital periphery
- I^2C configuration (via internal wishbone bus)
- Pixel arranged in double columns with end of column (EoC) each.
- Fast serial data transmission (640MHz)
- Implementing all the lessons learned from RD50 MPW1/2
- Chip submission in October 2021, delivery expected in early 2022

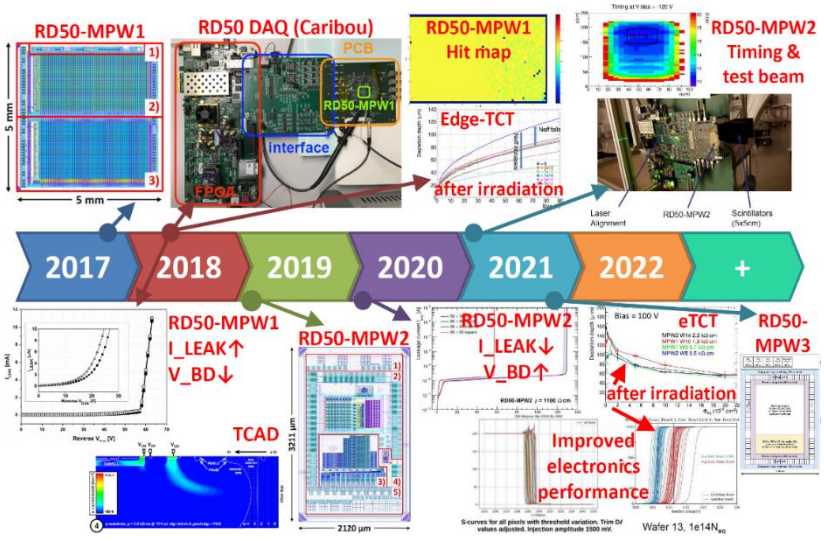

Fig. 3 Timeline of the RD50 HV-CMOS developments