4D particle tracking with monolithic silicon pixel sensors in SiGe BiCMOS

Lorenzo Paolozzi

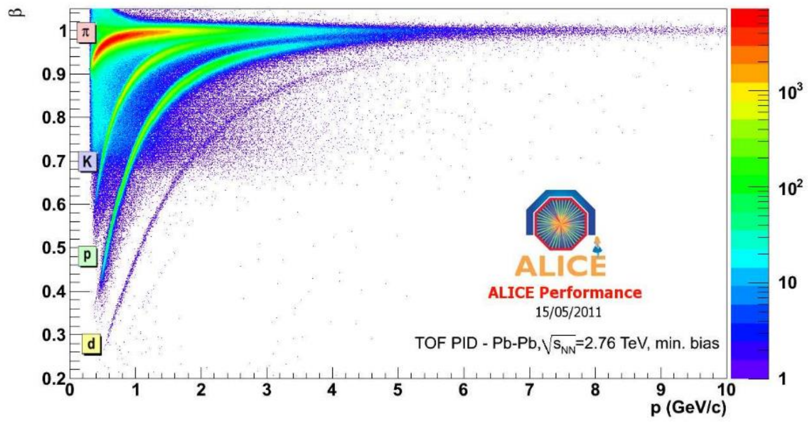
CERN

UNIVERSITÉ DE GENÈVE

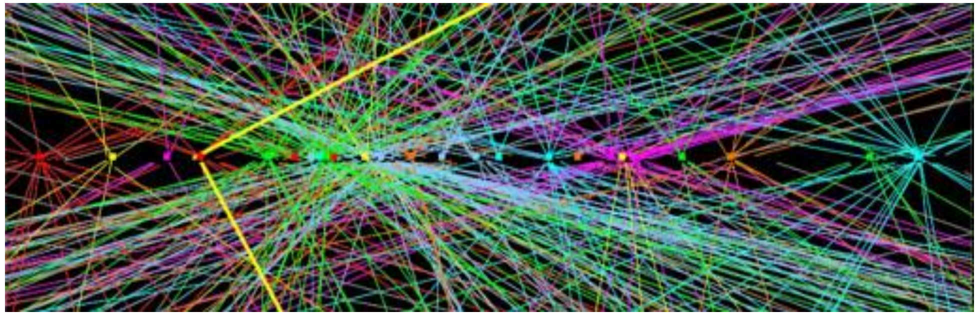
EPFL Seminar

Precise timing measurement in HEP

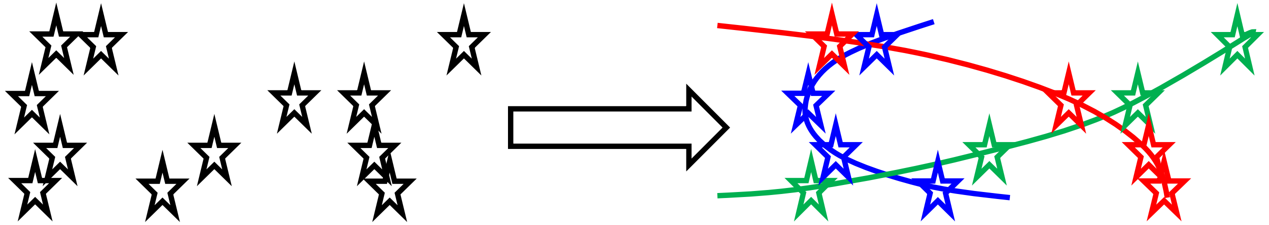
Particle identification



Pile-up suppression



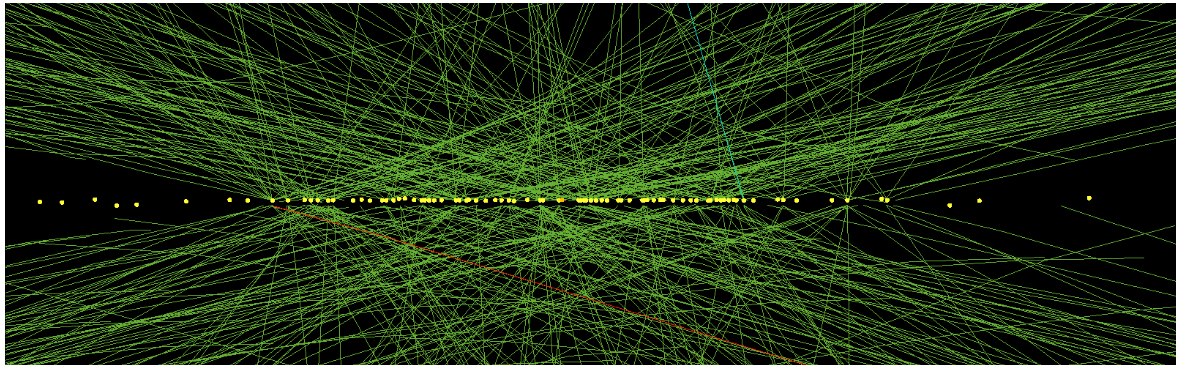
Support for fast tracking



4D tracking for pile-up suppression

Hartmut F-W Sadrozinski *et al* 2018 *Rep. Prog. Phys.* **81** 026101

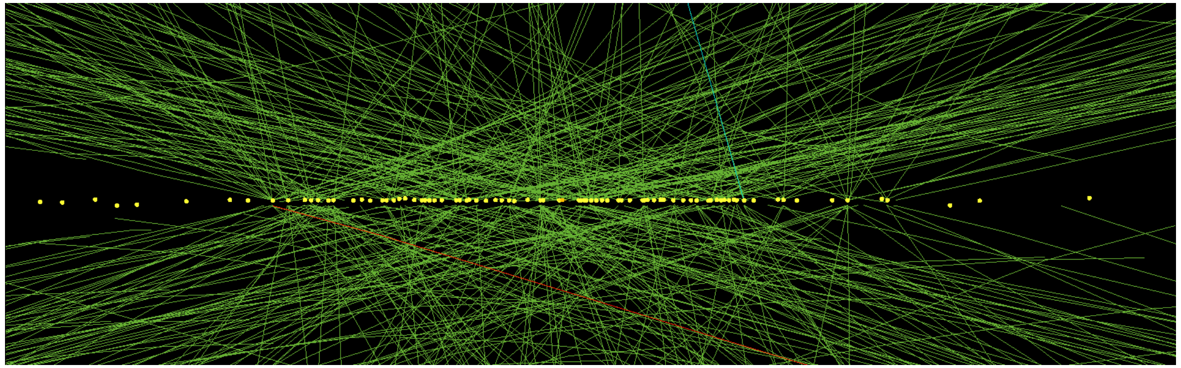
Without timing information



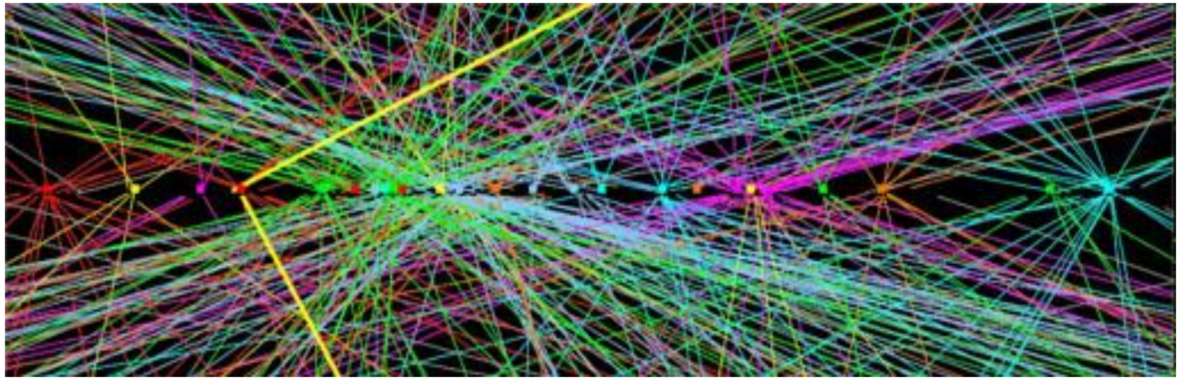
4D tracking for pile-up suppression

Hartmut F-W Sadrozinski *et al* 2018 *Rep. Prog. Phys.* **81** 026101

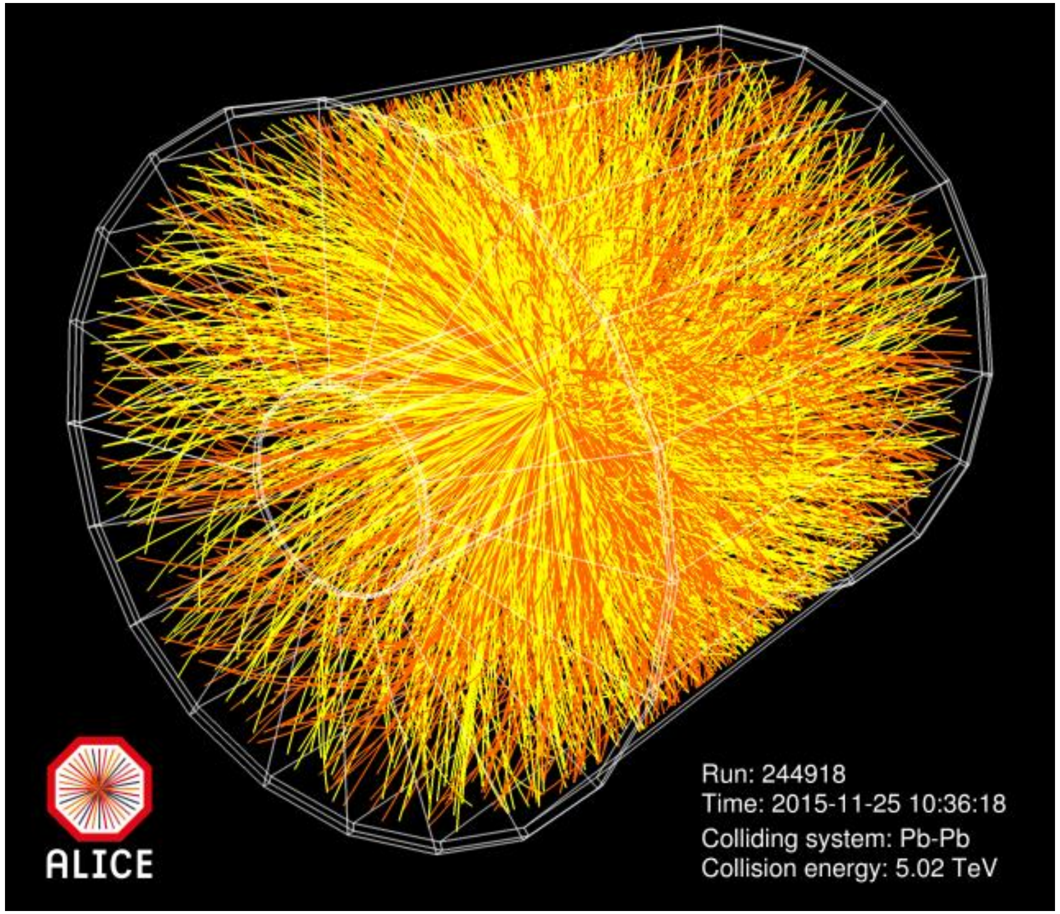
Without timing information



With timing information



4D tracking for pile-up suppression



Summary

1. **SiGe HBTs for fast, low power timing measurement.**

2. SiGe BiCMOS technologies.

3. R&D at the University of Geneva.

4. The FASER pre-shower detector.

5. The path toward picosecond time resolution.

Precise timing measurement with silicon detectors

What are the main parameters that determine the time resolution of semiconductor detectors?

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$

Precise timing measurement with silicon detectors

What are the main parameters that determine the time resolution of semiconductor detectors?

- Geometry and fields

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$

Precise timing measurement with silicon detectors

What are the main parameters that determine the time resolution of semiconductor detectors?

- Geometry and fields
- Charge collection noise

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$

Precise timing measurement with silicon detectors

What are the main parameters that determine the time resolution of semiconductor detectors?

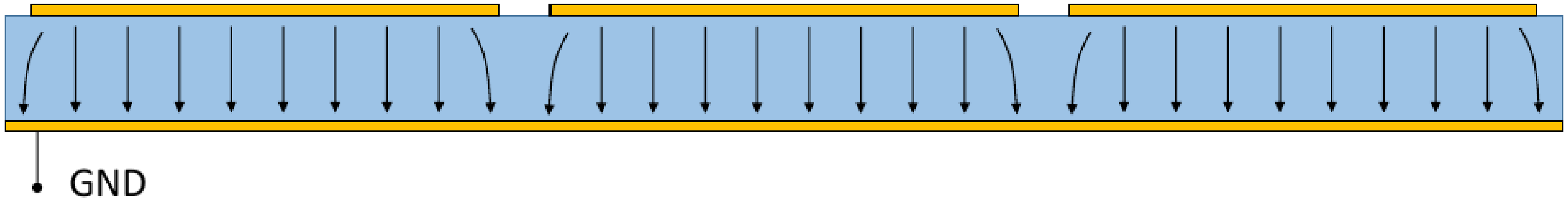
- Geometry and fields
- Charge collection noise
- Electronic noise

Induced current from the Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i}$$

1. Geometry and fields

Sensor optimization for time measurement means:
Sensor time response **independent** from the particle trajectory



→ "Parallel plate" read out: wide pixels w.r.t. depletion region

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

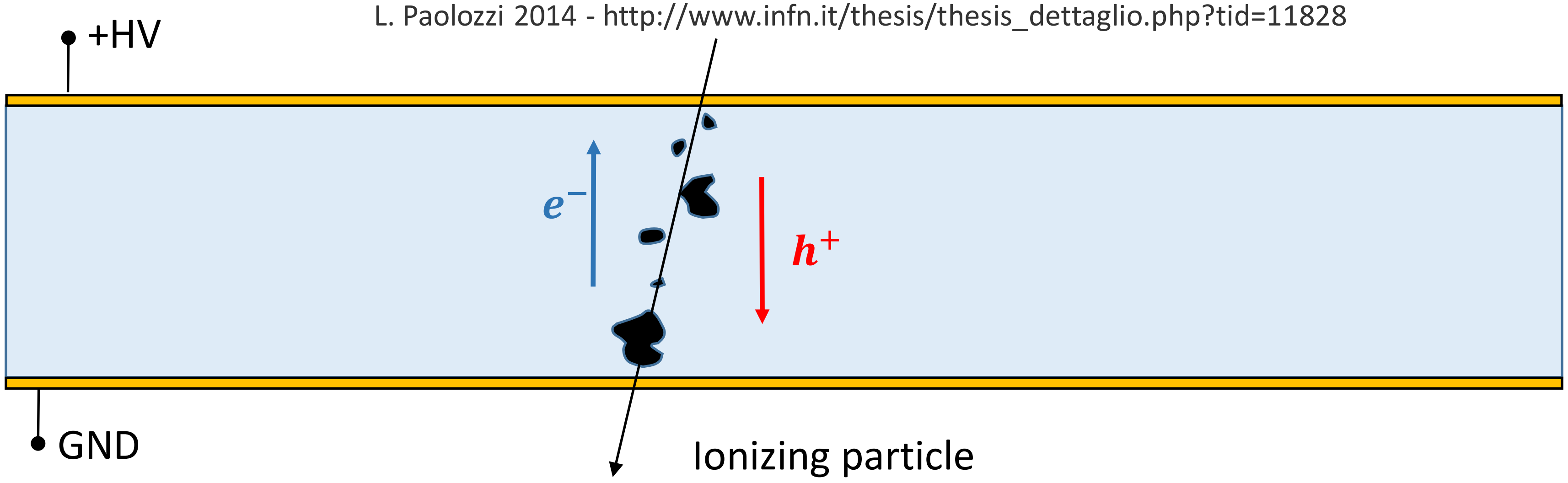
Scalar, saturated
Scalar, uniform

Desired features:

- Uniform **weighting field** (signal induction)
- Uniform **electric field** (charge transport)
- Saturated charge **drift velocity** (signal speed)

2. Charge-collection noise

L. Paolozzi 2014 - http://www.infn.it/thesis/thesis_dettaglio.php?tid=11828

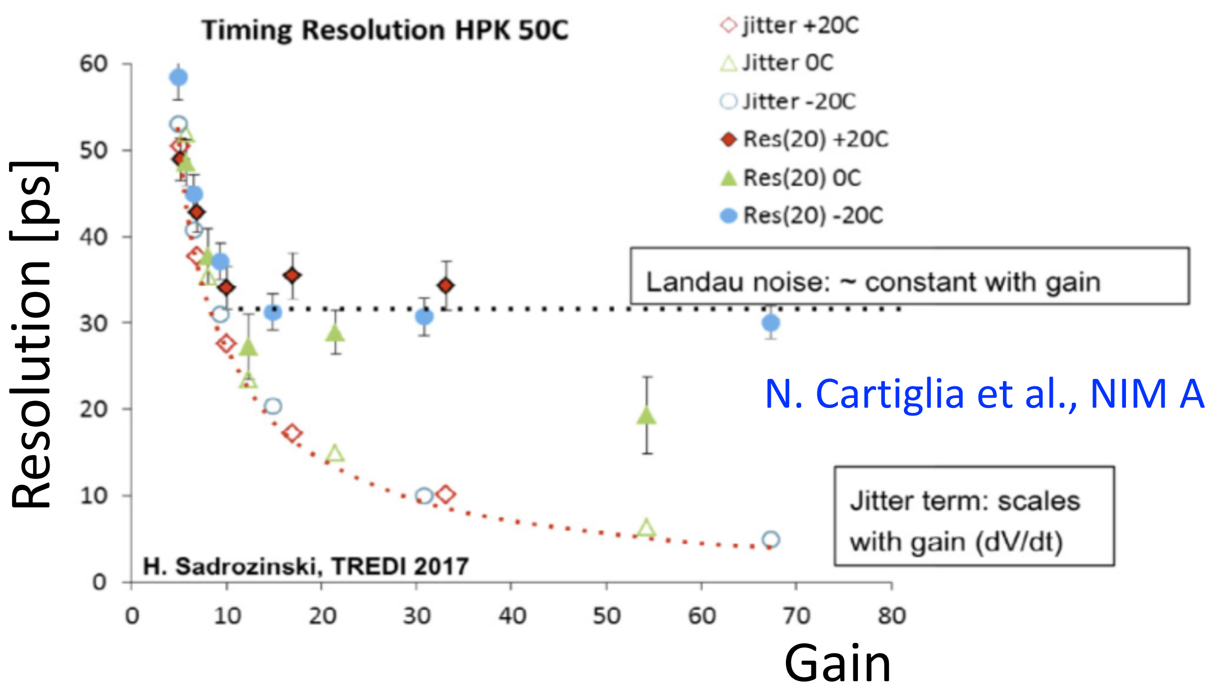


is produced by the **non uniformity of the charge deposition** in the sensor:

$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

When **large clusters** are absorbed at the electrodes, their contribution is removed from the induced current. The **statistical origin** of this variability of I_{ind} makes this effect irreducible in PN-junction sensors.

2. Charge-collection noise



N. Cartiglia et al., NIM A 924 (2019) 350-354

Charge collection noise represents an intrinsic limit to the time resolution for a semiconductor PN-junction detector.

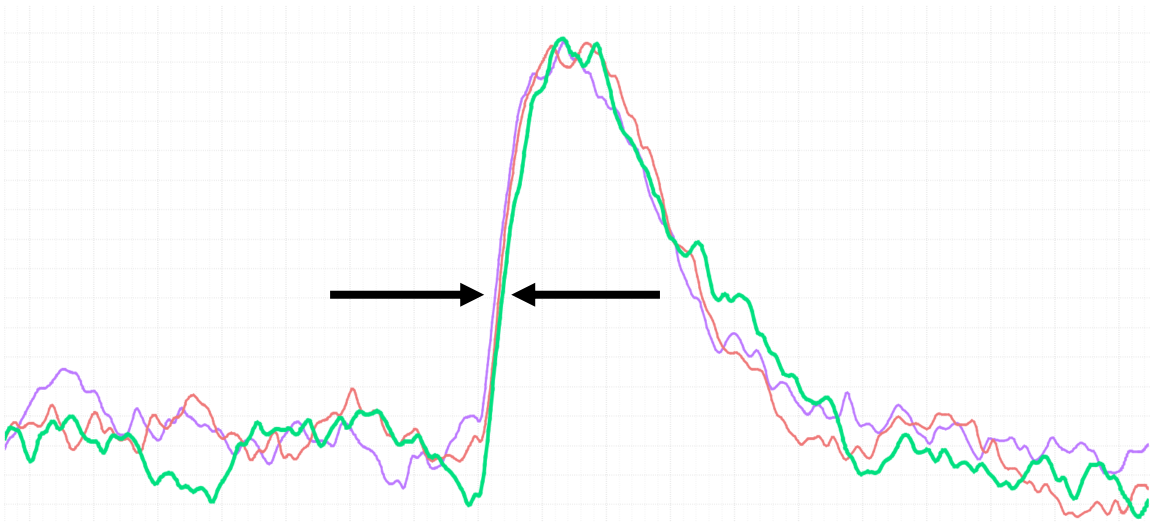
~30 ps reached by present LGAD sensors.

Lower contribution from sensors without internal gain

3. Electronic noise

Once the geometry has been fixed, the time resolution depends mostly on the **amplifier performance**.

Time jitter



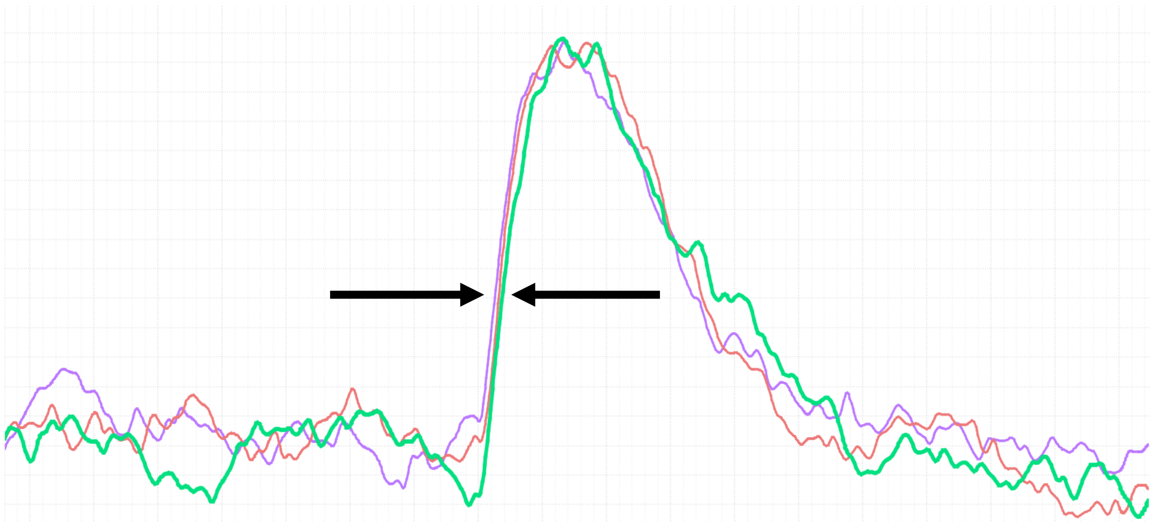
Fast integration

$$\sigma_t = \frac{\sigma_V}{dV/dt} \cong \frac{ENC}{I_{Ind}}$$

3. Electronic noise

Once the geometry has been fixed, the time resolution depends mostly on the **amplifier performance**.

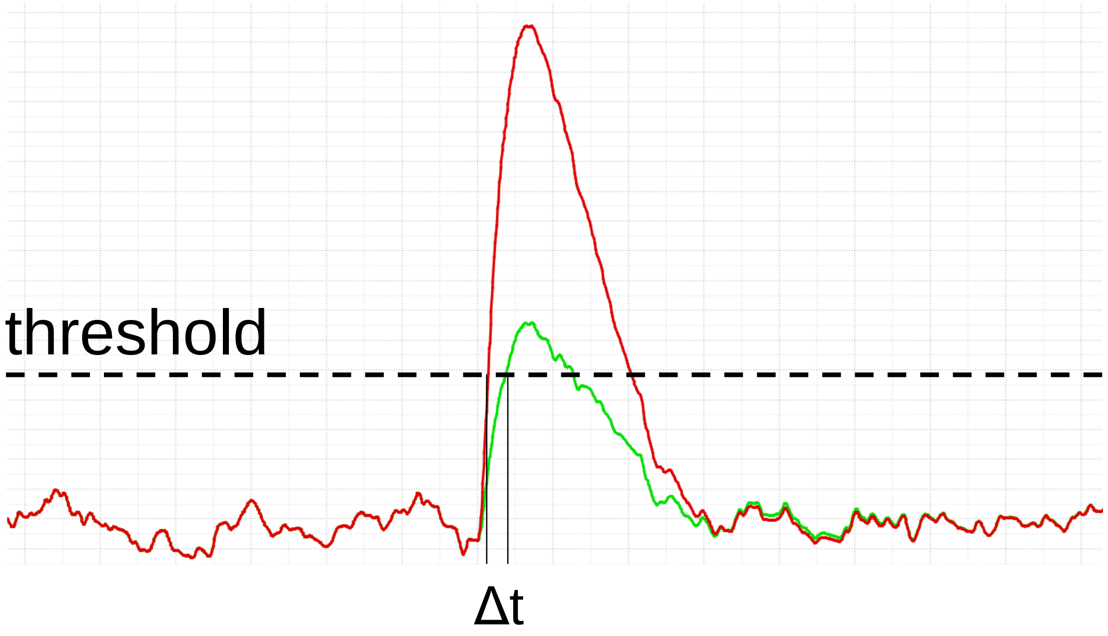
Time jitter



Fast integration

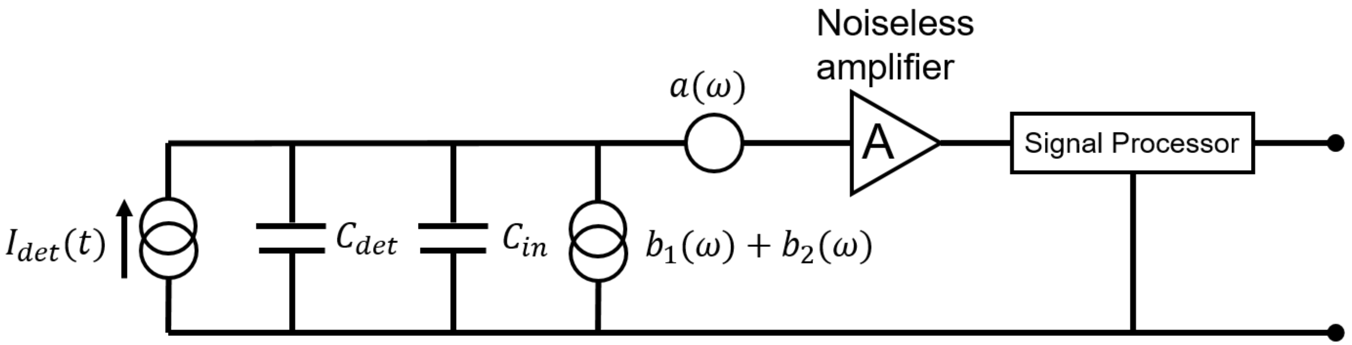
$$\sigma_t = \frac{\sigma_V}{dV/_{dt}} \cong \frac{ENC}{I_{Ind}}$$

Time walk



$$\sigma_t \propto ENC$$

Equivalent Noise Charge: device comparison

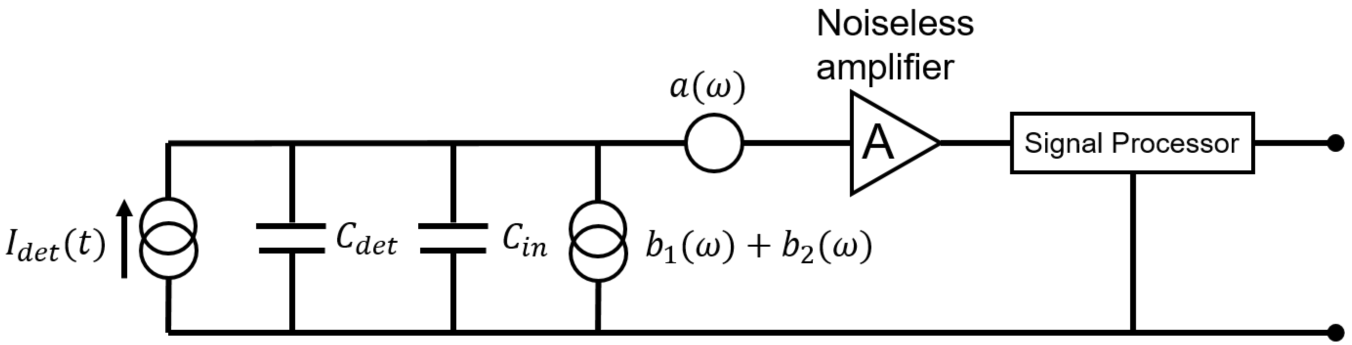


$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + A_3(b_1 + b_2)\tau_M$$

$$\tau_M \sim 1\,ns$$

How do MOS-FET and BJT compare in terms of noise?

Equivalent Noise Charge: device comparison



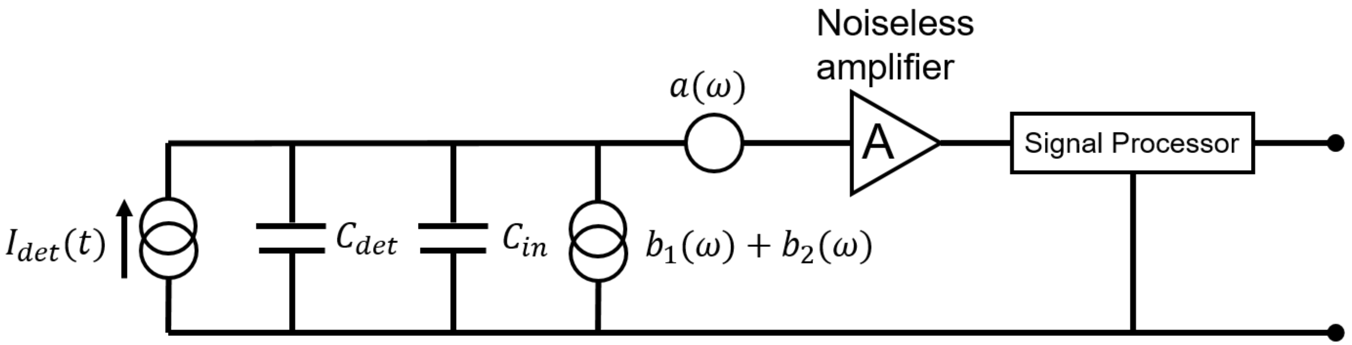
$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + A_3(b_1 + b_2)\tau_M$$

CMOS based amplifier

$$2kT\frac{h}{g_m}$$

Large $^1/_f$ contribution

Equivalent Noise Charge: device comparison



$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + A_3(b_1 + b_2)\tau_M$$

BJT based amplifier

$$ENC_{\text{series noise}} \propto \sqrt{k_1 \cdot \frac{C_{tot}^2}{\beta} + k_2 \cdot R_b C_{tot}^2}$$

Goal: maximize the current gain β at high frequencies while keeping a low base resistance R_b

Equivalent Noise Charge

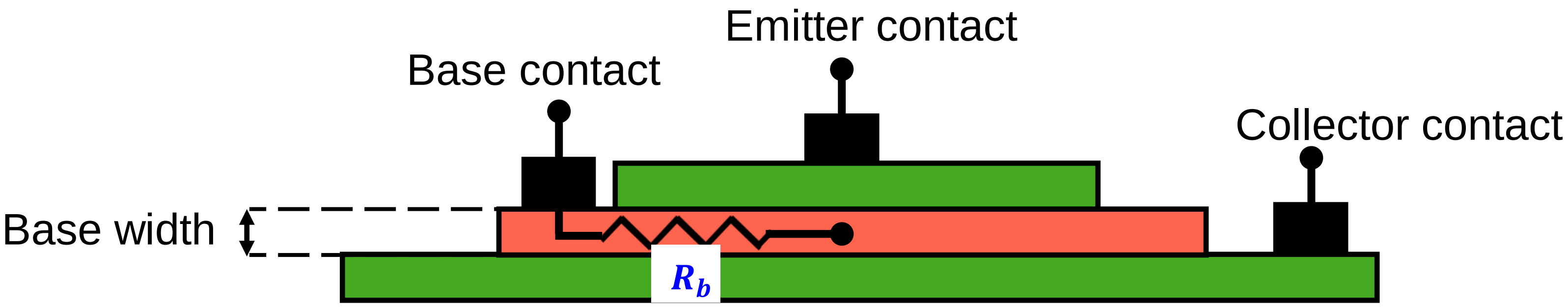
For a NPN BJT, the amplifier current gain β can be expressed as:

$$\beta = \frac{i_C}{i_B} = \frac{\tau_p}{\tau_t}$$

τ_p = hole recombination time in Base

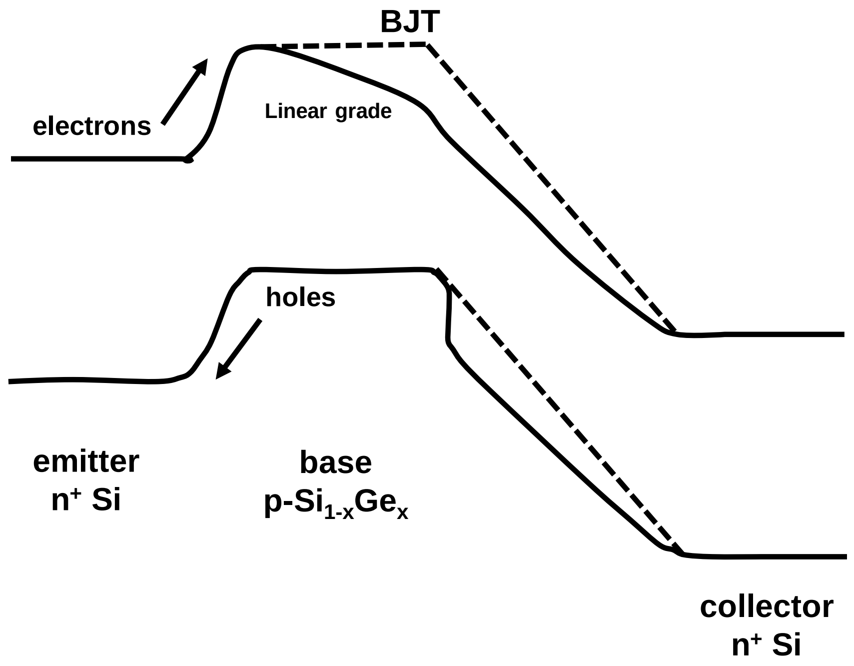
τ_t = electron transit time (Emitter to Collector)

Large $\beta \Longrightarrow$ Minimize the electron transit time



SiGe HBT technology for low-noise, fast amplifiers

In SiGe Heterojunction Bipolar Transistors (HBT) the **grading** of the bandgap in the Base changes the **charge-transport mechanism** in the Base from **diffusion** to **drift**:



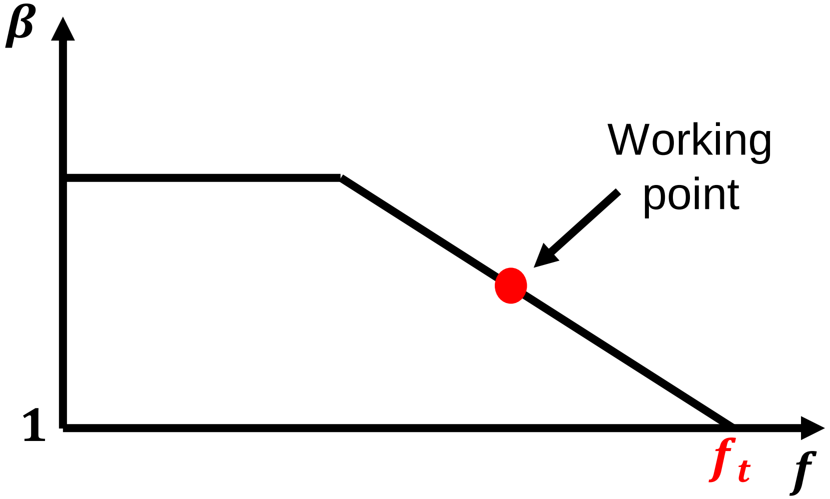
Grading of germanium in the base:
field-assisted charge transport in the Base,
equivalent to introducing an electric field in the Base

$\Longrightarrow$ short e$^-$ transit time in Base $\Longrightarrow$ very high β

$\Longrightarrow$ smaller size $\Longrightarrow$ reduction of R_b and very high f_t

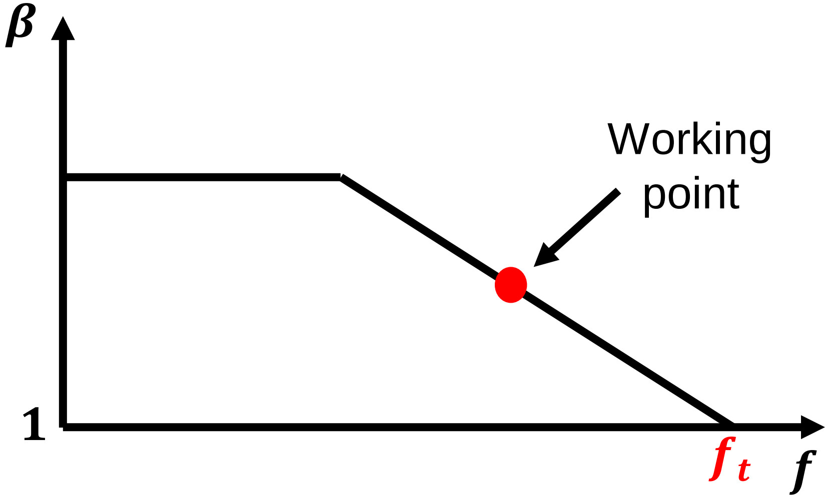
Hundreds of GHz

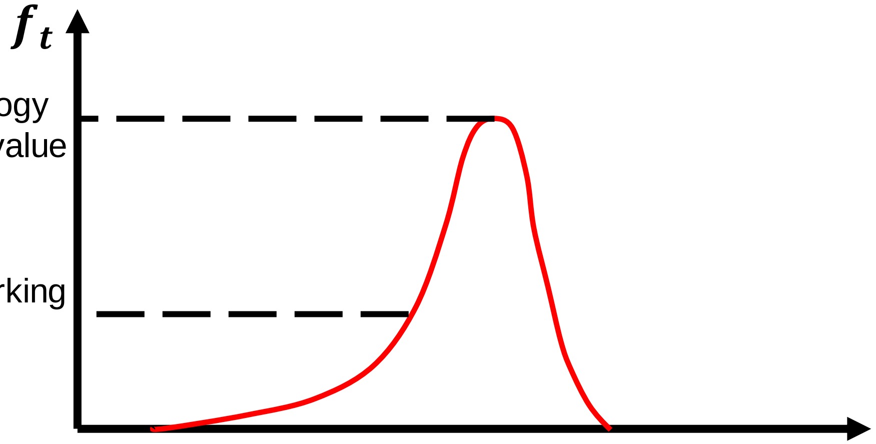
Current gain and power consumption: f_t is the key



	$f_t = 10\ GHz$	$f_t = 100\ GHz$
β_{max} at $200\ MHz$	50	500
β_{max} at $1\ GHz$	10	100
β_{max} at $5\ GHz$	2	20

Current gain and power consumption: f_t is the key





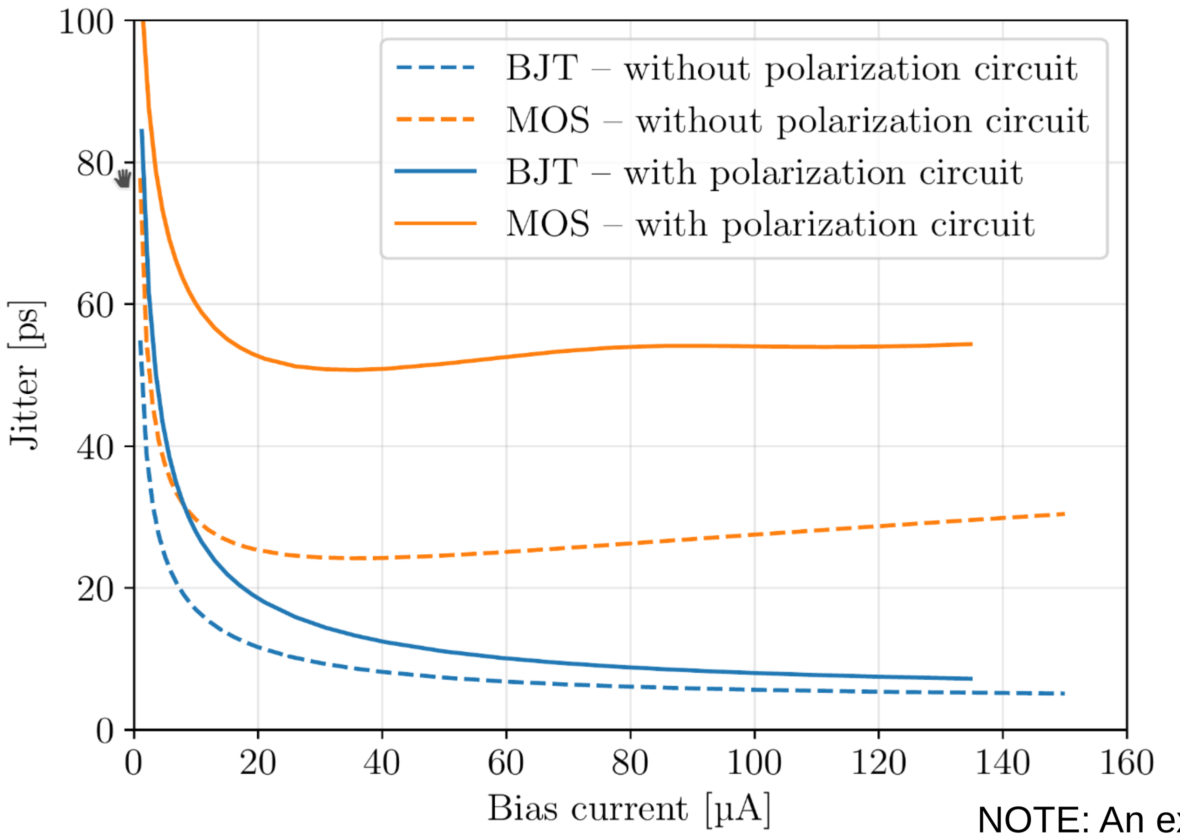
	$f_t = 10\ GHz$	$f_t = 100\ GHz$
$\beta_{max}\ at\ 200\ MHz$	50	500
$\beta_{max}\ at\ 1\ GHz$	10	100
$\beta_{max}\ at\ 5\ GHz$	2	20

Trade-off: **ENC** ⇔ **Power Consumption**

$f_t > 100\ GHz$ technologies are necessary for fast, low-power amplification.

SiGe HBT vs CMOS (our simulation)

Intrinsic amplifier jitter, an example:
Common emitter (source) configuration in a 130nm technology.



NOTE: An extra parasitic capacitance was accounted for the insulation of the HBT from substrate.

Summary

1. SiGe HBTs for fast, low power timing measurement.

2. **SiGe BiCMOS technologies.**

3. R&D at the University of Geneva.

4. The FASER pre-shower detector.

5. The path toward picosecond time resolution.

SiGe BiCMOS: A commercial VLSI foundry process

source: https://towerjazz.com/technology/rf-and-hpa/sige-bicmos-platform/

Some applications

- Automotive radars (27/77 GHz)
- Satellite communications
- LAN RF transceivers (60 GHz)
- Point-to-point radio (V-band, E-band)
- Defense
- Security
- Instrumentation

A **fast-growing technology: f_{max} = 700 GHz** transistor recently developed (DOT7 project, IHP microelectronics)

SiGe BiCMOS: A commercial VLSI foundry process

Some foundries offering SiGe BiCMOS:

- IHP Microelectronics (→ Research Inst.)
- Towerjazz
- Globafoundries
- TSMC
- STm
- AMS
- …

Implemented as an adder module to an existing CMOS technologies.

⇩

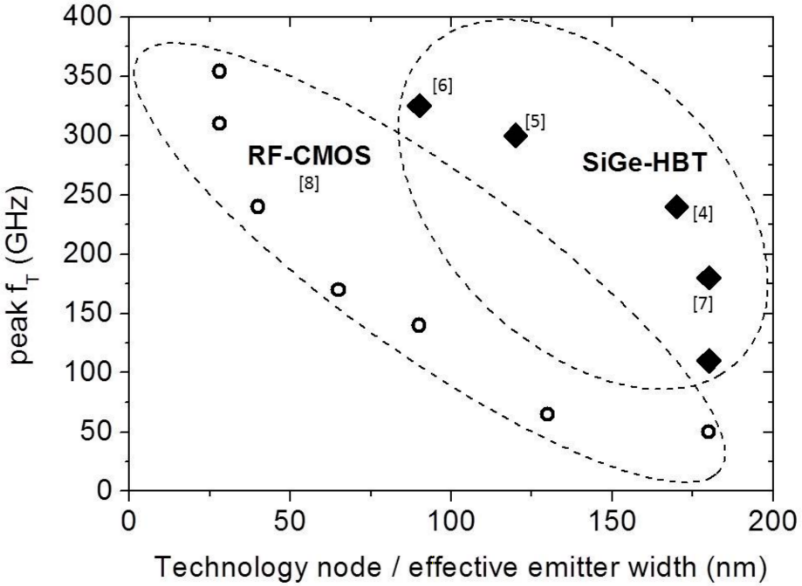
Typical increase for same tech. node in cost: ~10-15 %

Some characteristics of SiGe

- Integrated in CMOS platforms ⟹ SiGe-HBT AND Si-CMOS
- Vertical transport device ⟹ Not as dependent on lithography as CMOS
- Cryogenic compatible ⟹ Silicon-based device operating at < 1 K
- Inherently rad. hard ⟹ Good radiation tolerance with standard processing
- High output current drive ⟹ Tolerance to parasitics

A comparison with CMOS technologies

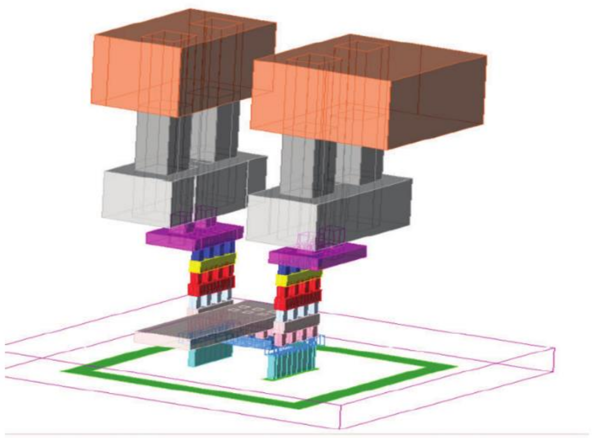
Intrinsic performance

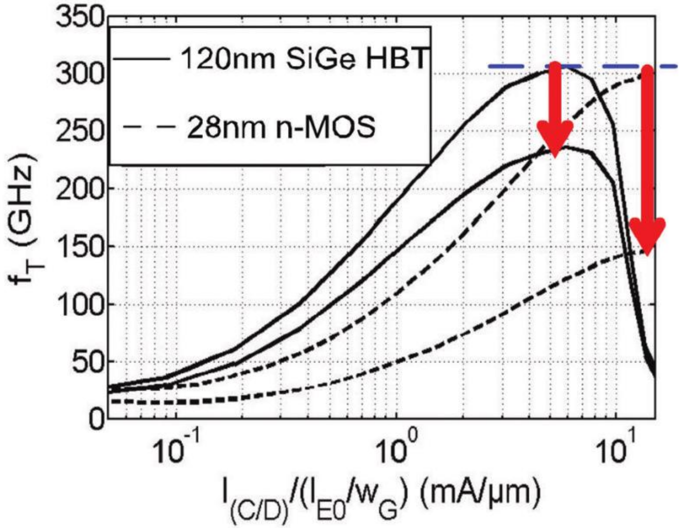


A. Mai and M. Kaynak, SiGe-BiCMOS based technology platforms for mm-wave and radar applications.
DOI: 10.1109/MIKON.2016.7492062

Robustness to parasitics

M. Schröter, U. Pfeiffer and R. Jain, Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications.





SiGe HBT scaling

Figure of merit	SiGe HBT		CMOS	
	Base	Scaling	Base	Scaling
f_T	Good	Improves	Good	Improves
f_{MAX}	Good	Improves	Good	Improves
NF_{MIN}	Good	Improves	Good	Improves
1/f noise	Good	Neutral	Neutral	Worsens
g_M/g_O	Good	Improves	Poor	Worsens
g_M	Good	Improves	Poor	Improves
mismatch	Good	Neutral	Poor	Worsens
linearity	Good	Neutral	Good	Worsens
voltage headroom	Neutral	Neutral	Poor	Worsens
breakdown voltage	Good	Neutral	Poor	Worsens

From: J.D. Cressler, IEEE transactions on nuclear science, vol. 60, n. 3 (2013)

SG13G2 technology from IHP Microelectronics

Exploit the properties of state-of-the-art SiGe Bi-CMOS transistors to produce an **ultra-fast, low-noise, low-power consumption** amplifier

Leading-edge technology: **IHP SG13G2**

130 nm process featuring **SiGe HBT** with

- Transistor transition frequency: $f_t = 0.3\,THz$
- DC Current gain: $\beta = 900$
- Delay gate: **1.8 ps**

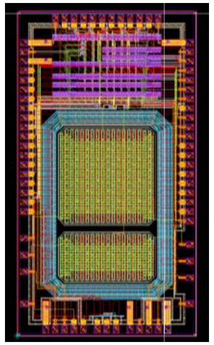
innovations for high performance microelectronics

Leibniz-Institut für innovative Mikroelektronik

Summary

1. SiGe HBTs for fast, low power timing measurement.
2. SiGe BiCMOS technologies.
3. **R&D at the University of Geneva.**
4. The FASER pre-shower detector.
5. The path toward picosecond time resolution.

2016



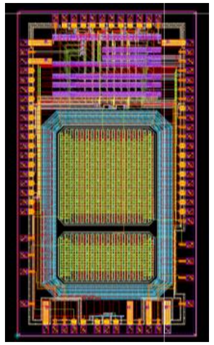
200 ps

- 1000 × 500 µm pixel.
- Discriminator output.
- **200 ps time resolution.**

For the a TOF PET Project

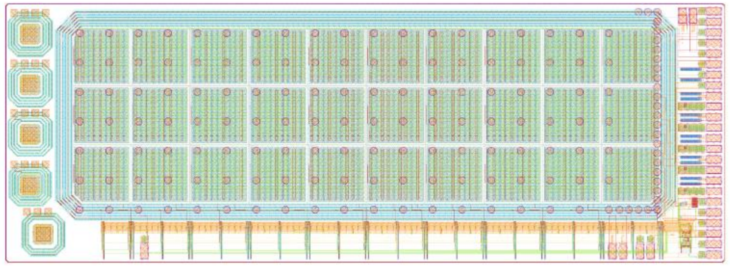
Monolithic silicon pixel sensors in SiGe BiCMOS technology

2016



200 ps

2017



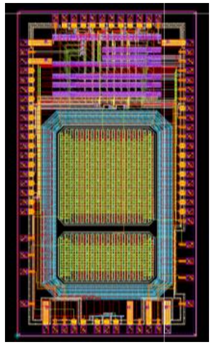
100 ps

For the a TOF PET Project

Monolithic silicon pixel sensors in SiGe BiCMOS technology

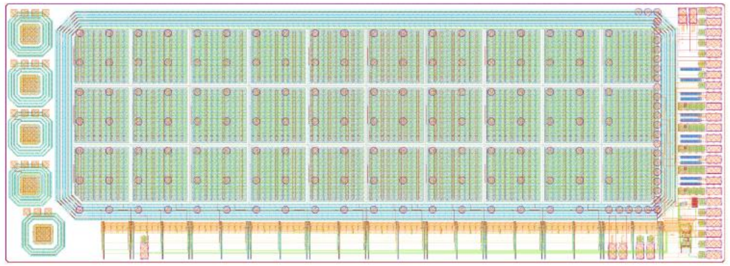
- 500 × 500 µm pixels
- 100 ps TDC + I/O logic
- **100 ps time resolution.**

2016



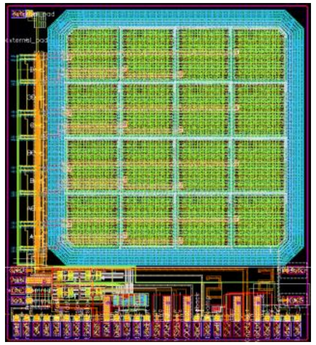
200 ps

2017



100 ps

2019



TT-PET

For the a TOF PET Project

Monolithic silicon pixel sensors in SiGe BiCMOS technology

- 500 × 500 µm pixels
- TDC + I/O logic
- 100 ps time resolution.
- **Minor bug fixes on TDC.**

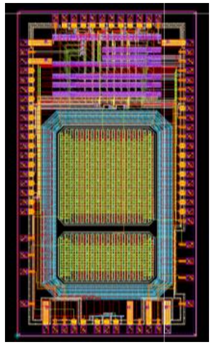
Monolithic silicon pixel sensors in SiGe BiCMOS technology

UNIVERSITÉ DE GENÈVE

innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik

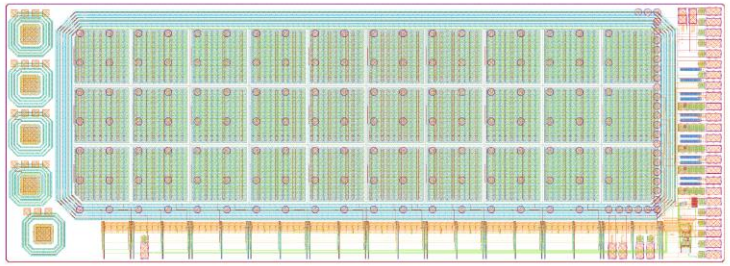
INFN Sezione di Roma Tor Vergata

2016



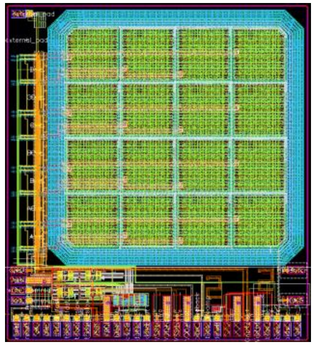
200 ps

2017



100 ps

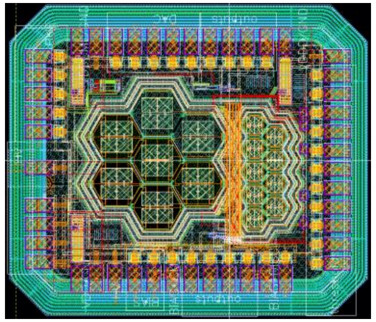
2019



TT-PET

For the a TOF PET Project

2018



50 ps

- 65µm side, hexagonal pixels
- Discriminator output
- **50 ps time resolution**

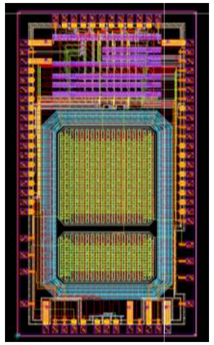
For HEP timing sensor R&D

UNIVERSITÉ DE GENÈVE

innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik

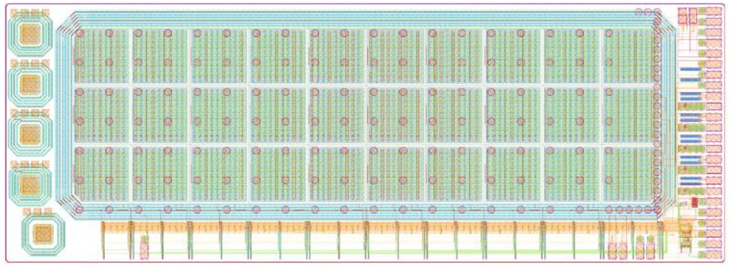
INFN Sezione di Roma Tor Vergata

2016



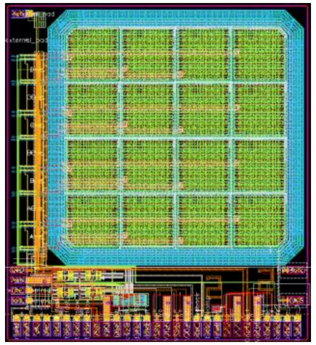
200 ps

2017



100 ps

2019

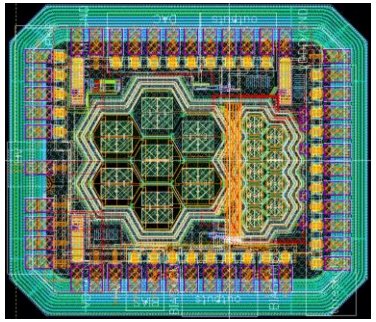


TT-PET

For the a TOF PET Project

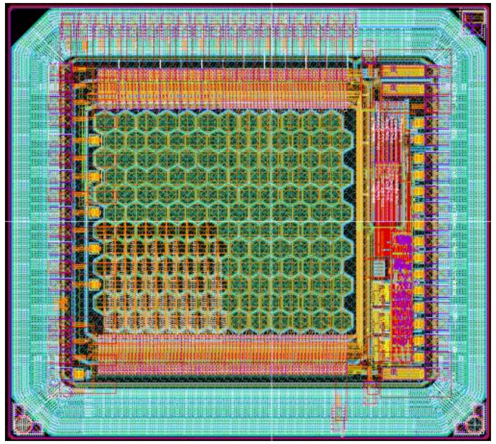
Monolithic silicon pixel sensors in SiGe BiCMOS technology

2018



50 ps

2019



New results

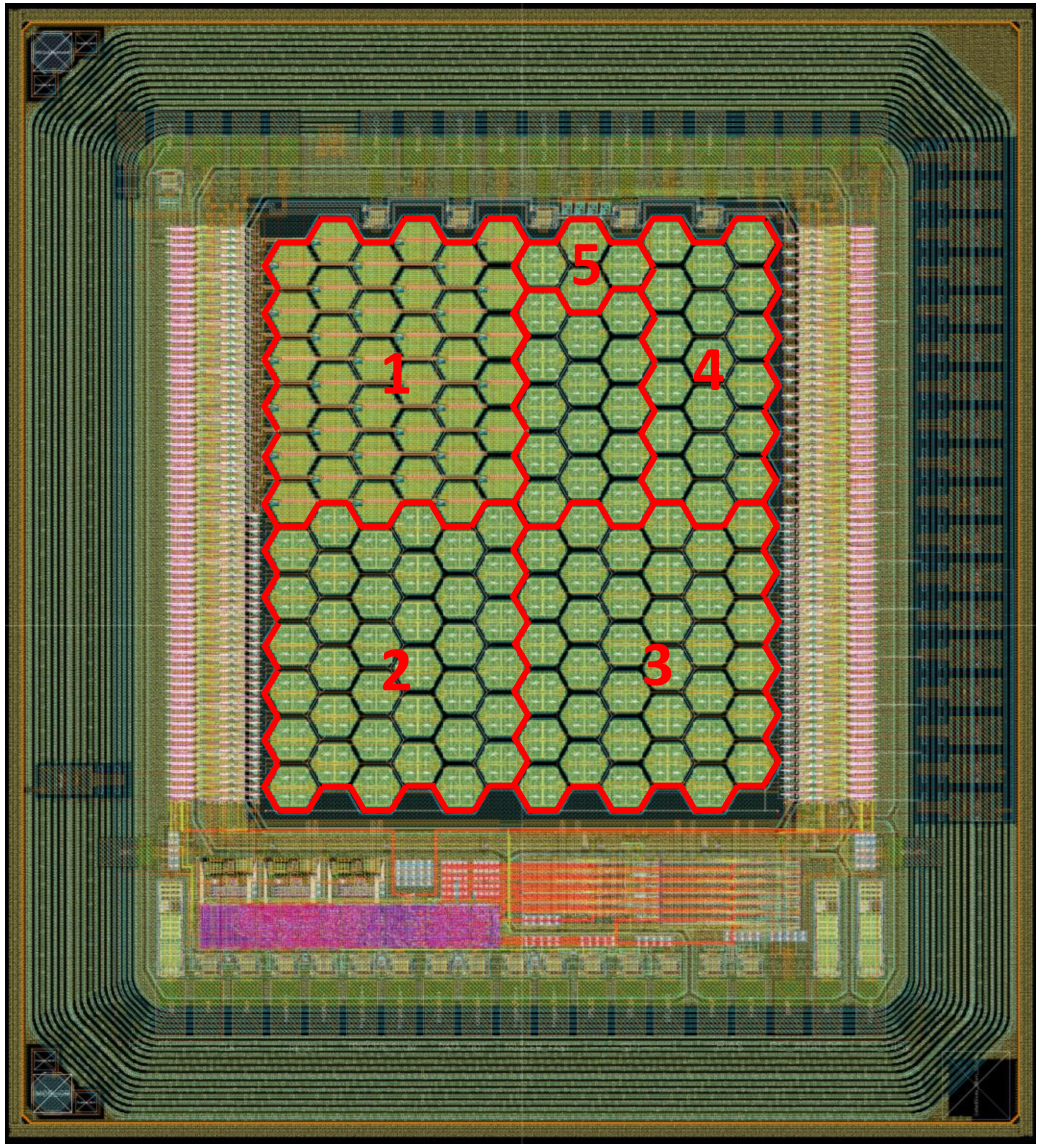
2021

For HEP timing sensor R&D

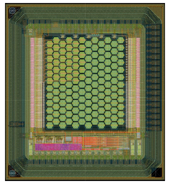
The “ATTRACT” prototype

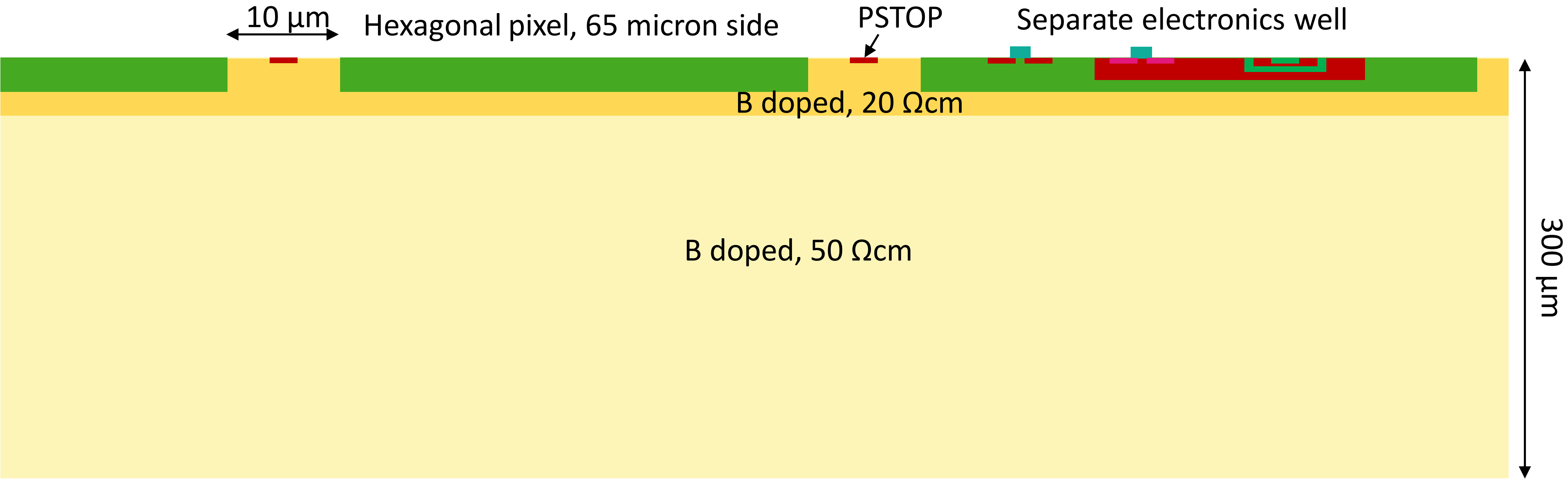
- MPW submission in 2019 funded by H2020 ATTRACT MonPicoAD project
  Prototype chip with 5 different pixel matrices for R&D investigation

1. Active pixel:
   - Front End in pixel
   - HBT preamp + driver (in pixel) + CMOS discriminator (outisde pixel)
2. TT-PET version:
   - HBT preamp + CMOS discriminator
3. Limiting amplifier:
   - HBT preamp + HBT limiting amplifier
4. Double Threshold:
   - HBT preamp + two CMOS discriminators
5. Analogue Channels:
   - HBT preamp + two HBT Emitter Followers to 500Ω Resistance on pad.



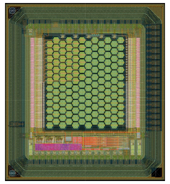
The “ATTRACT” prototype





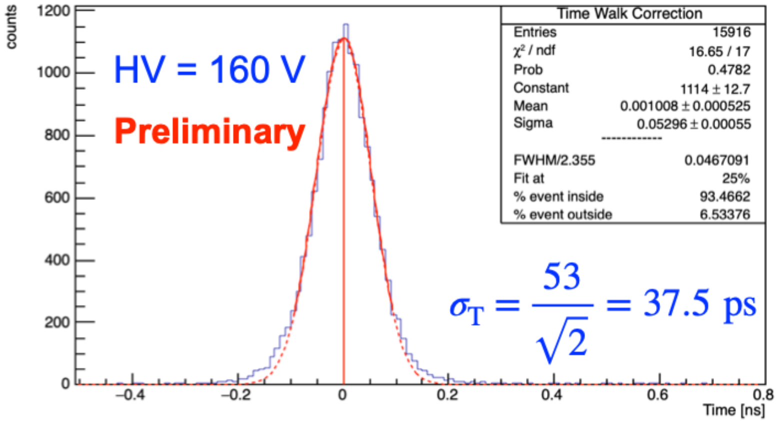
- Negative HV applied to substrate from backside and from top.
- All pixels and electronic nwells at positive low voltage.
- Typical HV: -140 V corresponds to a depletion layer of 26 µm.
  ⟹ Typical signal charge for a MIP: ~1600 electrons.

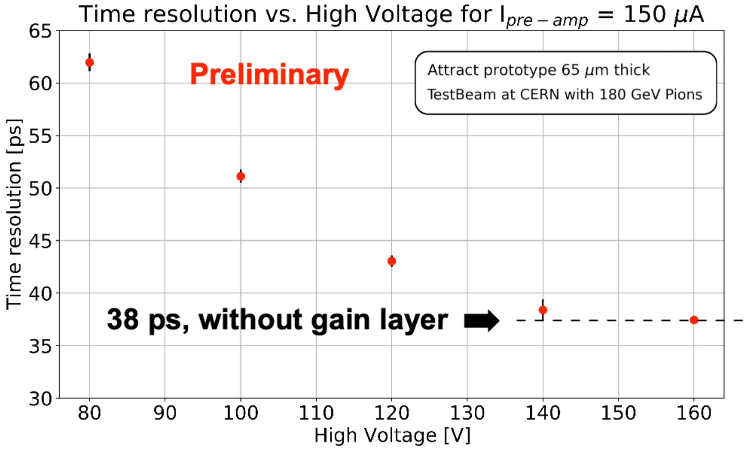
Small pixel ATTRACT prototype – test beam results



- Tested at CERN SPS testbeam in Q2 2021
  - Timing plateau at **~38 ps** and detection efficiency **>99%**

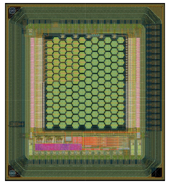
Time of flight between two sensors





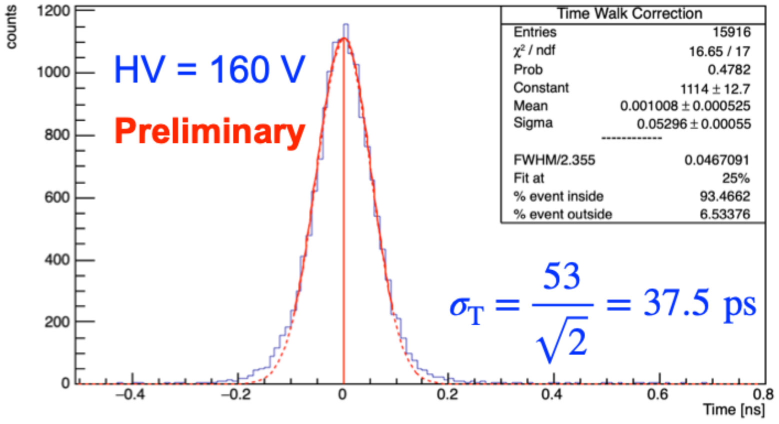
No avalanche gain

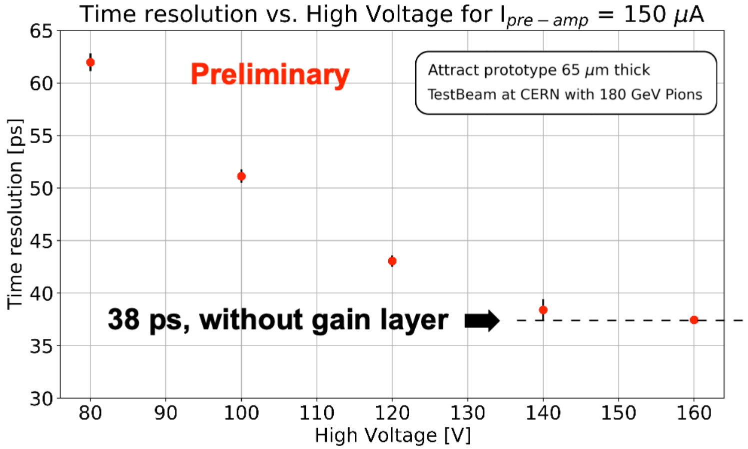
Small pixel ATTRACT prototype – test beam results

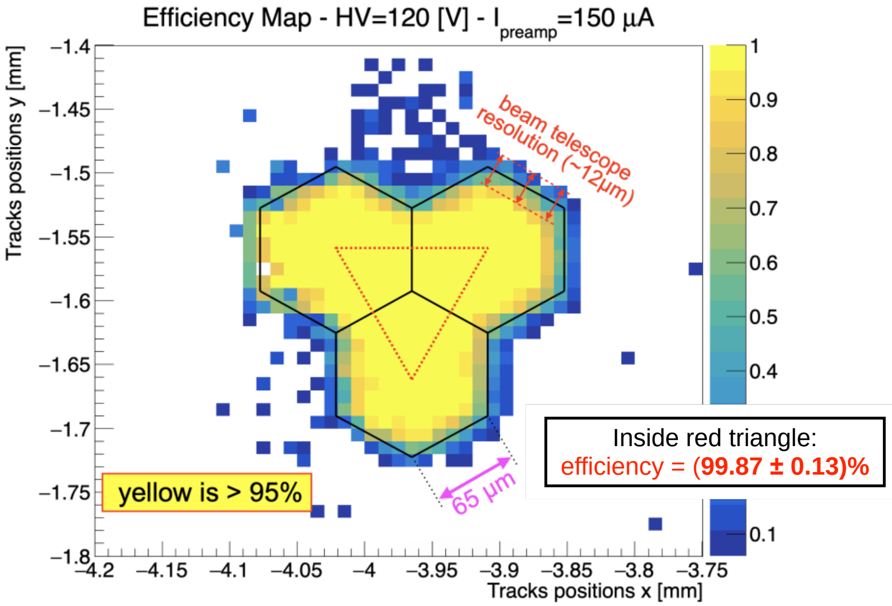


- Tested at CERN SPS testbeam in Q2 2021
  - Timing plateau at **~38 ps** and detection efficiency **>99%**

Time of flight between two sensors

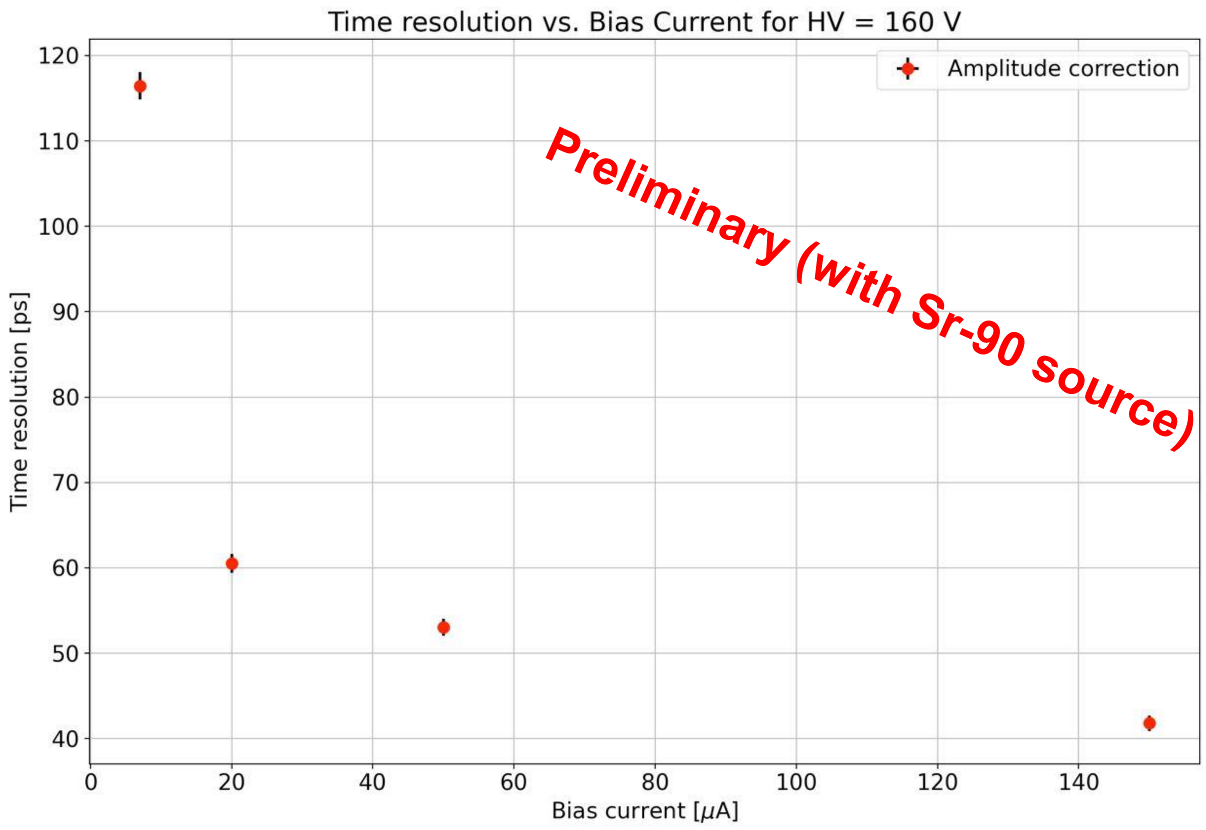






No avalanche gain

Small pixel ATTRACT prototype – power consumption



Summary

1. SiGe HBTs for fast, low power timing measurement.

2. SiGe BiCMOS technologies.

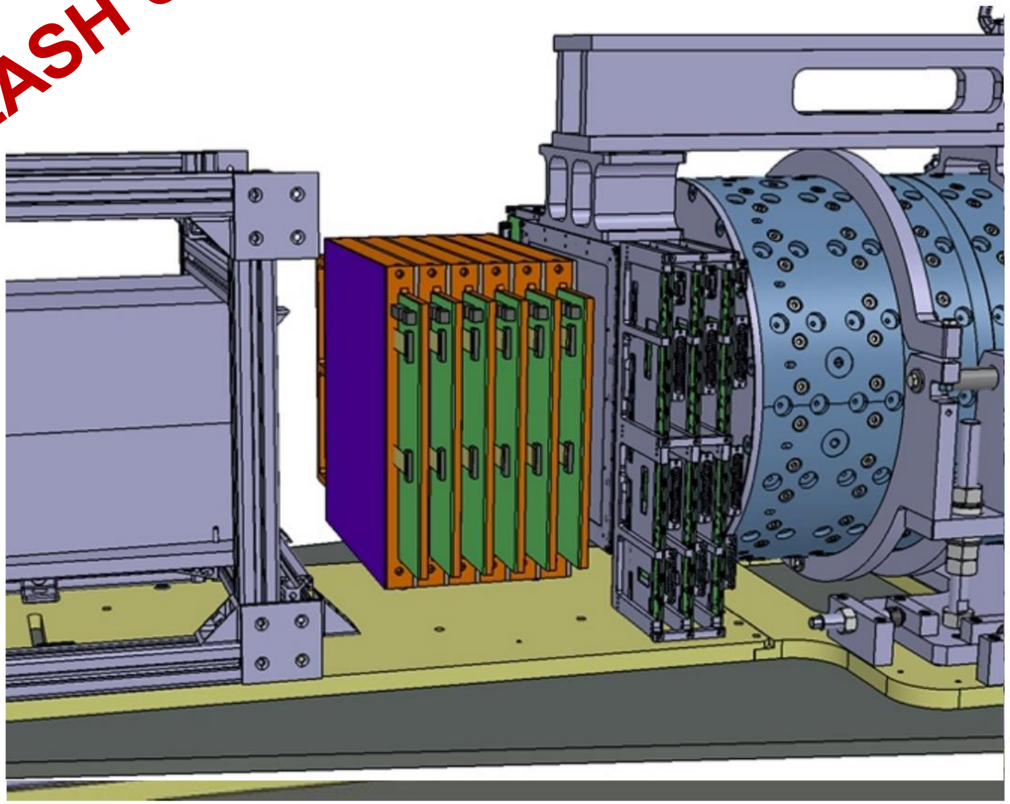
3. R&D at the University of Geneva.

4. **The FASER pre-shower detector.**

5. The path toward picosecond time resolution.

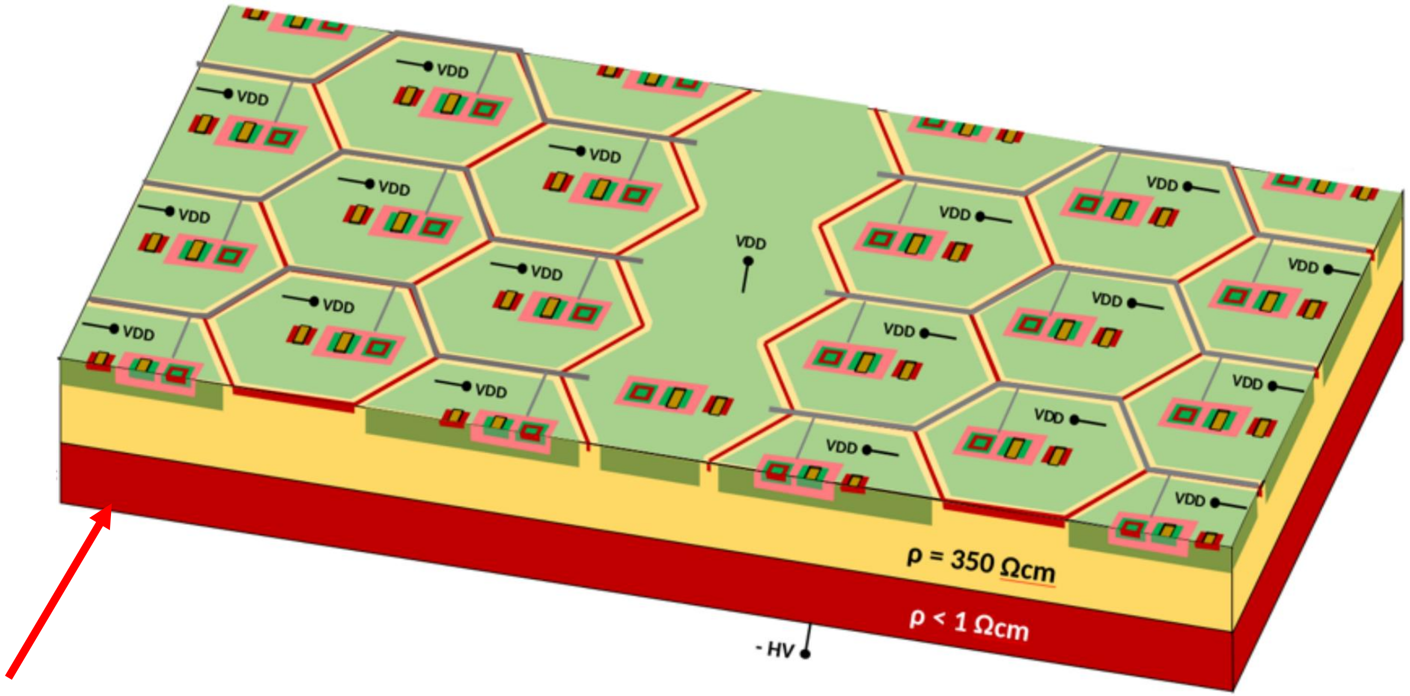
The FASER pre-shower

FLASH SLIDE



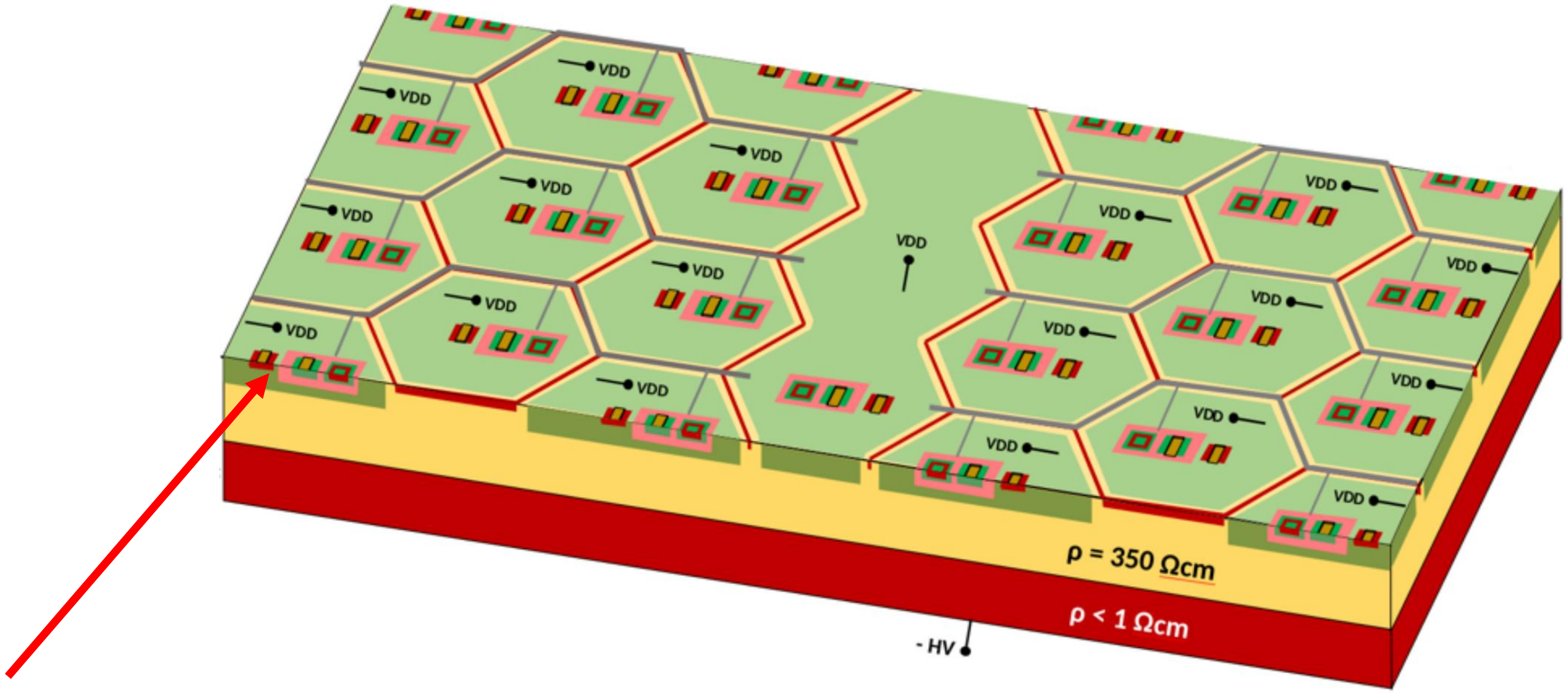
- Enable di-photon channel in FASER.
- Distinguish two ultra-collimated EM showers.
- Time resolution target: ~100 ps.
- Very large pixel dynamic range: 0.5 fC – 64 fC.
- Large area prototype submission: July 2021.
- Full-reticle ASIC submission: March 2022.

Monolithic design for 4D tracking: FASER pre-shower



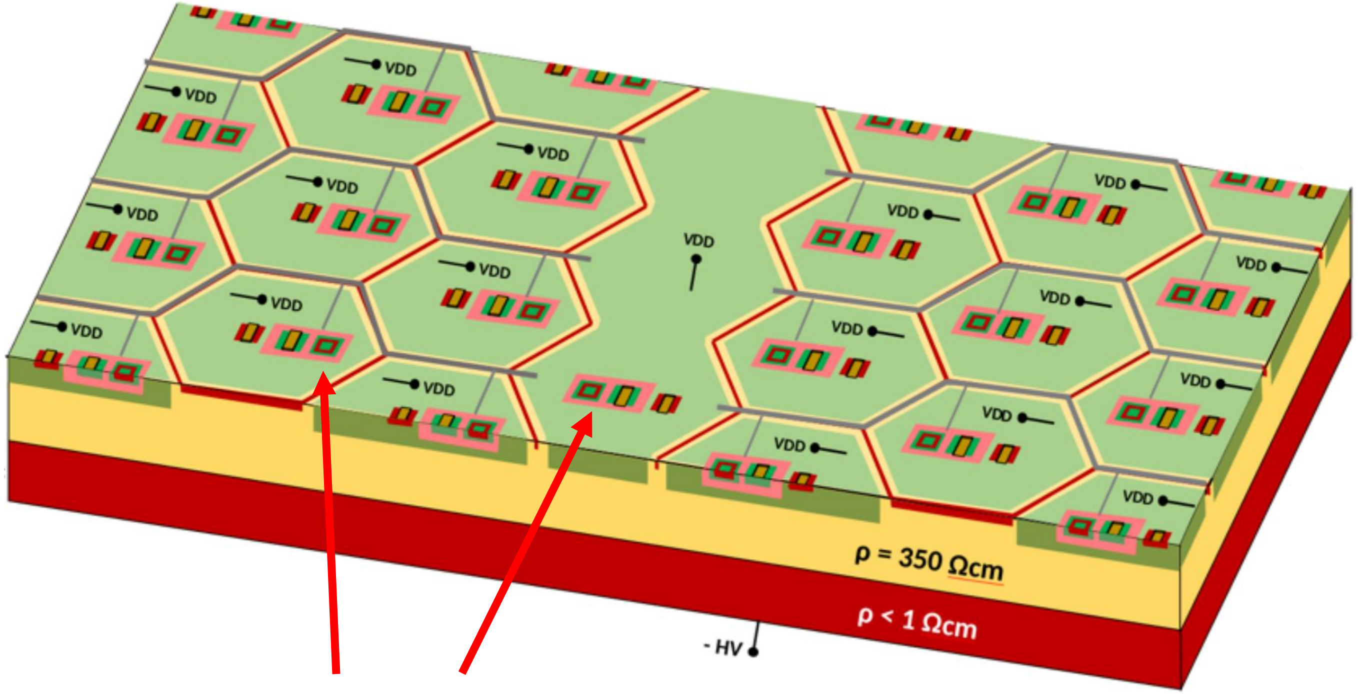
- <1 Ωcm, heavily P-doped substrate.
- Negative High Voltage applied to the substrate.

Monolithic design for 4D tracking: FASER pre-shower



- Electronics inside the guard-ring, isolated from substrate using deep n-well.
- Triple well design: polysilicon, nmos and HBTs in an isolated pwell, pmos directly in the pixel nwell.
- Pixel and electronic deep n-wells are kept at positive low voltage.

Monolithic design for 4D tracking: FASER pre-shower



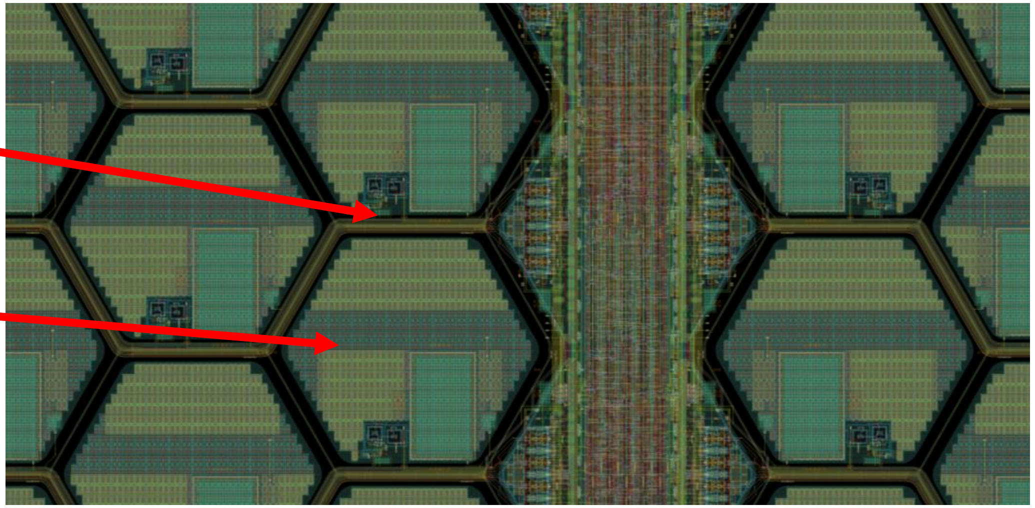
- Analogue electronics in pixel, digital electronics in a separate deep-nwell to improve noise robustness.
  >95% fill factor.

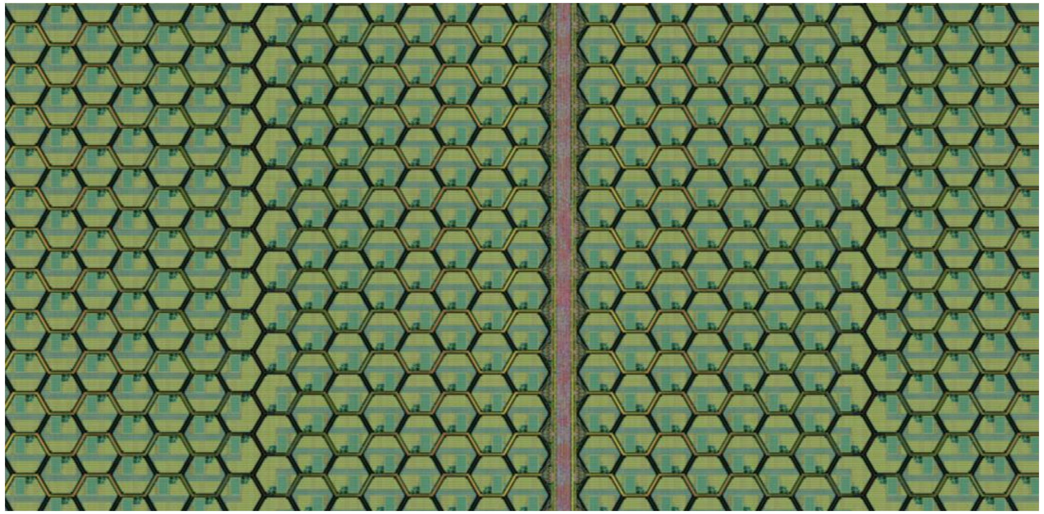
- Target time resolution: ~**100ps.**

- Very large pixel dynamic range: 0.5 fC – 64 fC.

Monolithic design for 4D tracking

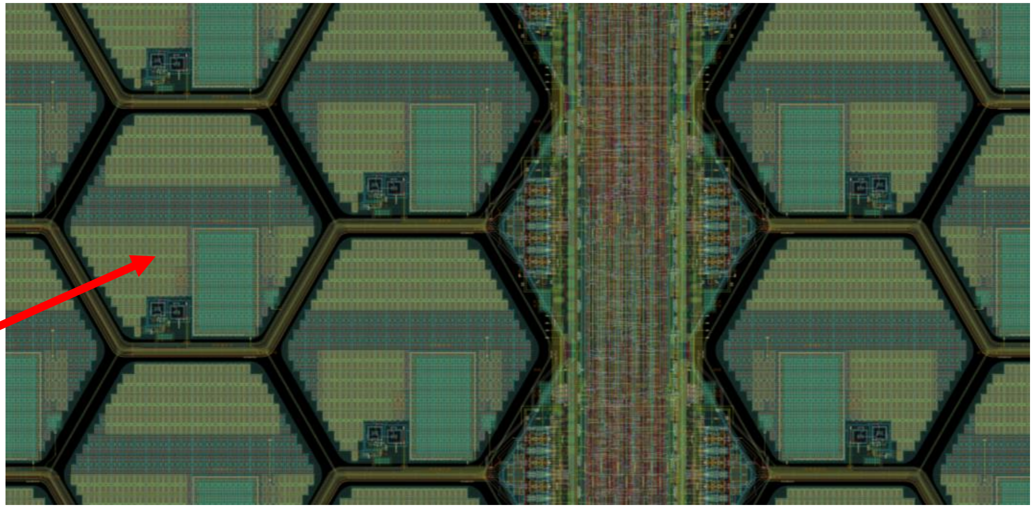
- Polysilicon capacitance to nwell is too high to realize a proper biasing: pmos bias is necessary.
- Pixel bias at Vcc to avoid body effect on pmos.

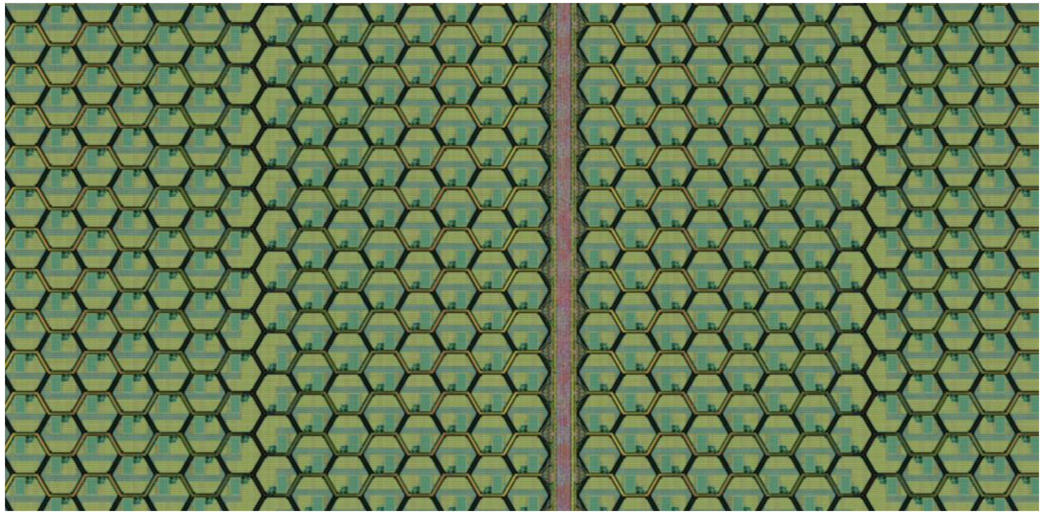




Monolithic design for 4D tracking

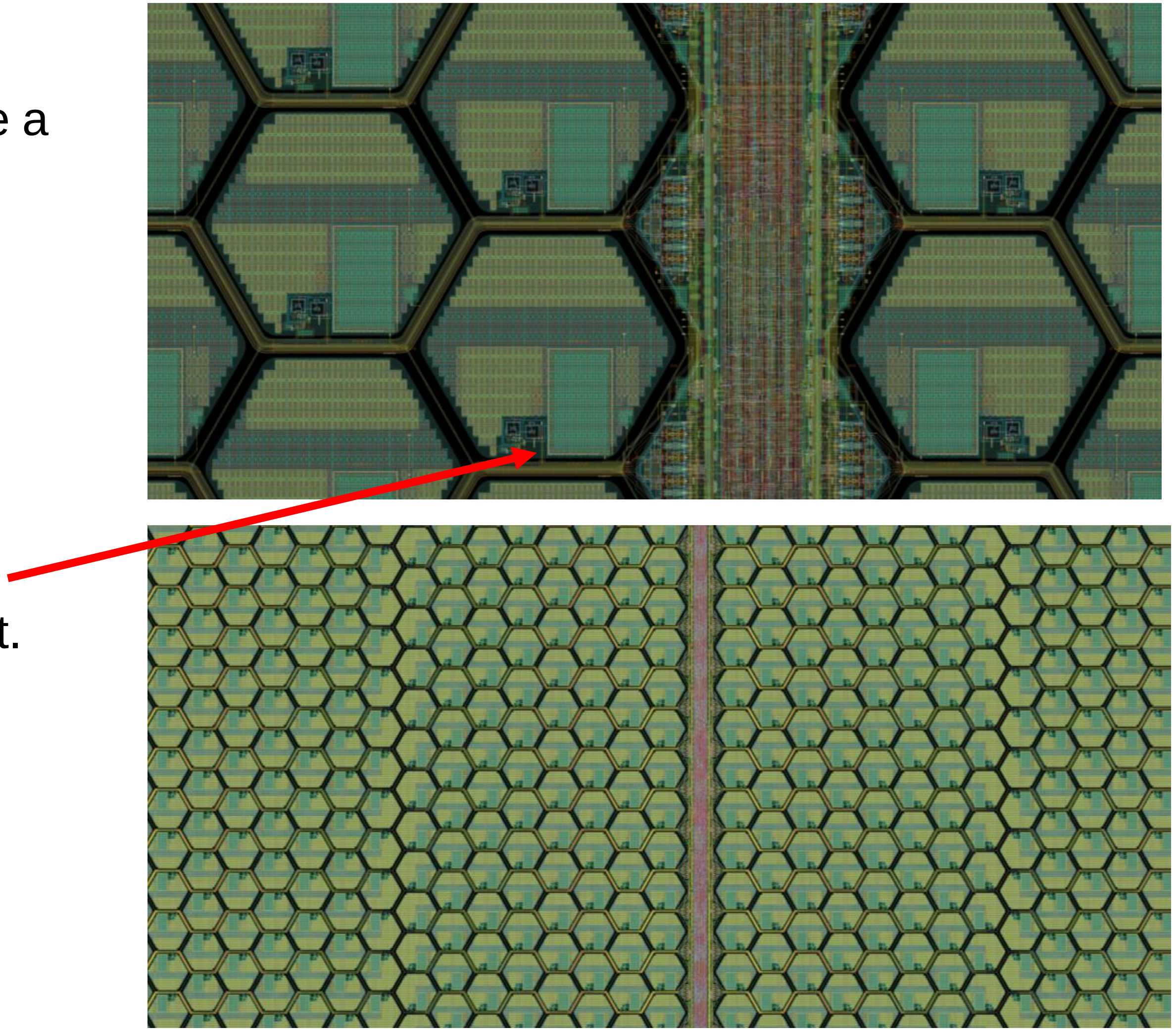
- Polysilicon capacitance to nwell is too high to realize a proper biasing: pmos bias is necessary.
- Pixel bias at Vcc to avoid body effect on pmos.
- Capacitive coupling using a matrix of large area pmos distributed in the pixel.





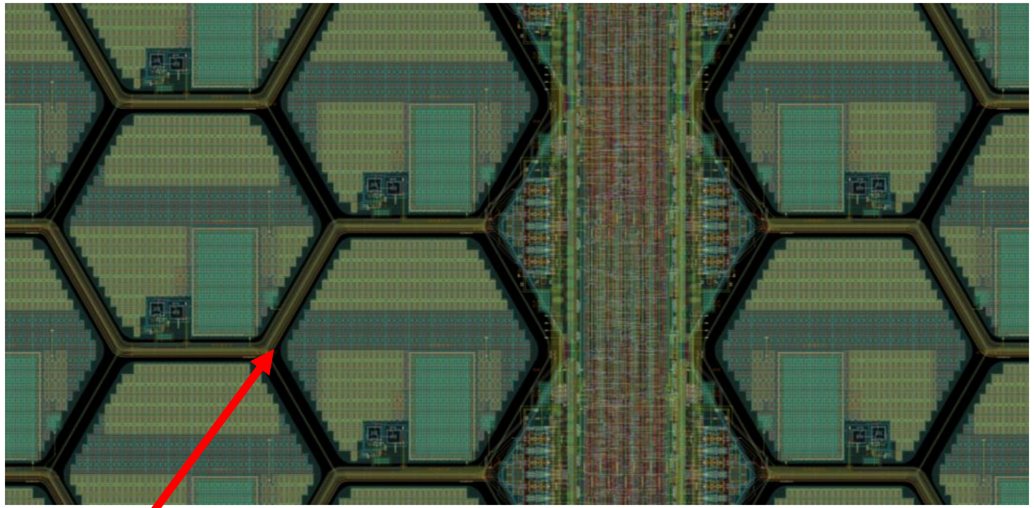
Monolithic design for 4D tracking

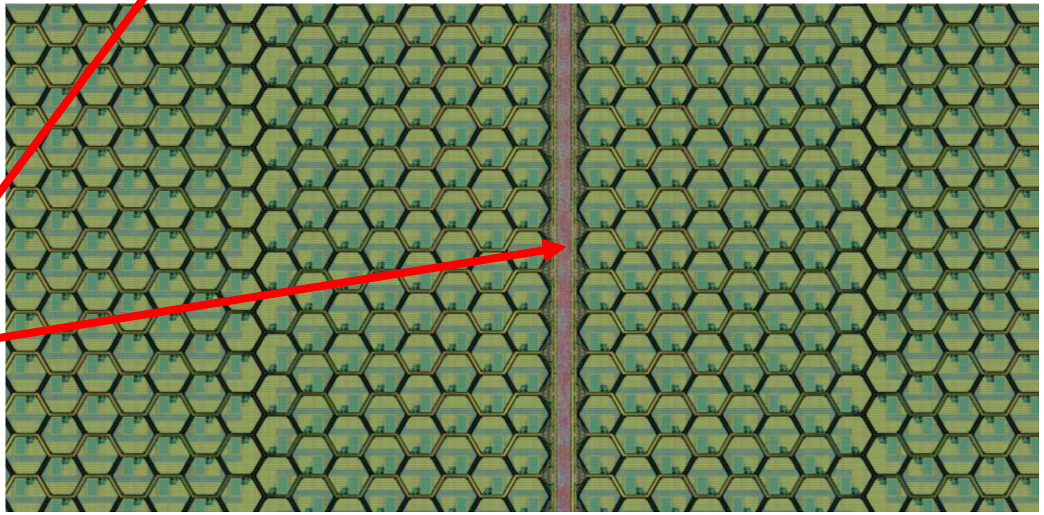
- Polysilicon capacitance to nwell is too high to realize a proper biasing: pmos bias is necessary.
- Pixel bias at Vcc to avoid body effect on pmos.
- Capacitive coupling using a matrix of large area pmos distributed in the pixel.
- Nmos are preferred in sensitive nodes, to avoid unnecessary parasitic capacitance towards the input.



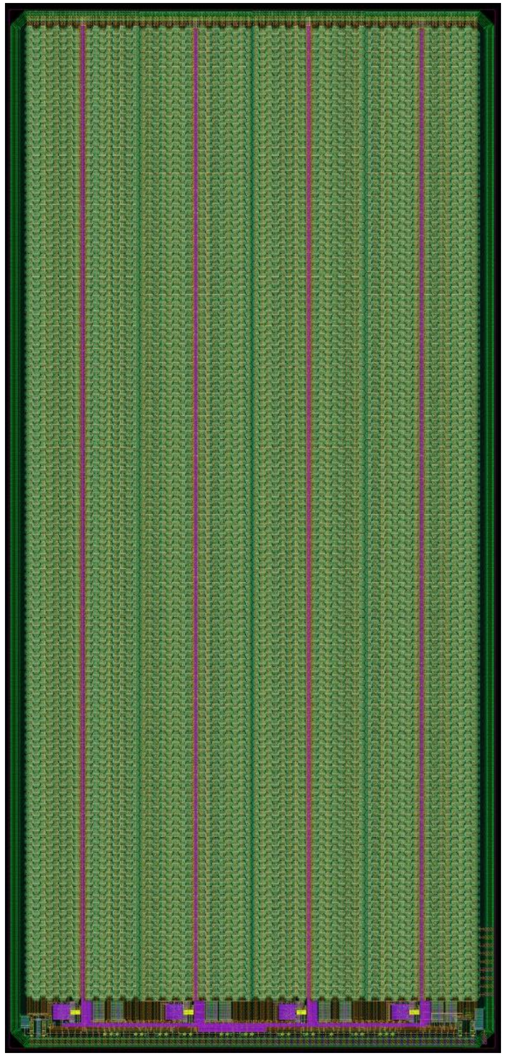
Monolithic design for 4D tracking

- Polysilicon capacitance to nwell is too high to realize a proper biasing: pmos bias is necessary.
- Pixel bias at Vcc to avoid body effect on pmos.
- Capacitive coupling using a matrix of large area pmos distributed in the pixel.
- Nmos are preferred in sensitive nodes, to avoid unnecessary parasitic capacitance towards the input.
- Signal routing after amplification stage requires shielded bus to avoid cross-talk to pixels.
- Digital electronics in separate well.



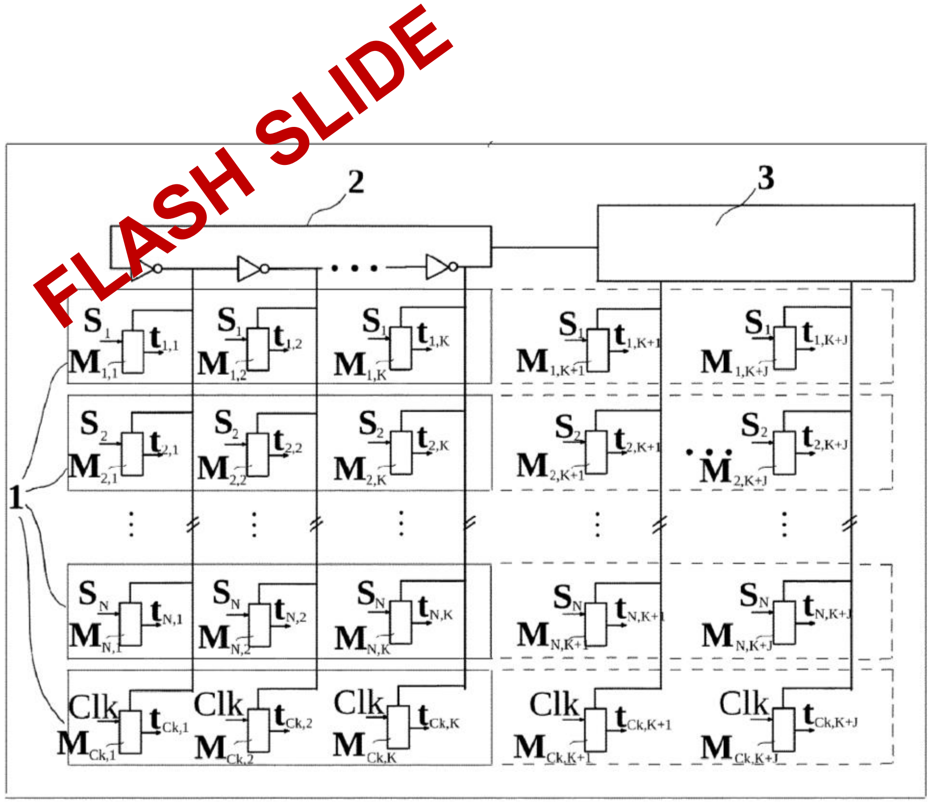


Pre-production ASIC



- Large area, fully functional prototype (7.5 × 15 mm^2).
- Two alternative test layouts with 3 columns.
- Submitted July 2021.

A self calibrating, low-power TDC



- 16 channels, each made by three sets of latches (1) connected to the same ring oscillator (2) to measure TOA and TOT of the signal.
- 1 calibration channel is used to measure the period of the ring oscillator on an event-by-event basis (UniGe patent).
- Linear Feedback Shift Registers (3) are used to extend the dynamic range of the measurements / also to store and trasnfer data.
- The large load on the Ring Oscillator may reduce its speed: a chain of buffers is connected to maintain a high oscillation frequency.
- The Ring Oscillator is always running, to increase its stability, while the buffers can be activated on demand, to reduce the power consumption.

https://worldwide.espacenet.com/patent/search?q=pn%3DEP3591477A1

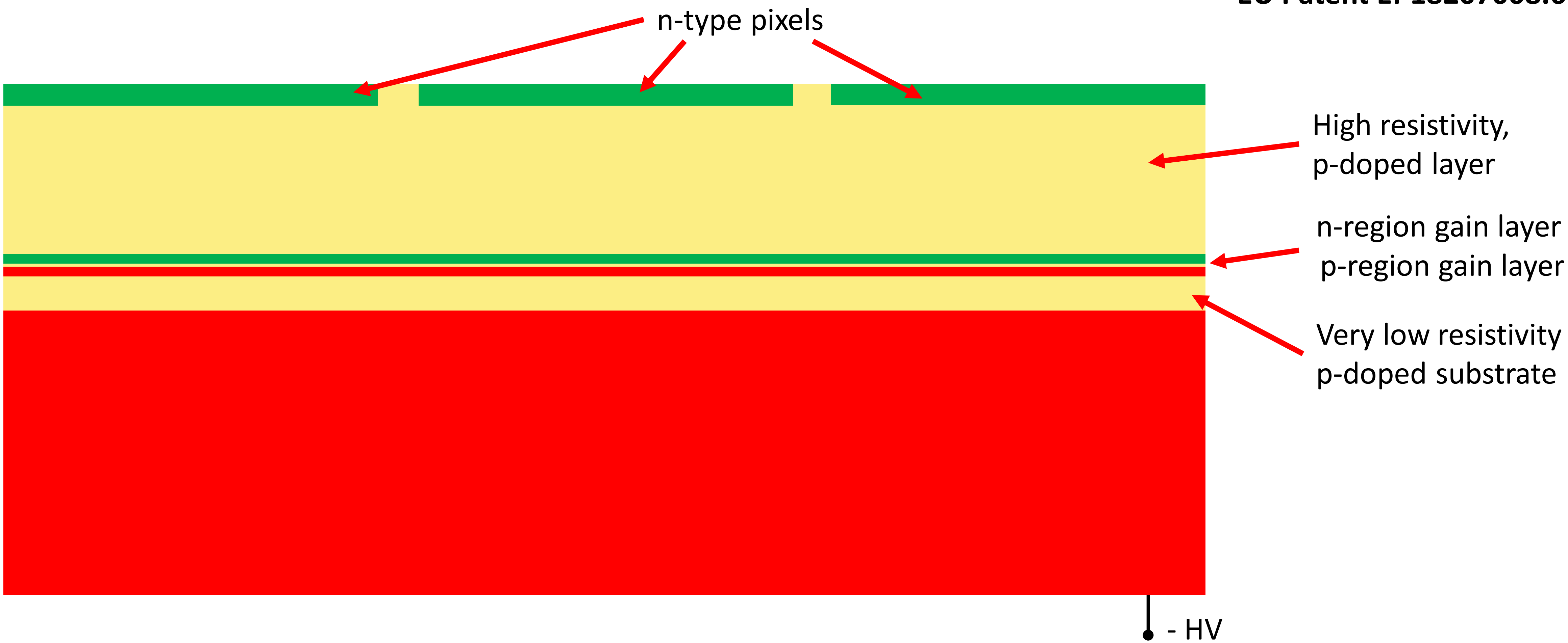
Summary

1. SiGe HBTs for fast, low power timing measurement.
2. SiGe BiCMOS technologies.
3. R&D at the University of Geneva.
4. The FASER pre-shower detector.
5. **The path toward picosecond time resolution.**

PicoAD: The PicoSecond Avalanche detector

- **Multi-Junction, pixelated avalanche detector.**

EU Patent EP18207008.6



PicoAD: The PicoSecond Avalanche detector

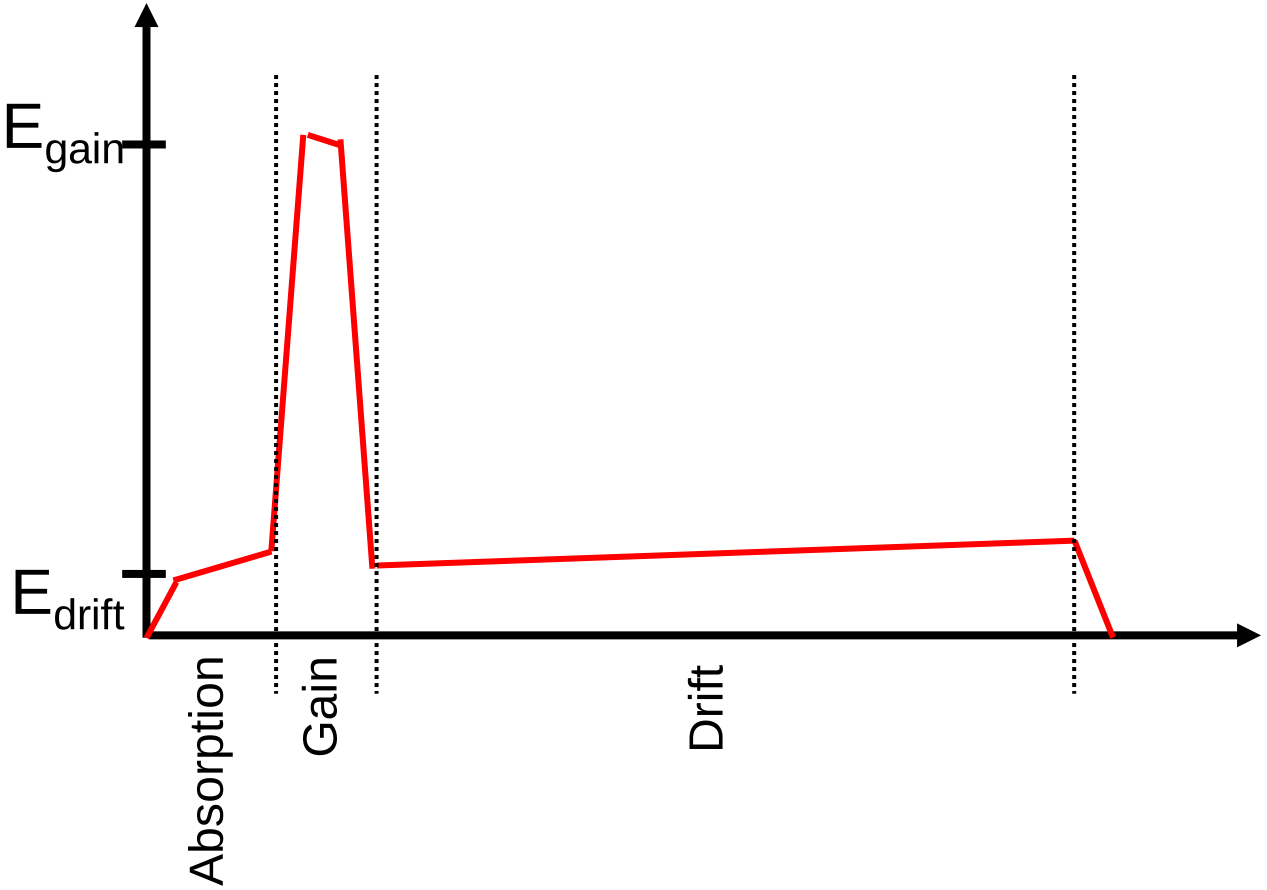
- **Multi-Junction, pixelated avalanche detector.**

EU Patent EP18207008.6

PicoAD: The PicoSecond Avalanche detector

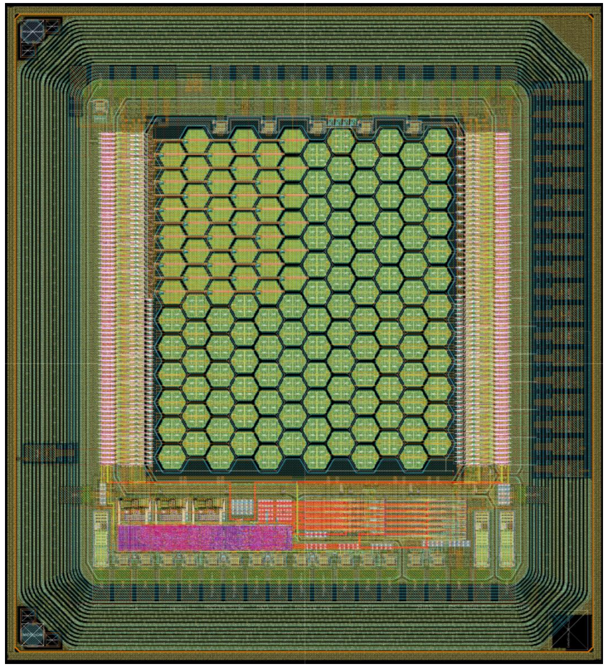
- **Multi-Junction, pixelated avalanche detector.**

EU Patent EP18207008.6



- The introduction of fully-depleted multi-pn junctions allows to **engineer the electric field**.
- New device with unique timing and reliability performance.
- Gain with 100% fill-factor.
- Geant4 + Cadence simulations estimate ~**2ps time resolution** contribution from the sensor.
- Requires low-noise, ultra fast electronics to be fully exploited.

First PicoAD prototypes



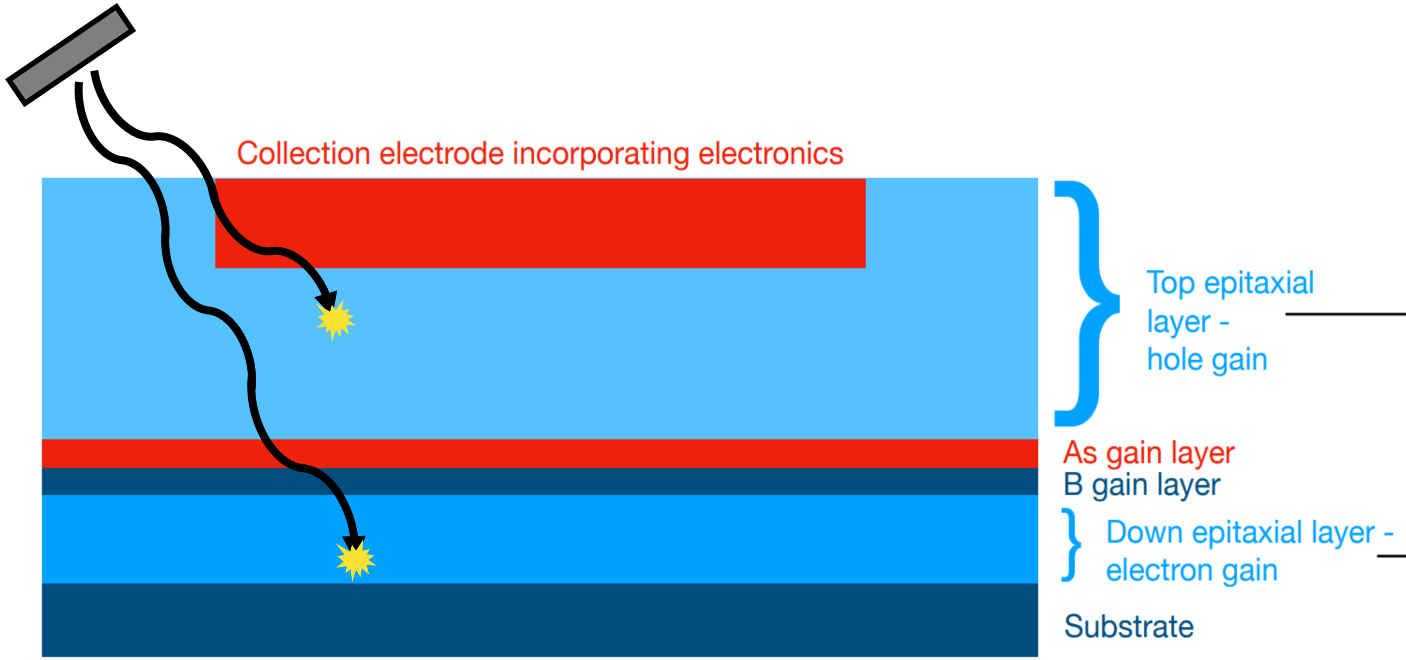
- Integrated in a special wafer for the ATTRACT prototype.
- Process design in collaboration with IHP.
- First prototype tested in lab and at SPS beam line.

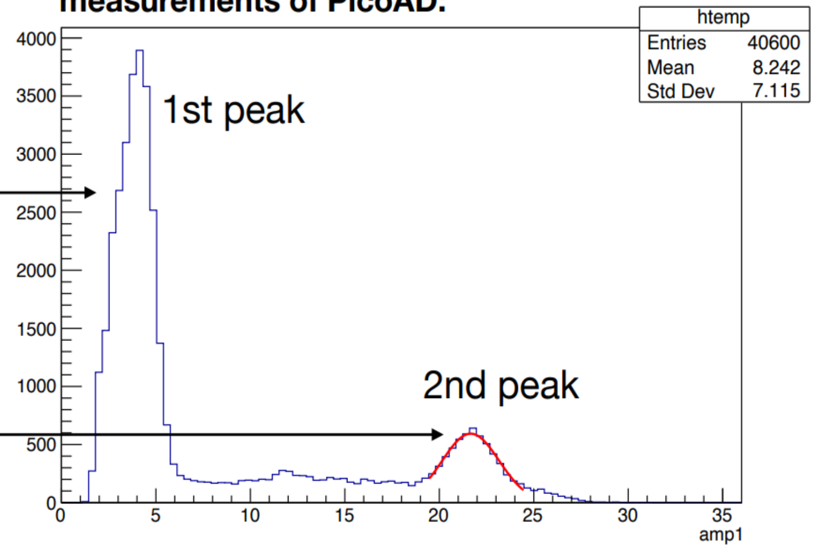
CAVEAT:

- Not ideal manufacturing process, it was not possible to saturate the charge drift velocity.

PicoAD: First prototype test with Fe-55 source

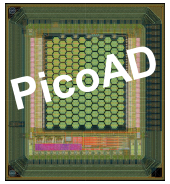
Fe-55 X-ray source: point-like charge deposition inside the sensor



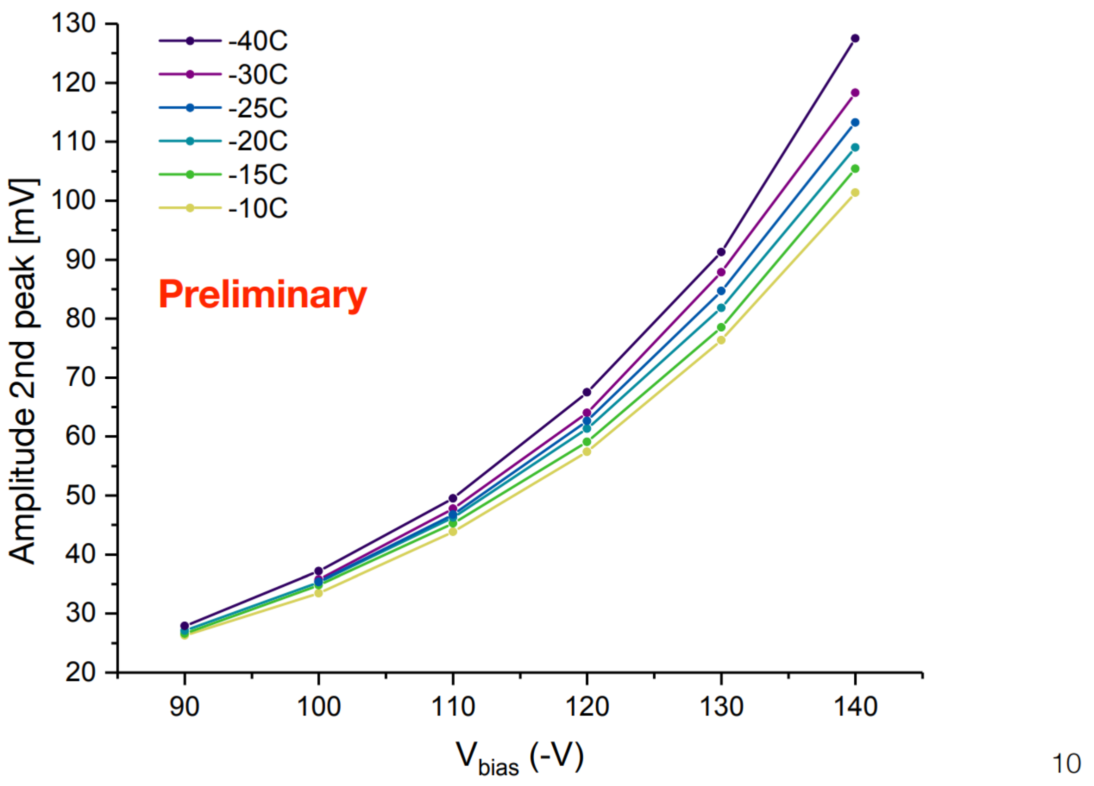


Gain = 2nd peak / 1st peak before hole gain

PicoAD: First prototype test with Fe-55 source



Measurements of sensor gain using 55-iron source in climate chamber:



<u>Measured sensor gain depends on temperature:</u>

Higher gain for lower temperatures due to change in impact ionisation coefficient α:

$$G \propto e^{\alpha(E,T)\cdot d} \quad with \quad \alpha(E,T) \propto e^{-(a+b\cdot T)/E}$$

G = Gain, d=distance, E=electric field

Significant gain of > 20

Note: challenging to determine due to convolution of sensor and frontend effects at lower temperatures

—> Proof of novel picoAD concept

Preliminary results from beam test are promising

MONOLITH Project: Targets

5-year ERC Advanced project at University of Geneva. PI: Giuseppe Iacobucci.

- Develop the PicoAD technology for ionizing radiation.
- Develop picosecond electronics for large area chips (Front-End, TDC, Logic).
- Assess radiation hardness of the PicoAD.
- Integrate the sensor in a Full Reticle detector for HEP experiments.

MONOLITH Project: Milestones

July 2020:	Starting date. ✓
December 2020:	Optimized front-end and wafers for picosecond timing. ✓
December 2021:	Low-power, picosecond TDC. ✓
December 2022:	Small prototype integration.
June 2024:	Full-reticle chip.

CONCLUSIONS

- SiGe BiCMOS proved the feasibility of a monolithic integration of silicon pixel sensors for ionizing radiation for **large area detectors with state-of-the-art space-time resolution**.
- Previous prototypes showed **38 ps time resolution without avalanche gain**.
- A **full-reticle chip will be produced** for the new FASER pre-shower, targeting 100 ps time resolution.
- The development of a **4D detector with picosecond time resolution** is in progress with the MONOLITH project. State-of-the-art space and time resolution are possible in a single device.

Publications and patents

Articles:

- Small-area pixels power consumption: arXiv:2005.14161 - Accepted for publication on JINST
- Hexagonal small-area pixels: JINST 14 (2019) P11008, https://doi.org/10.1088/1748-0221/14/11/P11008
- TT-PET demonstrator chip testbeam: JINST 14 (2019) P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
- TT-PET demonstrator chip design: JINST 14 (2019) P07013, https://doi.org/10.1088/1748-0221/14/07/P07013
- First TT-PET prototype: JINST 13 (2017) P02015, https://doi.org/10.1088/1748-0221/13/04/P04015
- Proof-of-concept amplifier: JINST 11 (2016) P03011, https://doi.org/10.1088/1748-0221/11/03/P03011

- TT-PET engineering: arxiv:1812.00788
- TT-PET simulation & performance: arxiv:1811.12381

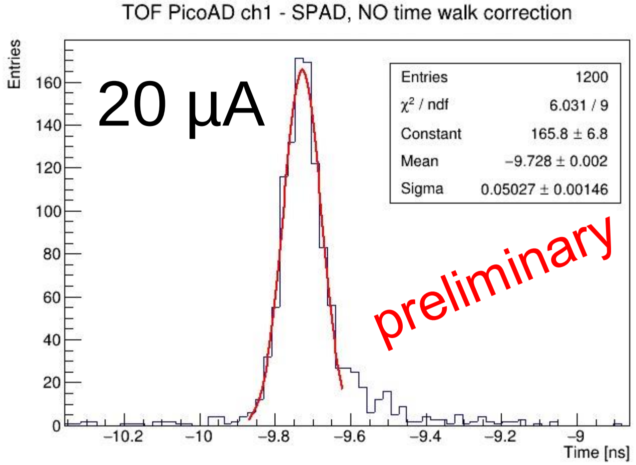
Patents:

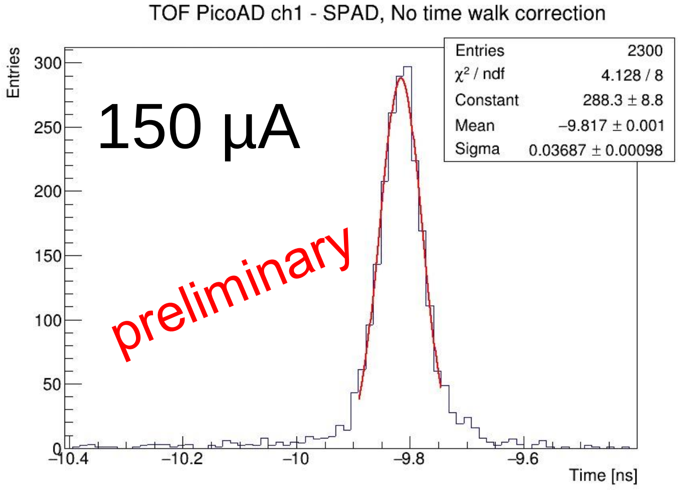
- PLL-less TDC & synchronization System: EU Patent EP18181123.3
- Picosecond Avalanche Detector: EU Patent EP18207008.6

Extra Material

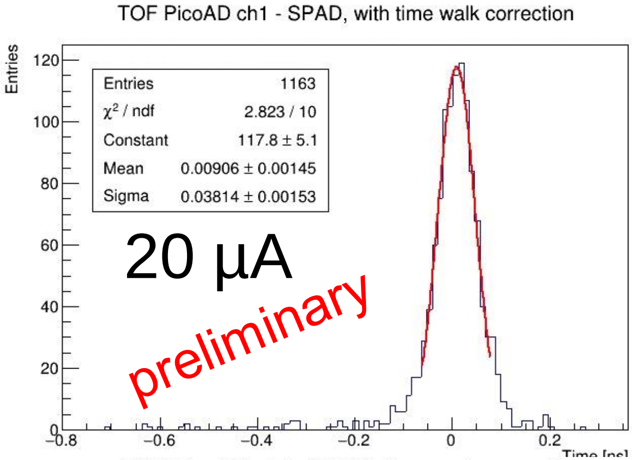
PicoAD: Preliminary results from beam test

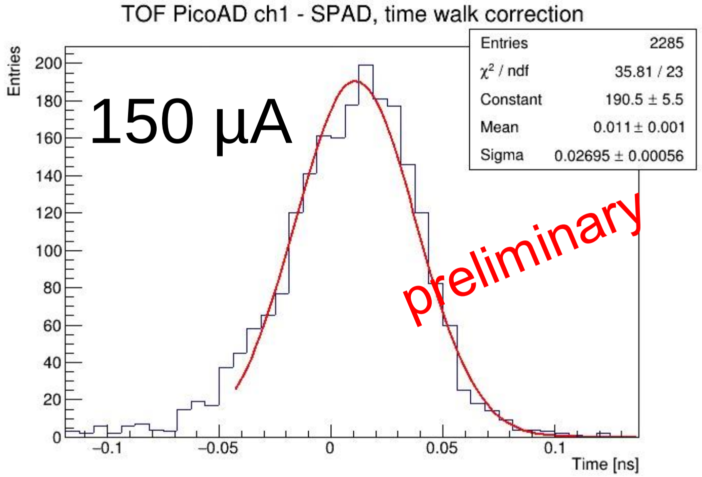
No time walk correction





With time walk correction

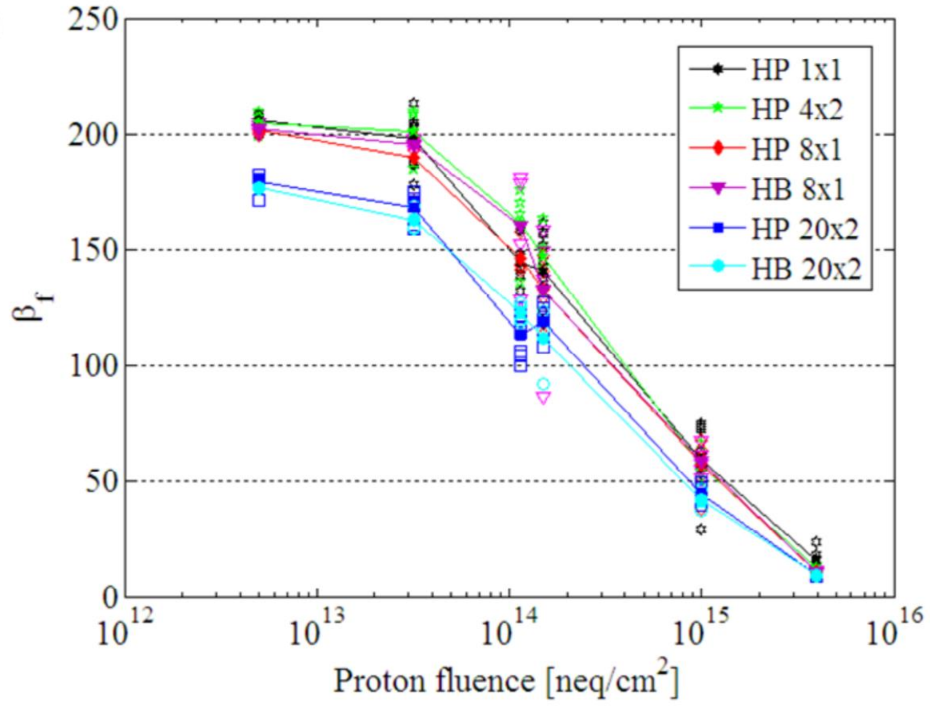




- A time resolution of 50ps is achieved at **very low power** consumption and **without time walk correction**.
- Integrates **state-of-the-art time and space resolution** in a single device.

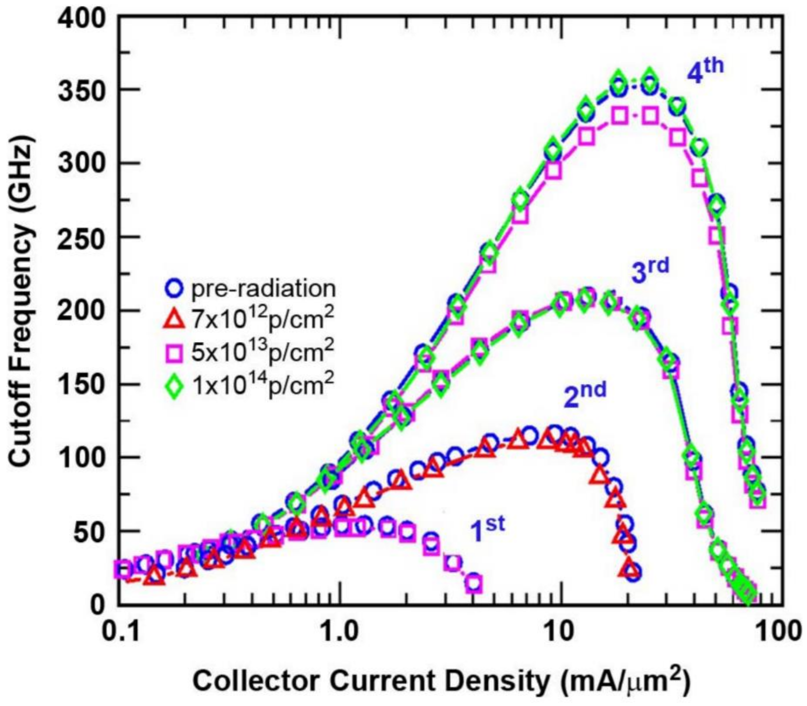
Radiation hardness of standard commercial HBTs

DC characteristics



S. Díez et al, IEEE Nuclear Science Symposuim & Medical Imaging Conference, Knoxville, TN, 2010, pp. 587-593, doi: 10.1109/NSSMIC.2010.5873828.

AC characteristics



From: J.D. Cressler, IEEE transactions on nuclear science, vol. 60, n. 3 (2013)

No studies available on AC characteristics and noise above 10^{14} p/cm^2