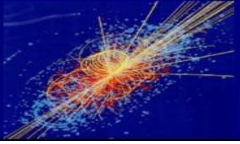
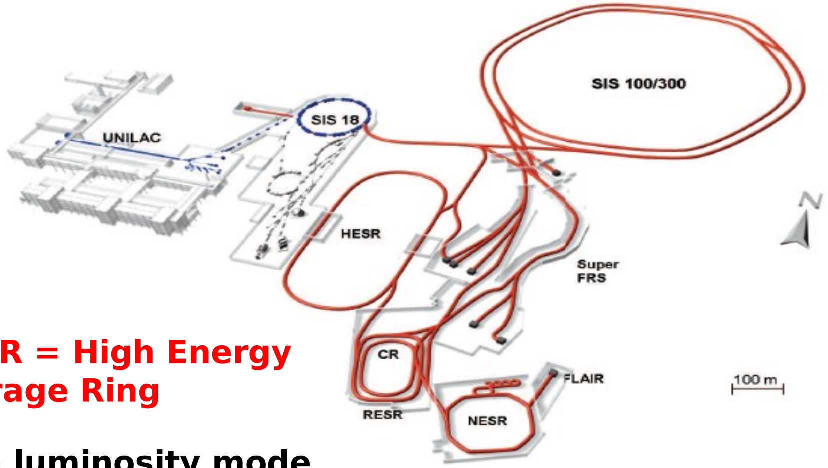


Front-End Electronics developments for the Microvertex detector of the PANDA Experiments at FAIR

D. Calvo[1], T. Kugathasan[1,2], P. De Remigis[1], G.Mazza[1],
*M. Mignone[1], **A. Rivetti[1]**, S. Salerno[1], T. Stockmanns[3] and R. Wheadon[1]*

1 INFN, Sezione di Torino, Italy
2 Università di Torino, Dip. di Fisica Sperimentale, Italy
3 Forschungszentrum Jülich, Germany

PANDA @ FAIR



HESR = High Energy Storage Ring

High luminosity mode

- **Luminosity = 2×10^{32} cm^{-2}s^{-1}**
- **$\delta p/p \sim 10^{-4}$ (stochastic cooling)**

High resolution mode

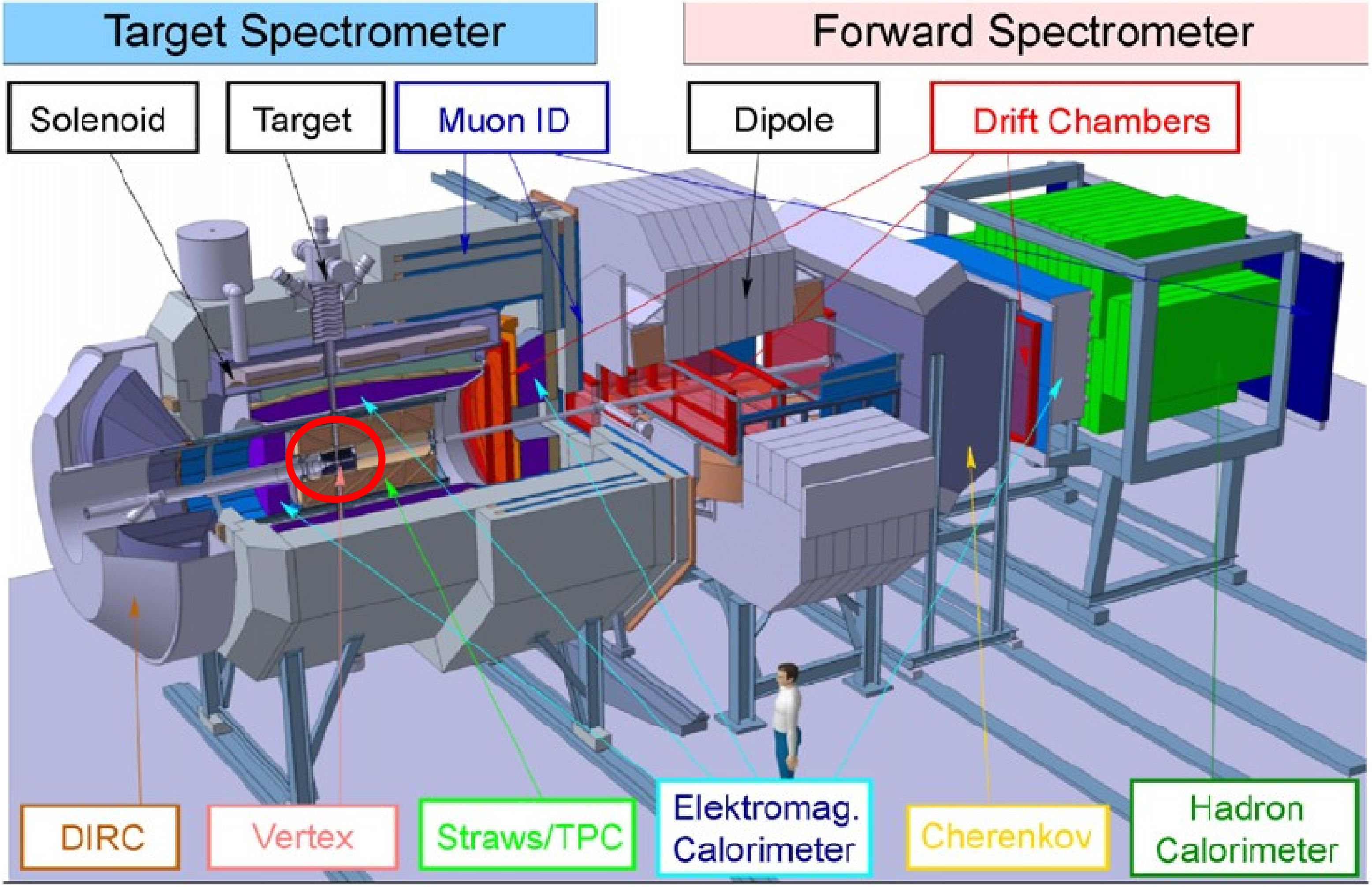
- **$\delta p/p \sim 10^{-5}$ (el. cooling < 8 GeV/c)**
- **Luminosity = 10^{31} cm^{-2}s^{-1}**

- **FAIR: Facility for Antiproton and Ion Research.**
- **PANDA: Pbar ANnihilation at Darmstadt. Multipurpose experiment:**

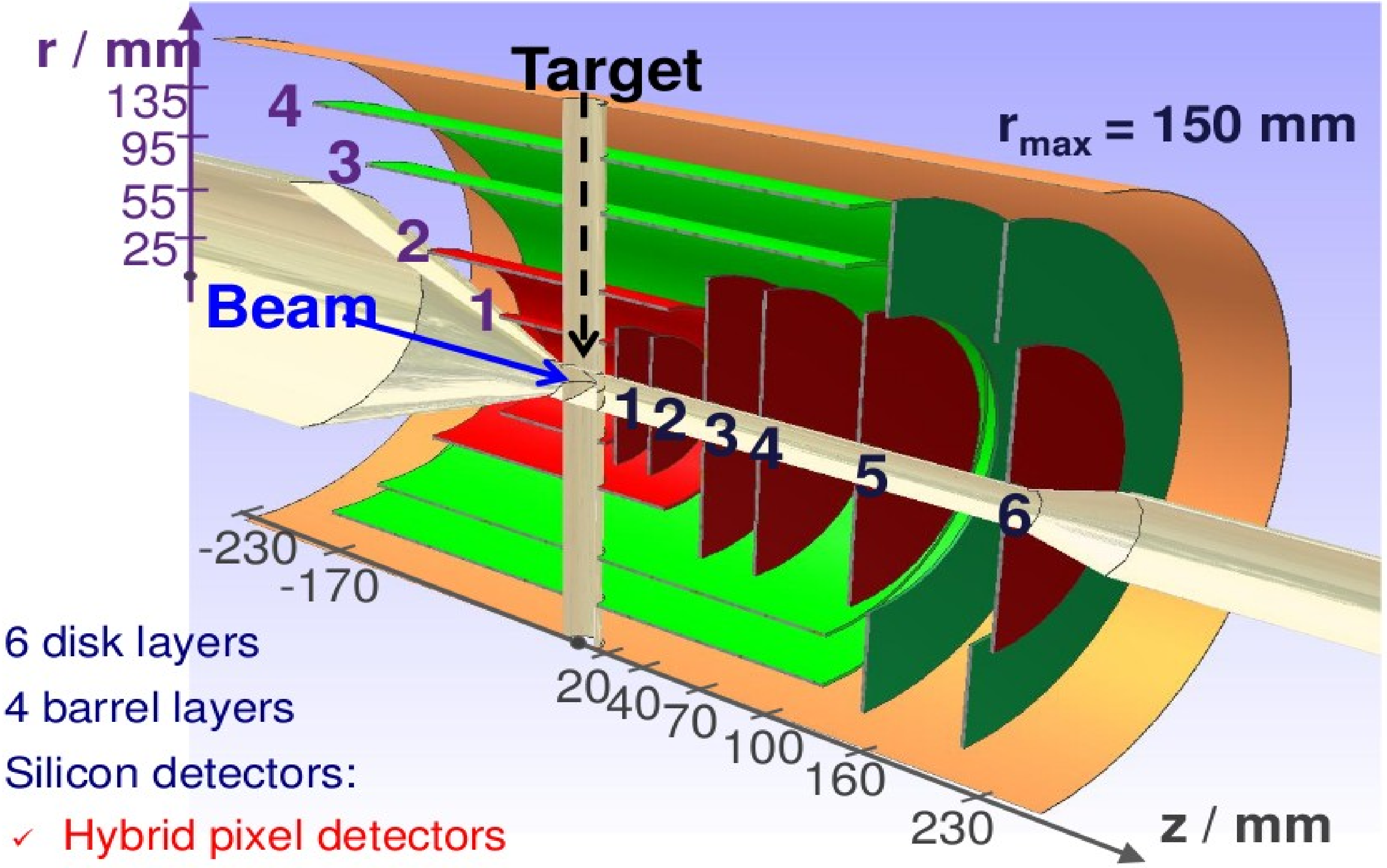
- **charmonium spectroscopy**
- **glueballs and hybrids**
- **hadrons in nuclear matter**
- **open charm production**
- **γ-ray spectroscopy of hypernuclei**

TRIGGERLESS READOUT

The PANDA apparatus



The Micro-Vertex Detector



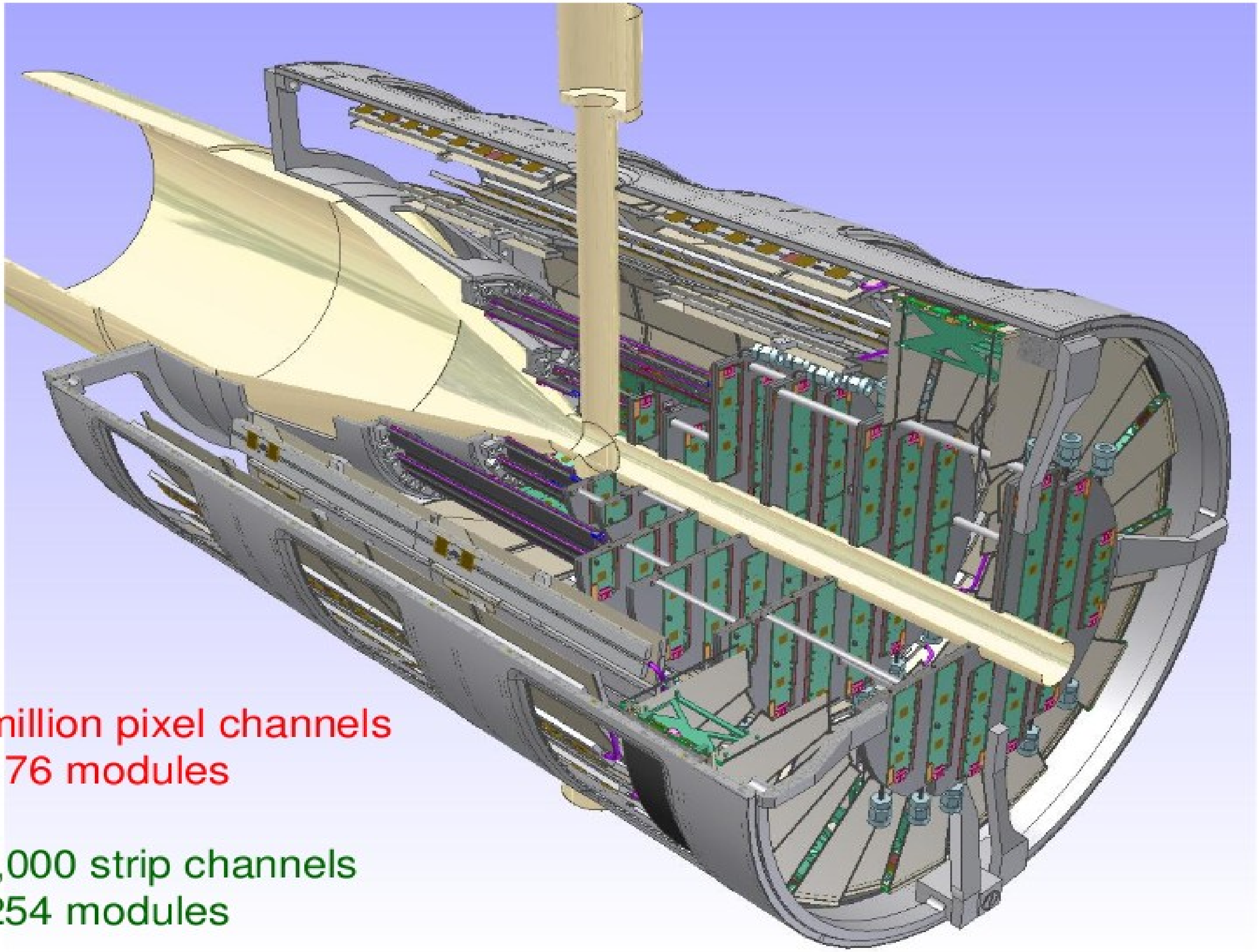
6 disk layers

4 barrel layers

Silicon detectors:

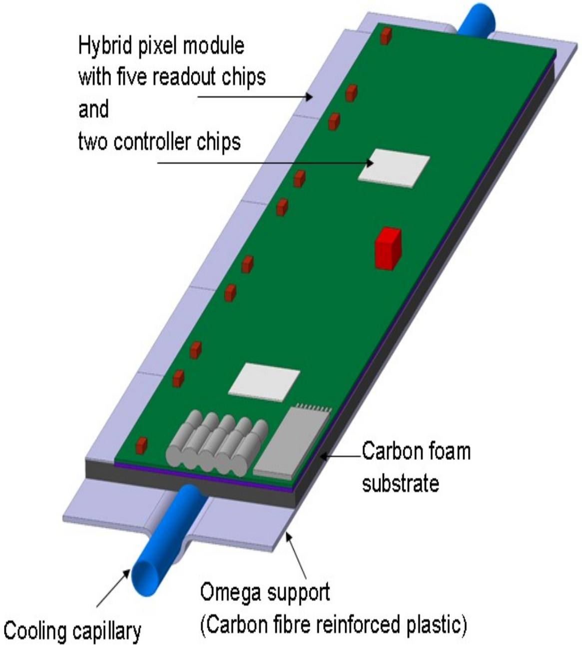
- ✓ Hybrid pixel detectors
- ✓ Double-sided microstrip detectors

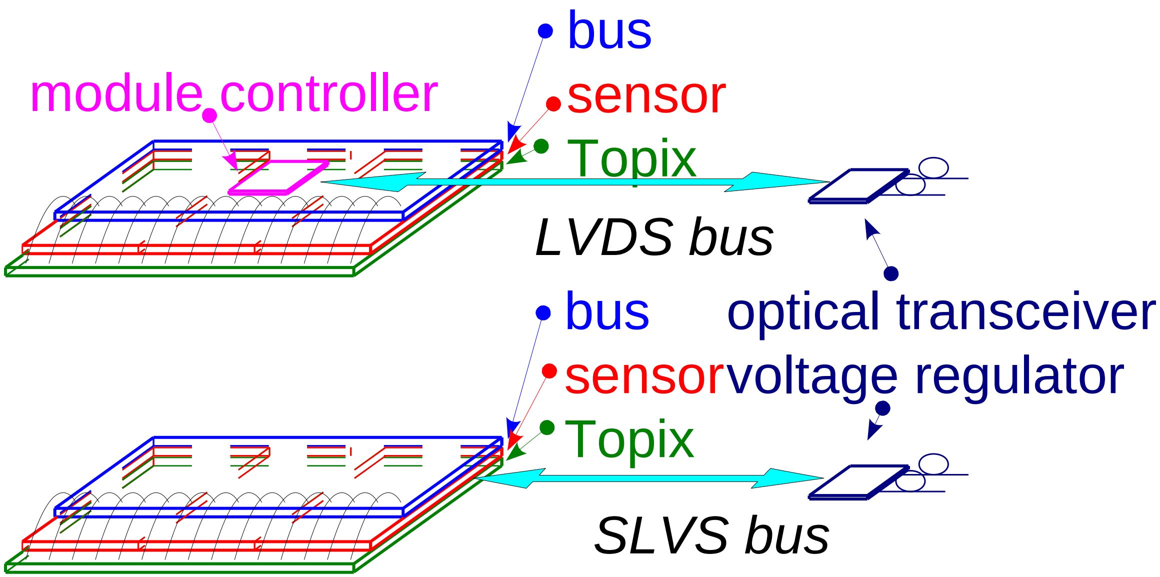
The Micro-Vertex Detector



- 10 million pixel channels on 176 modules
- 200,000 strip channels on 254 modules

The hybrid pixel detector





module controller

- bus
- sensor
- Topix

LVDS bus

optical transceiver

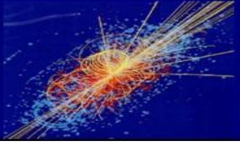
- bus
- sensor
- Topix

voltage regulator

SLVS bus

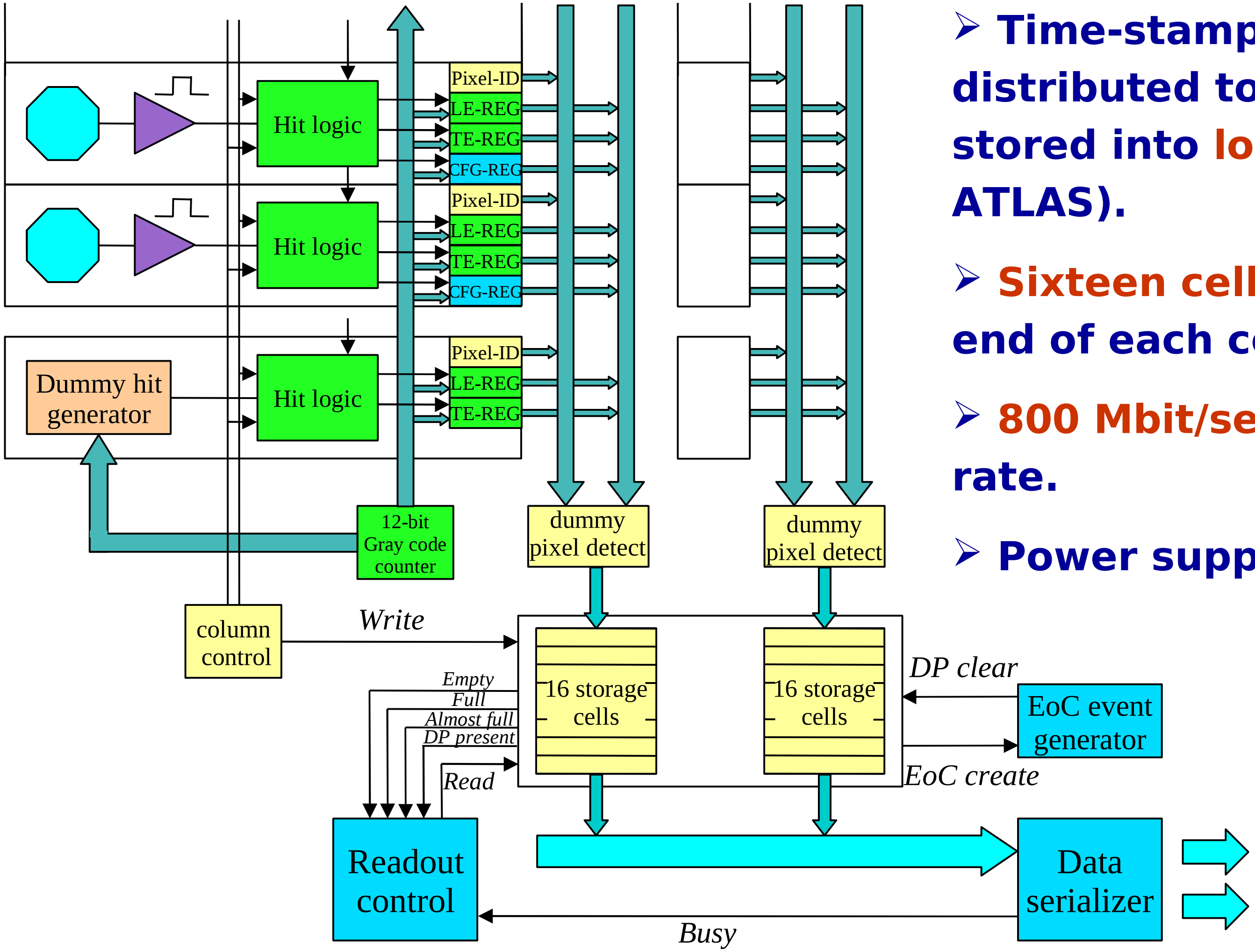
- Baseline solution based on well-proven technology (hybrid pixel with bump bonding)
- Custom development only where strictly needed (e.g. front-end chip)

Specs for the pixel detector



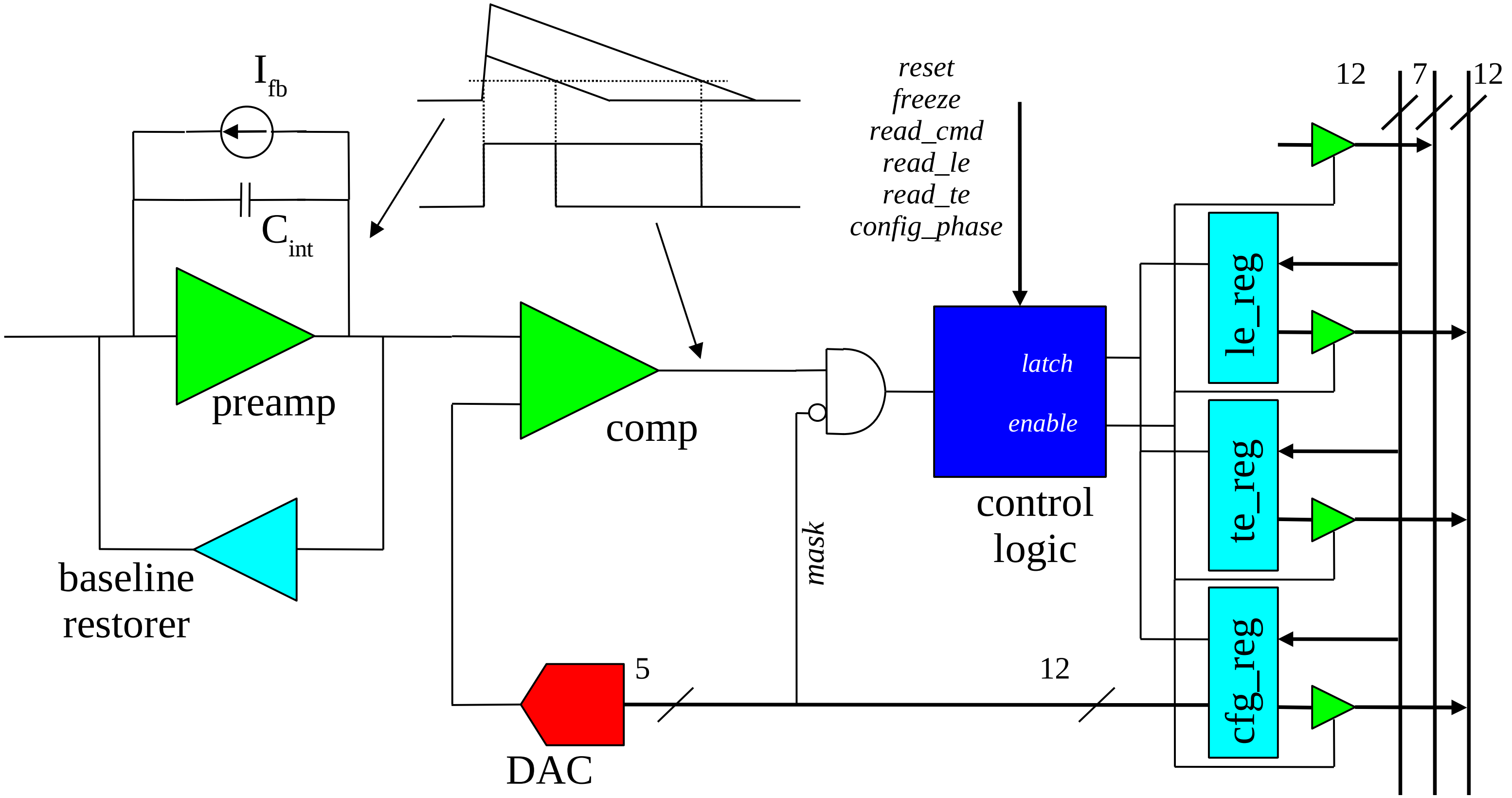
- Pixel cell specs:
  - Pixel size: 100 μm x 100 μm.
  - Noise level: < 200 e- rms.
  - Linear dynamic range: up to 50 fC.
  - Power consumption: < 20 μW.
  - Selectable input signal polarity.
  - Leakage insensitive up to 50 nA.
- ASIC specs:
  - Self triggering
  - Clock 160 MHz
  - Active area: O(1 cm^2)
  - Data rate: O(0.8 Gbit/sec.)
  - Radiation tolerance: LHC grade.
  - Simultaneous time stamping and charge measurement.
- No existing chip could match simultaneously all the PANDA requirements.
- Custom solution under investigation.
- Technology: CMOS 0.13 μm.

ASIC architecture

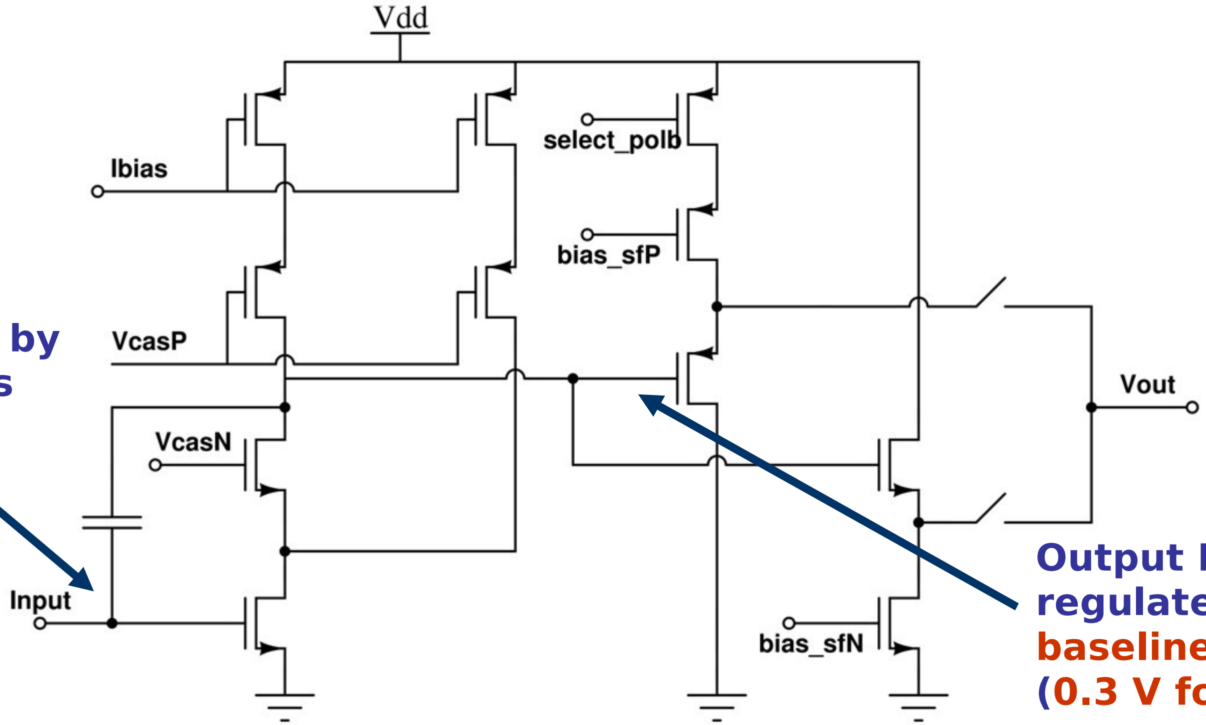


- **Time-stamp (Gray encoded) distributed to the pixels and stored into local registers (à la ATLAS).**
- **Sixteen cells deep-FIFO at the end of each column.**
- **800 Mbit/sec per cm^2 max data rate.**
- **Power supply: 1.2 V.**

Pixel cell architecture



Front-end amplifier

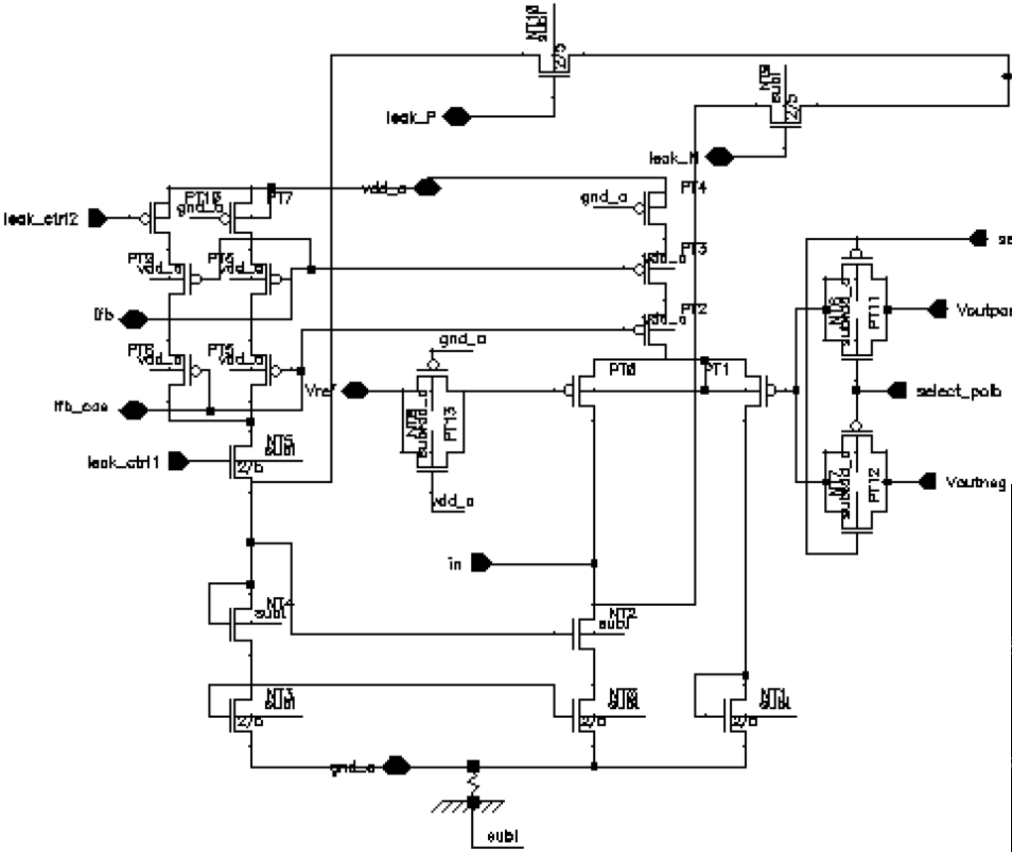


DC level fixed by transistor bias (0.3 V)

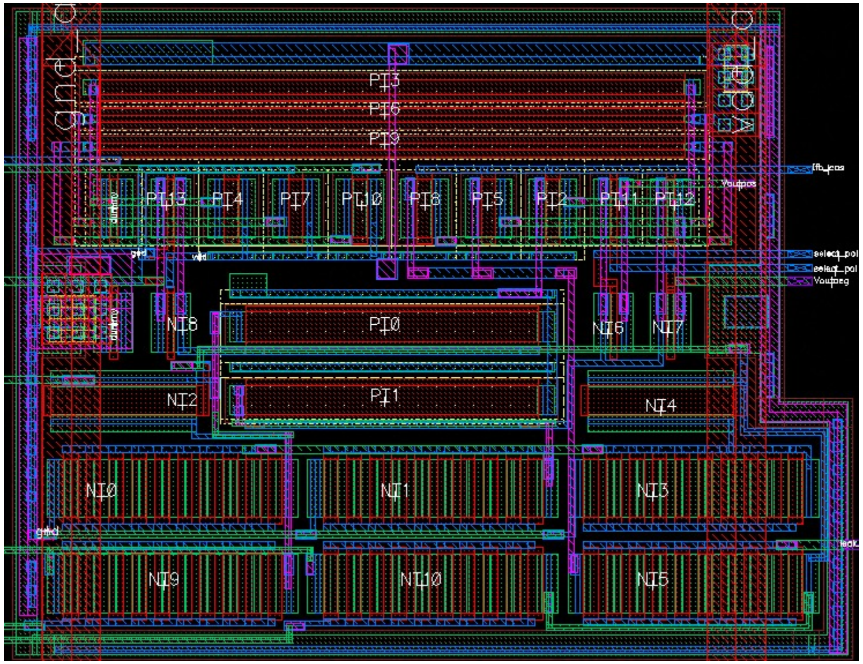
Output DC level regulated by the baseline restorer. (0.3 V for n-type sensor, 0.8 V for p-type)

- **Direct cascode with NMOS input transistor and split current source**
- **Triple well NFET input and cascode.**
- **Two selectable PMOS or NMOS output buffers.**
- **Current: 2μA in the input device, 1 μA in the source follower.**

Feed-back current switch

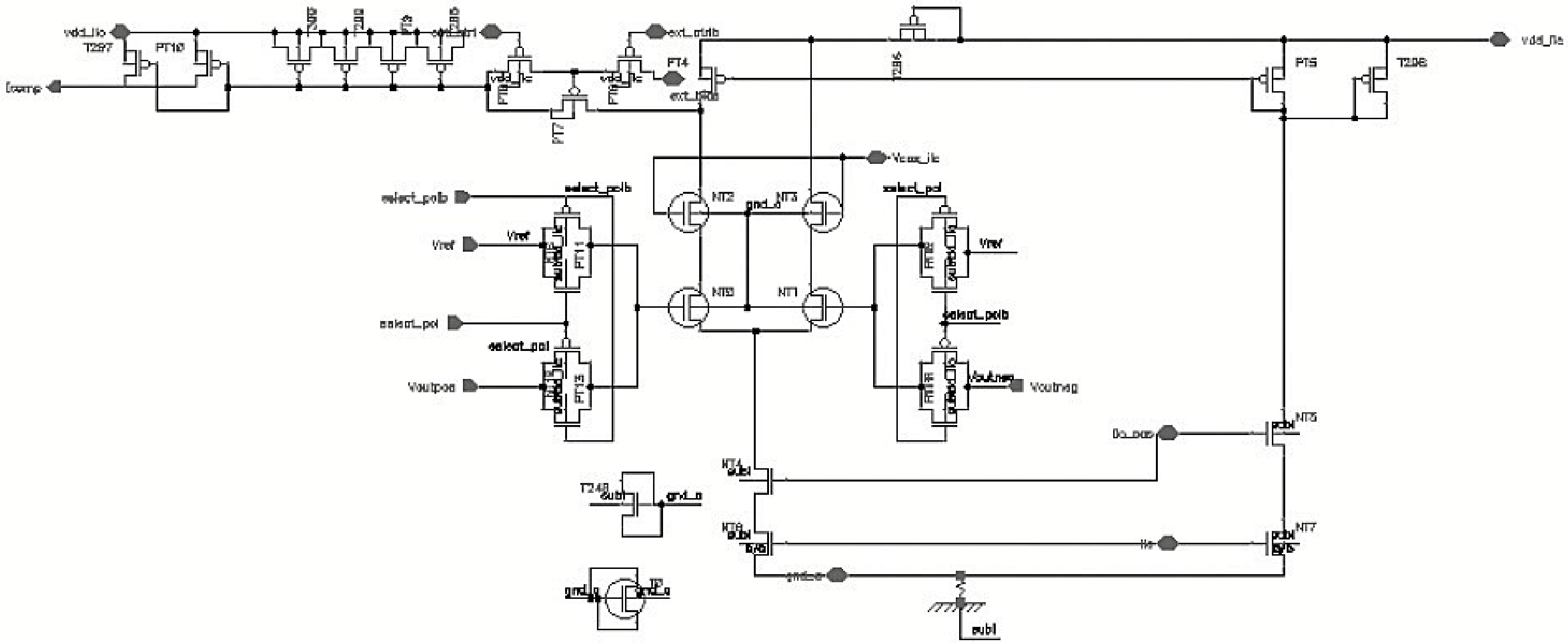


- **Differential current switch.**
- **At the equilibrium provides an equivalent 8MΩ feed-back resistor.**



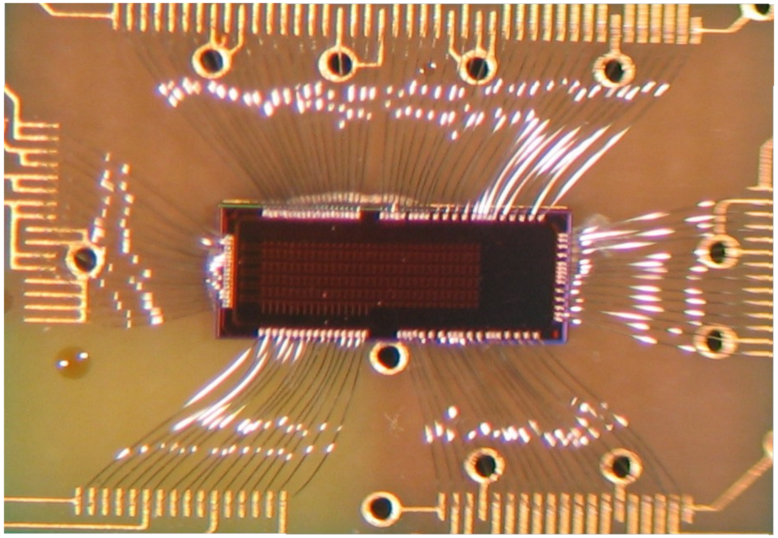
- **Issue: low-value of feed-back current (2.5nA to 10 nA) leads to long devices.**

Leakage compensation

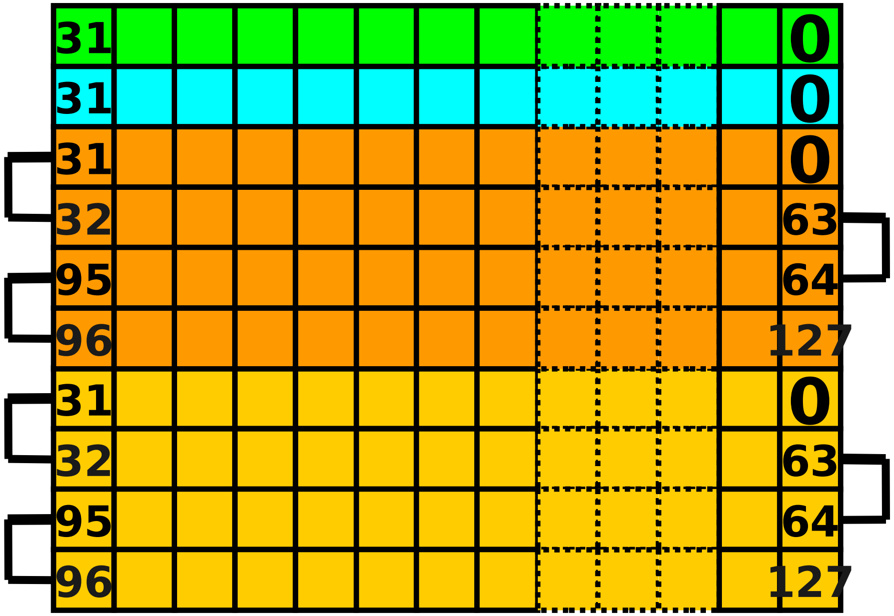


- ➢ **With large dynamic range ToT signals ca be very long (10-20 μs).**
- ➢ **Leakage compensation must be very narrowband, otherwise a non-linearity will result**
- ➢ **Need to implement compact filtering resistors with very high value.**

Chip prototype

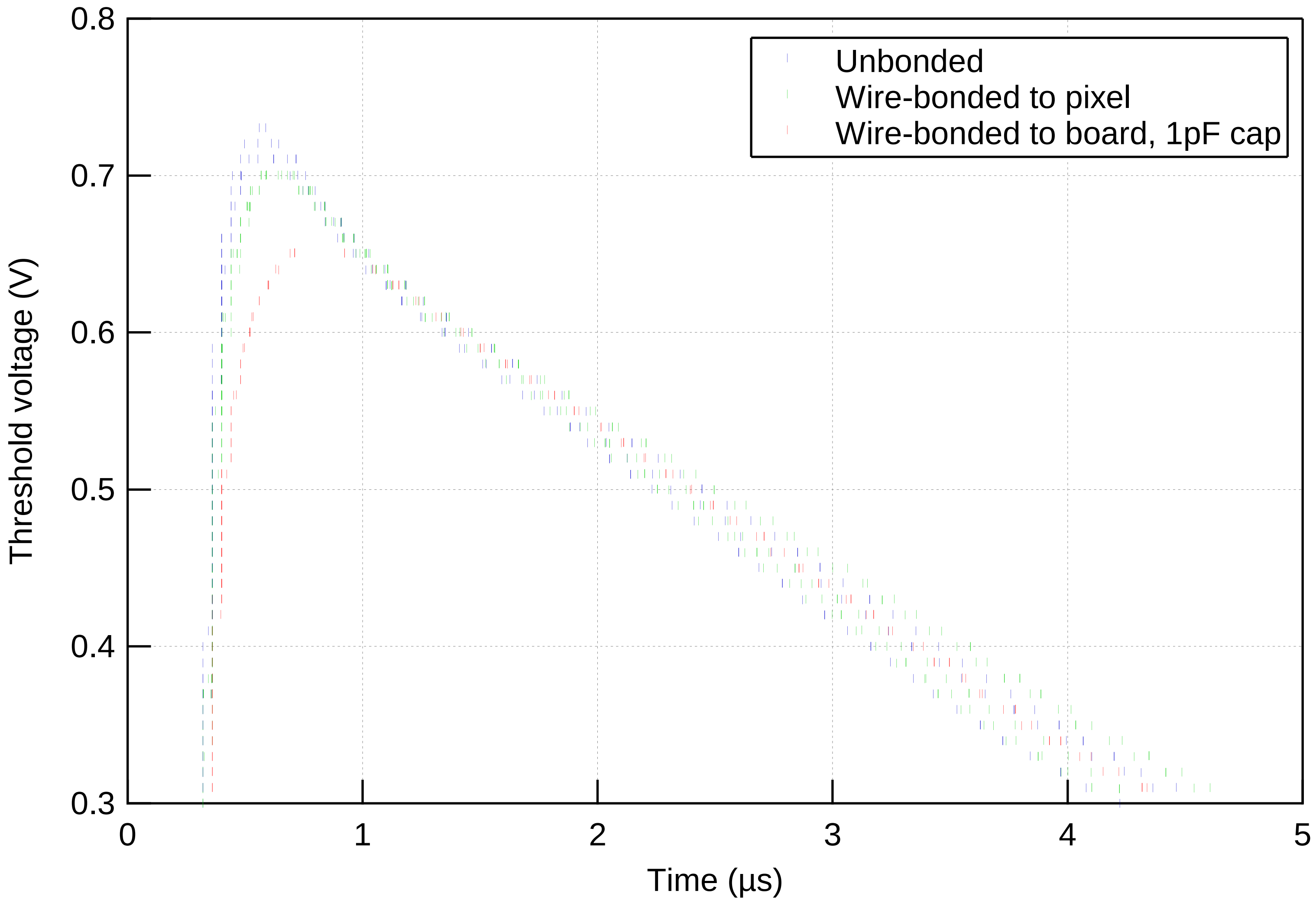


- Test chip produced in a MPW.
- Size: 5 mm x 2 mm.
- Column length: 12.8 mm.
- Column folding => full bus length.

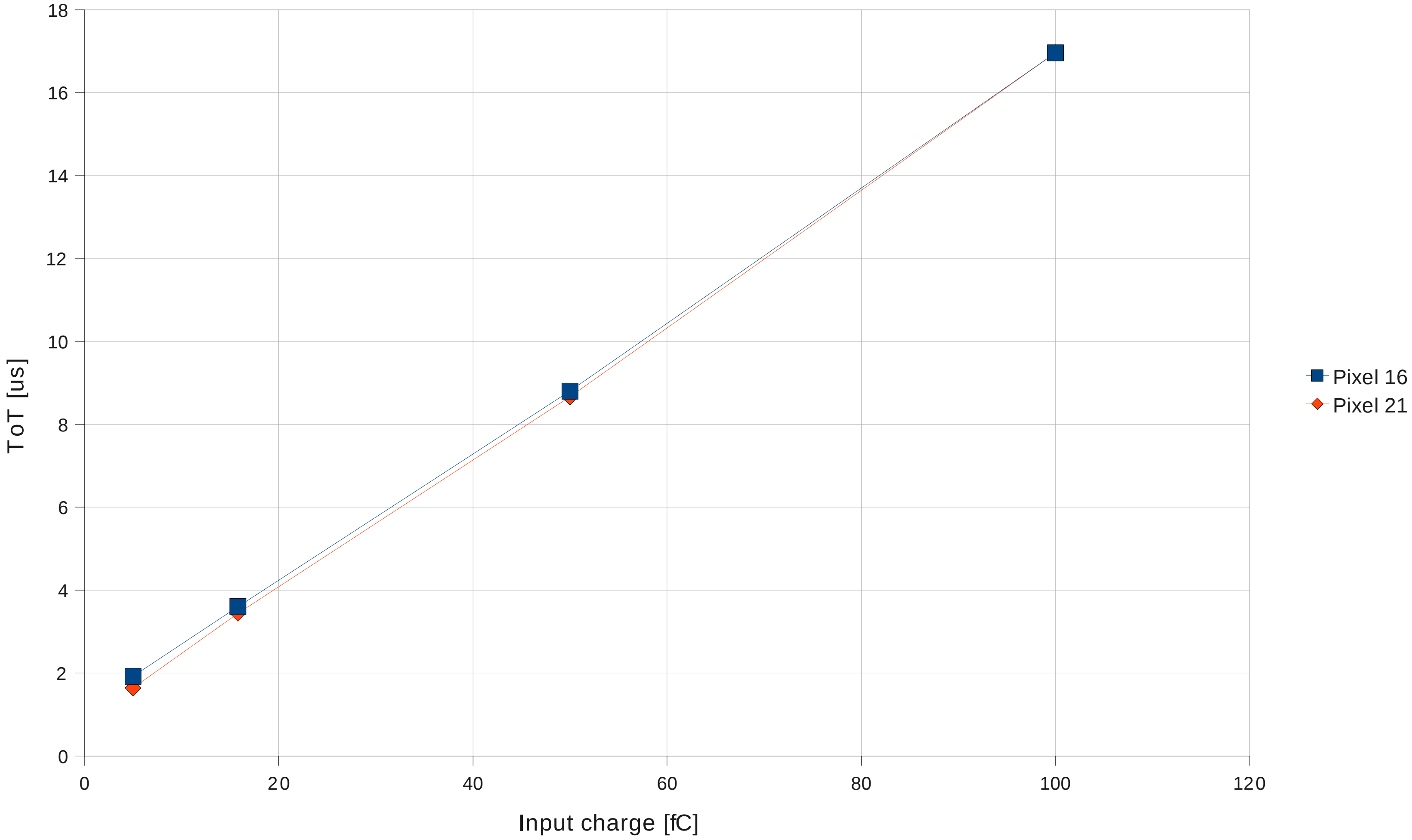


- Full pixel cell (analog and digital parts).
- Simplified end-of-column logic.
- Two folded columns with 128 pixels.
- Two short column with 32 pixels.
- Sixteen pixels with wire bonding pad.

Reconstructed pulse shape

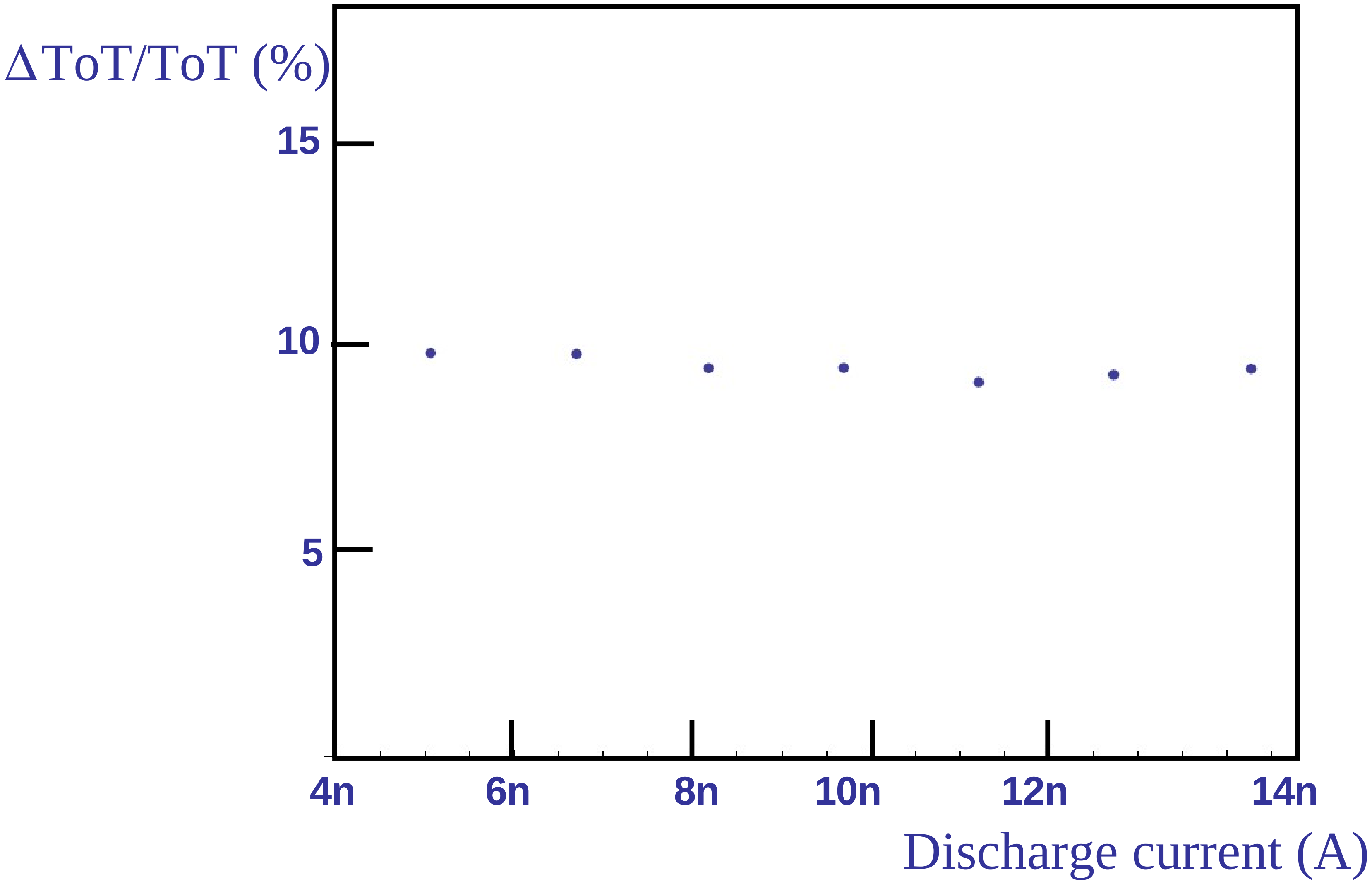


Linearity

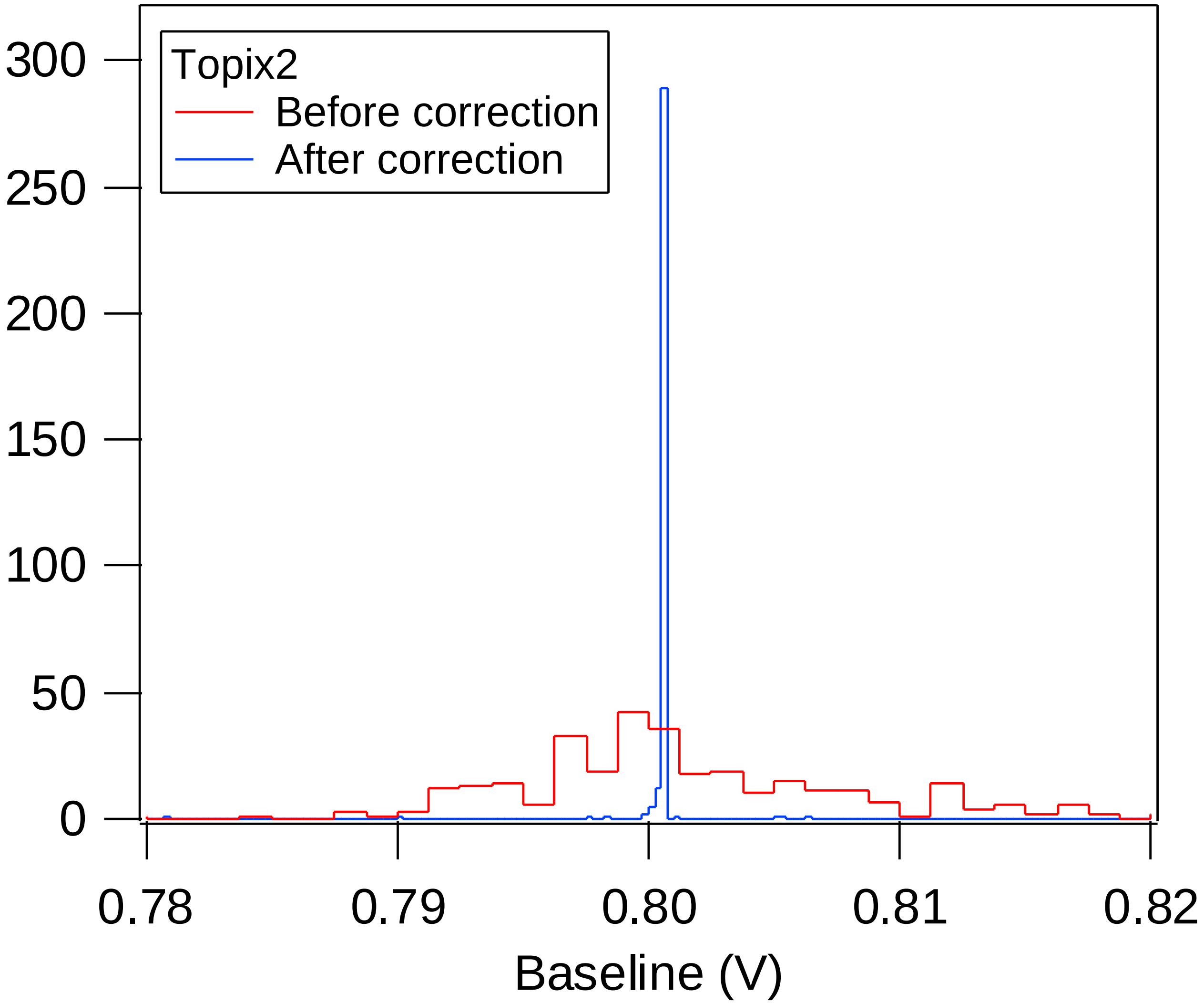


18
16
14
12
10
8
6
4
2
0
ToT [us]
0
20
40
60
80
100
120
Input charge [fC]
Pixel 16
Pixel 21

Across chip ToT variation

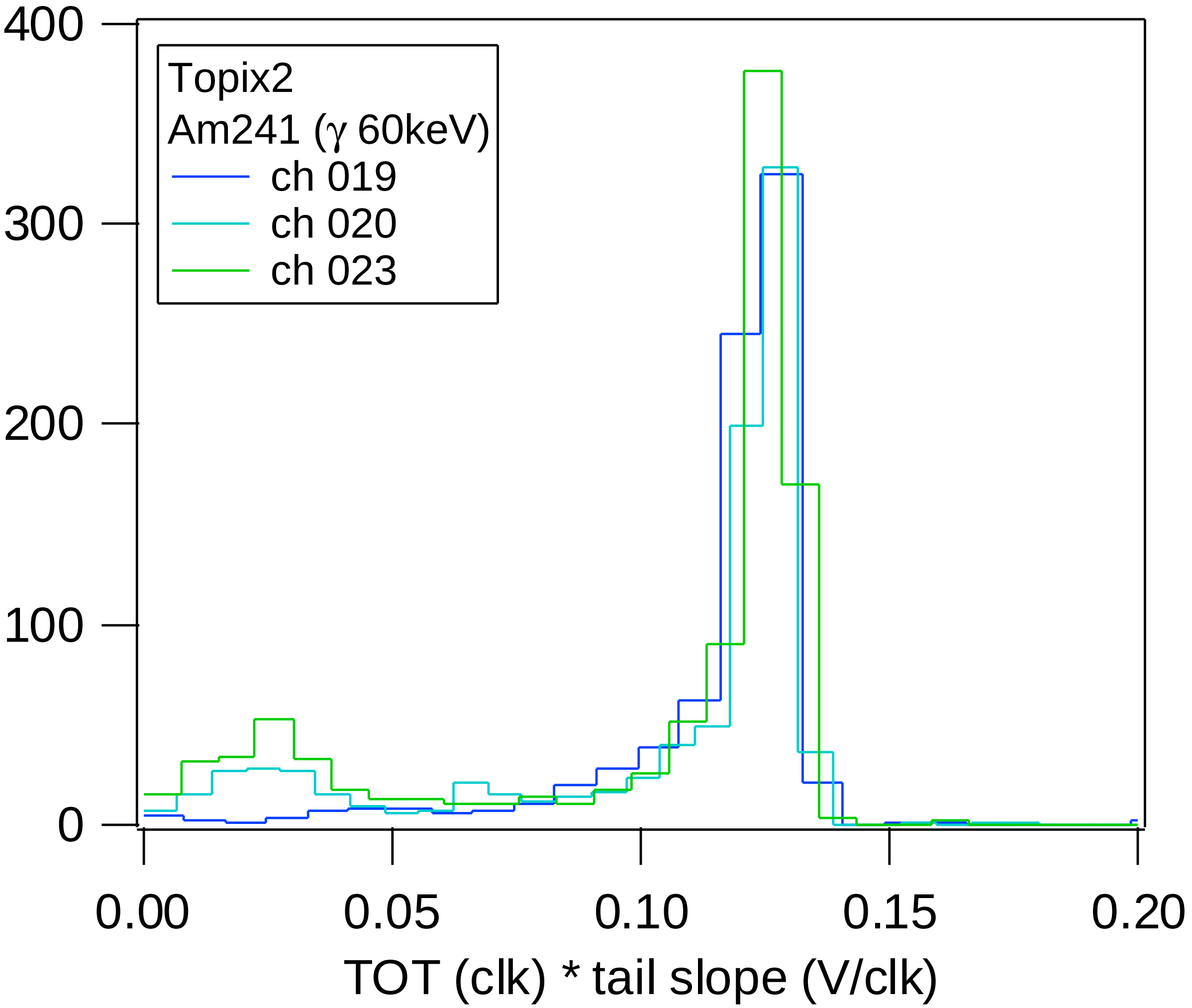


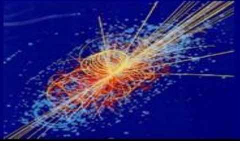
Measure: threshold dispersion



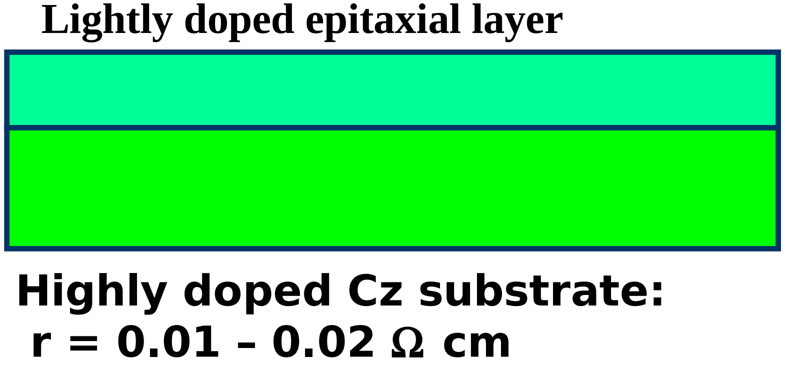
Measure: calibration with Am source

Standard p-type sensor 300 μm thick:





Epitaxial silicon sensor (1)

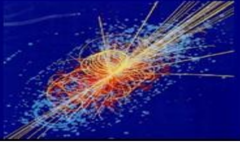


- **Several studies indicate that sensor build on epi wafer have good radiation tolerance.**
- **Interest for PANDA: radiation tolerance adequate with standard p-type design.**

Wafers supplied by ITME and processed by FBK-IRST in Trento
Project partially funded with through the ULISI-FP7 program

- **Substrate properties:**
  - **Diameter: 100 ± 0.5 mm.**
  - **Doping type: n/Sb.**
  - **Thickness 525 ± 25 μm.**
  - **Resistivity: 0.01 – 0.02 Ω cm.**

- **Epi layer properties:**
  - **Doping: time n/P.**
  - **Thickness 50/75/100 μm.**
  - **Variation: <4%/8%/8%**
  - **Resistivity: 2500 – 5000 Ω cm.**

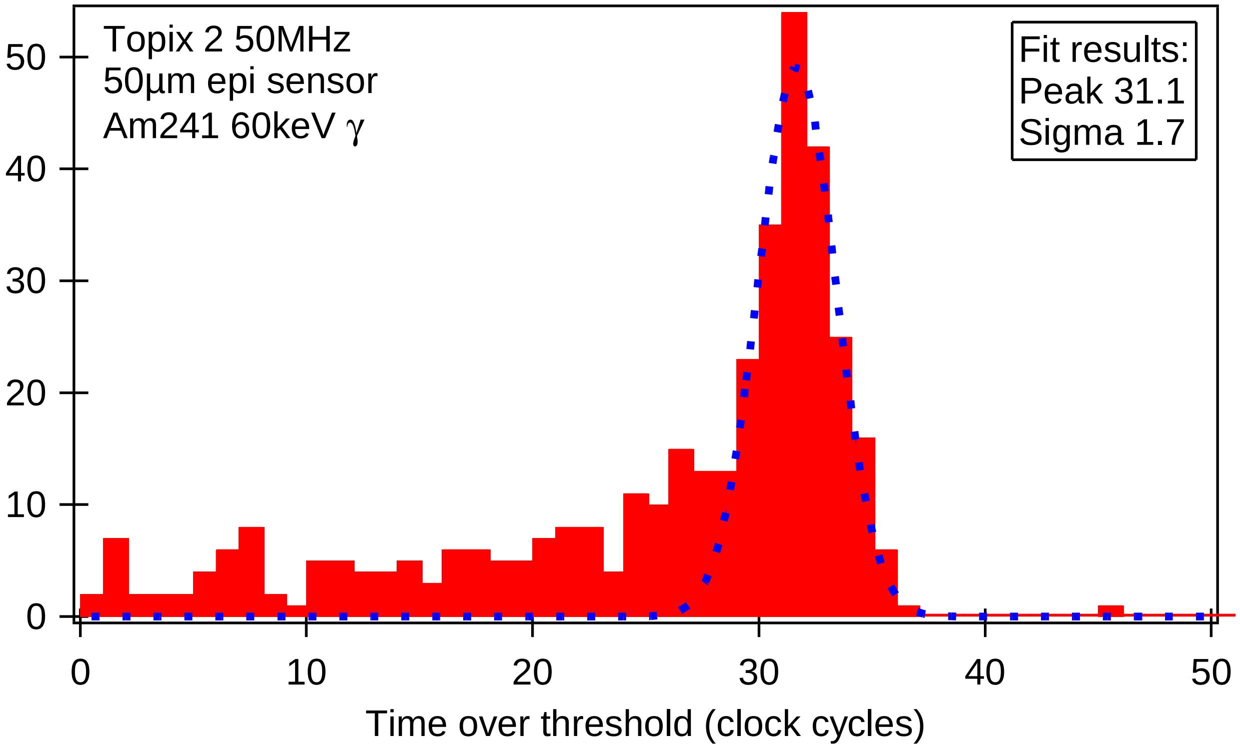


Epitaxial silicon sensor (2)

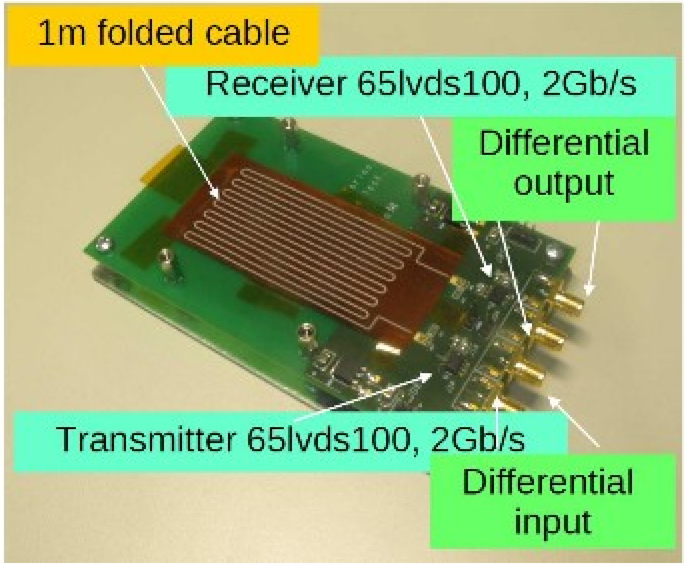
- **Low cost R&D reusing existing electronics and sensor design:**
  - **Electronics: ALICE front-end chip provided by CERN**
  - **Sensor: masks developed by INFN-Ferrara for NA62 project.**
- **Three types of epi assemblies:**
  - **3 with 150 µm total thickness (100 µm epi)**
  - **7 with 120 µm total thickness (75 µm epi)**
  - **1 with 100 µm total thickness (50 µm epi)**

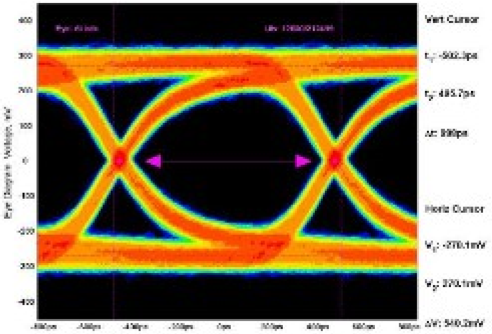
  - **Spare sensors to be wire-bonded to the prototype**

First spectra with an epi-sensor



Data transmission cables





Techfab: 7µm Al on 50 µm Kapton
CERN: 15 µm Al on 70 µm Kapton

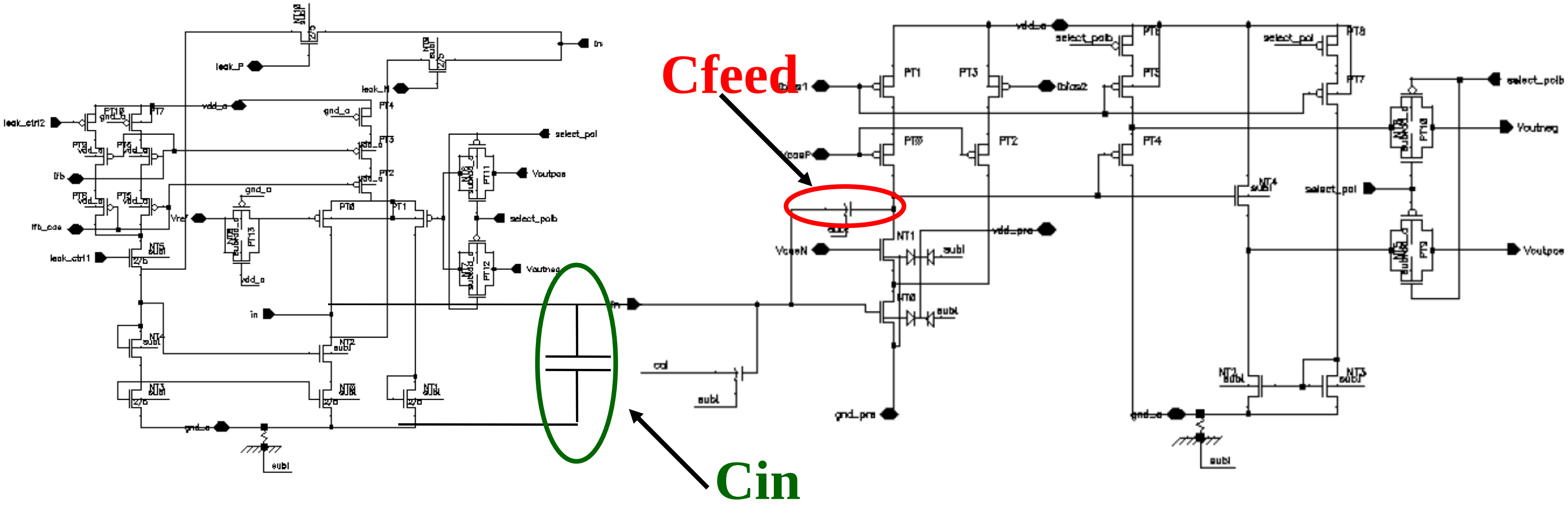
- 2-3 300 Gbit/sec link per front-end
- Al cable with 2Gbit/sec under study
- Transmission from the MVD to the counting room via the GBT chip set (under development at CERN).

Next steps

- Sumbit a new version on the front-end chip (scheduled for Nov. 2010)
  - Minor modifications in the analogue part
  - Opening for bump bonding
  - Migration to the baseline flavor of the process (thick upper metals for power distribution).
  - Full end of column logic
- Bump bonding with epitaxial silicon sensors
- 2011 devoted to detail testing
- Start the preparation of the engineering run in 2012.

SPARE SLIDES

Dynamic range



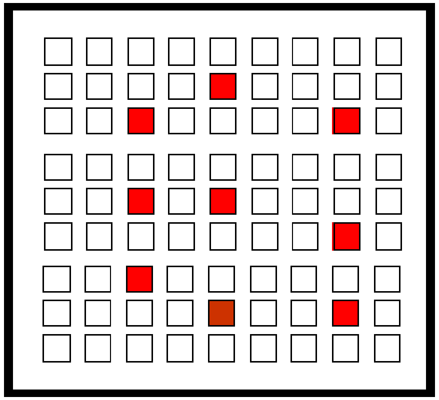
- **Linear mode (core amplifier not saturated): the signal charge is integrated on the feed-back capacitor Cfeed and removed by a constant current: 0.7 V/24 fF=16.8 fC.**

- **Saturated mode (core amplifier gain drops): the signal is integrated on the input capacitor and removed by a constant current**

- **Qmax=0.3V x 200 fF=60fC (n-type sensors) or 0.7V x 200 fF=140fC (p-type sensors).**

Saturation and cross-talk (1)

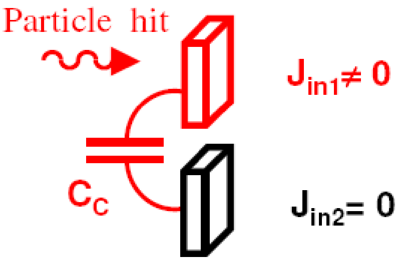
Pixel Matrix

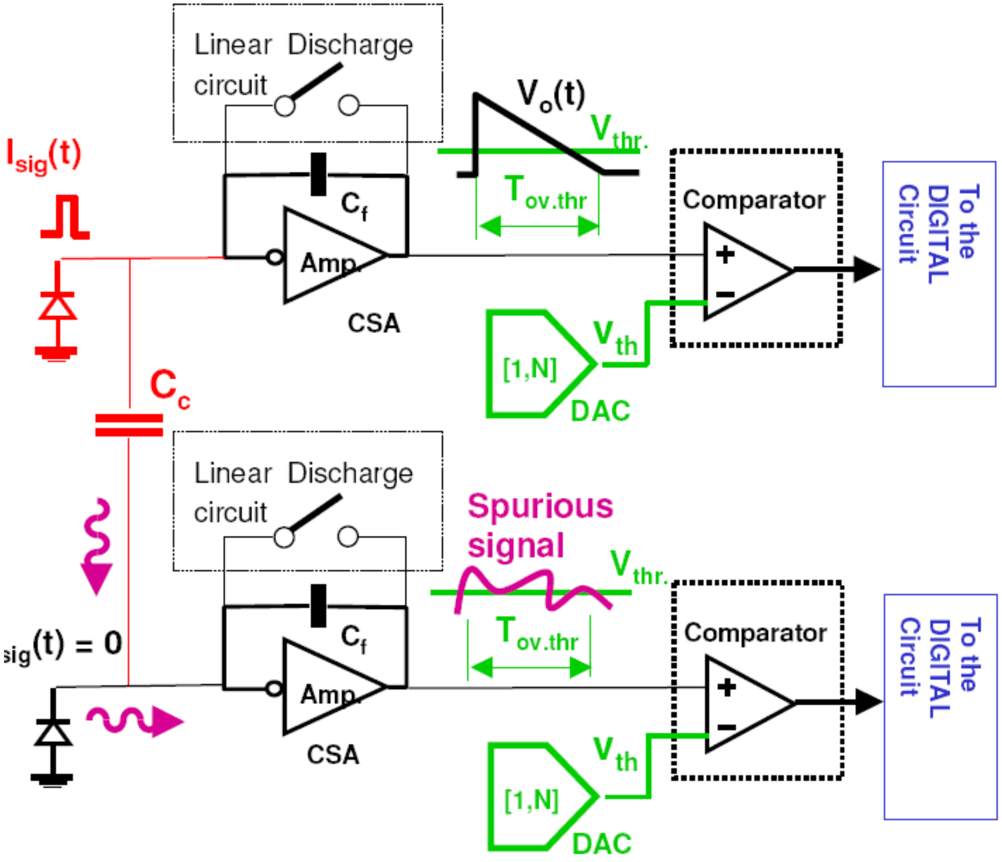


🟥 hit event

☐ no hit event

Adjacent Coupled Detectors





Saturation and cross-talk (2)