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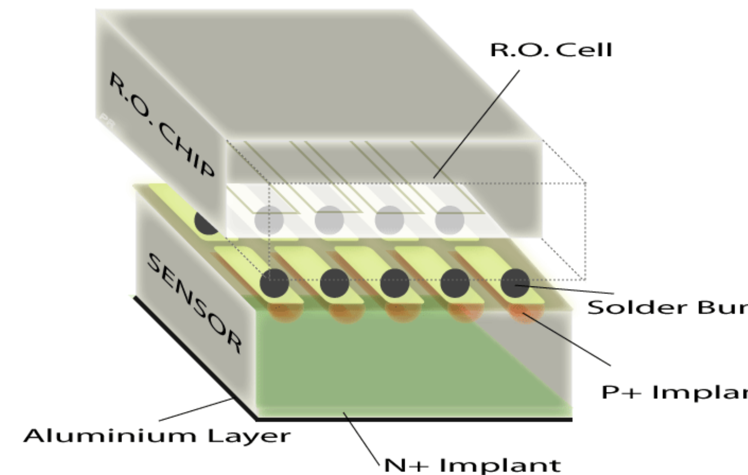
Interconnect Technologies >> Talk by Michael Campbell

Hybrid Pixel Detectors

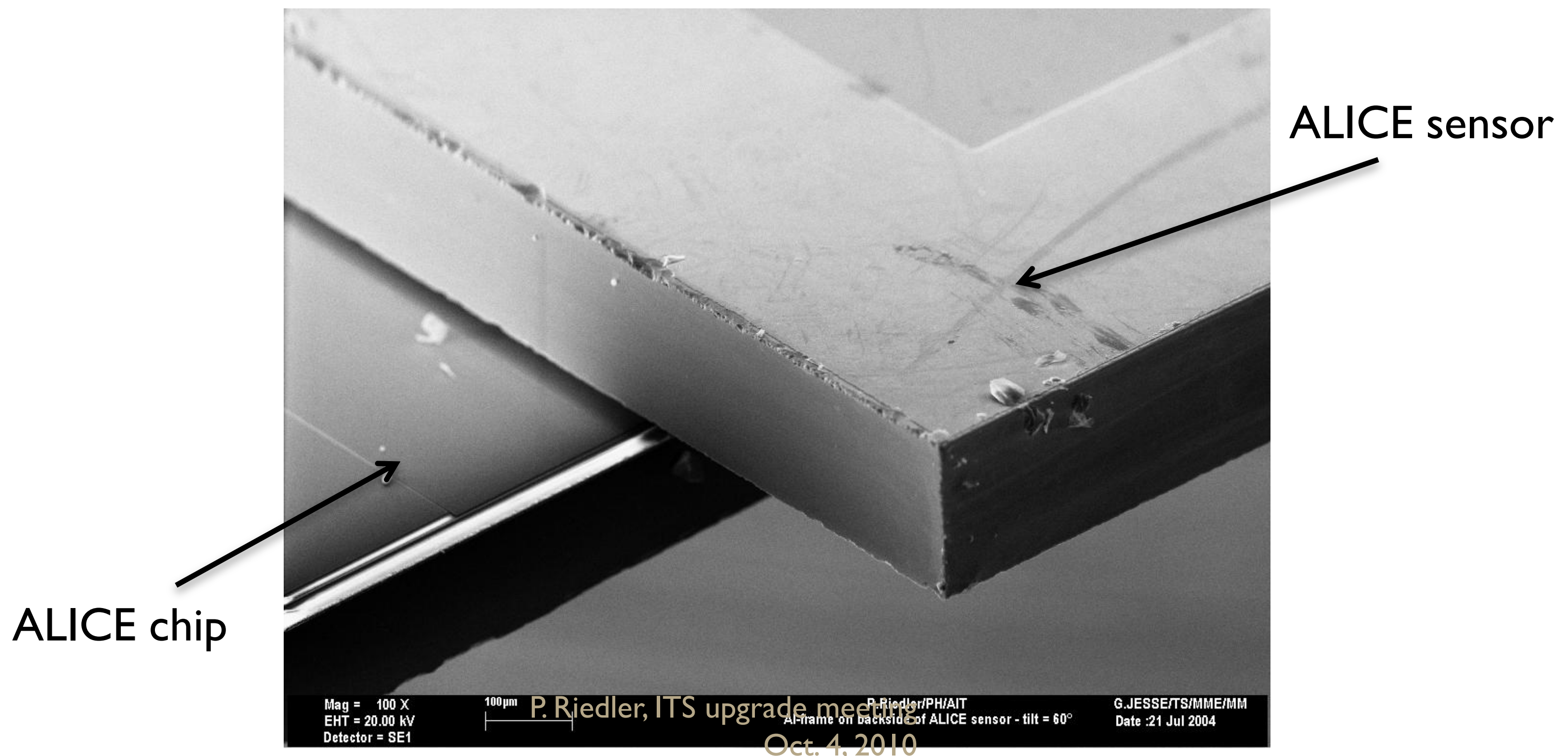
- Simplified view: Sandwich
  - Sensor
  - Frontend-readout chip
  - Interconnect (bump bonds)

- Sensor and chip can be optimized separately



Hybrid Pixel Detectors

- In reality we deal with a complex structure, where all the components are tightly linked to each other.

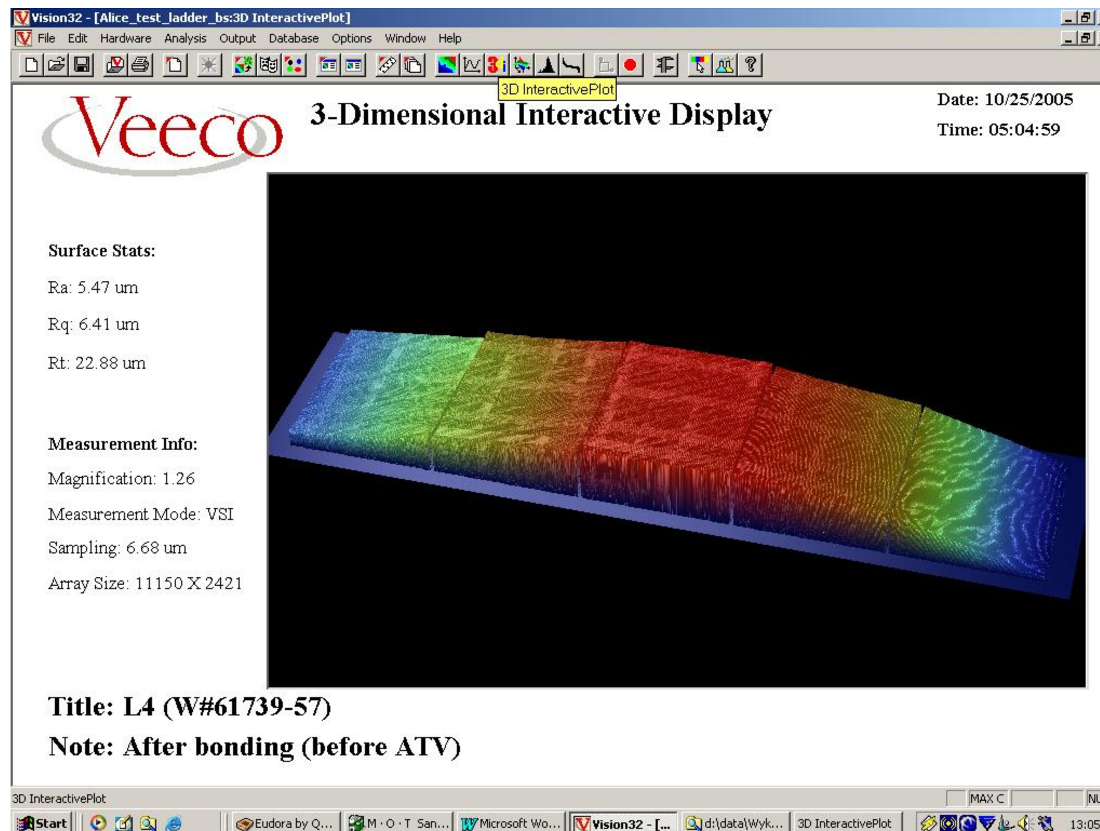


Hybrid Pixel Detectors

- Optimising one aspect can lead to a considerable increase in complexity of another one:
  - Thinner sensors >> feasibility, yield issues, cost, handling issues during bumping,..
  - Thinner readout chips >> handling, deformation, maintain high bump yield
  - …

Hybrid Pixel Detectors

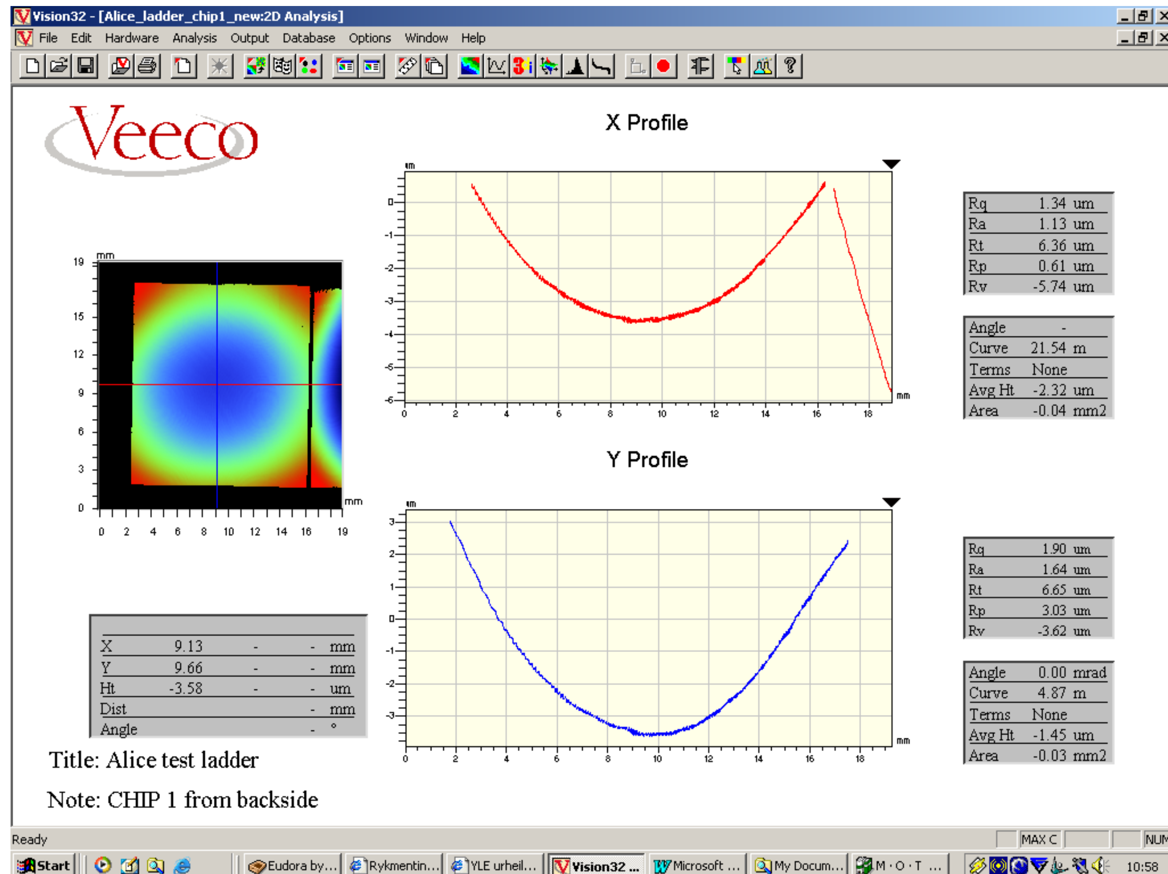
- ALICE pixel ladder with 5 readout chips



S.Vahanen

Hybrid Pixel Detectors

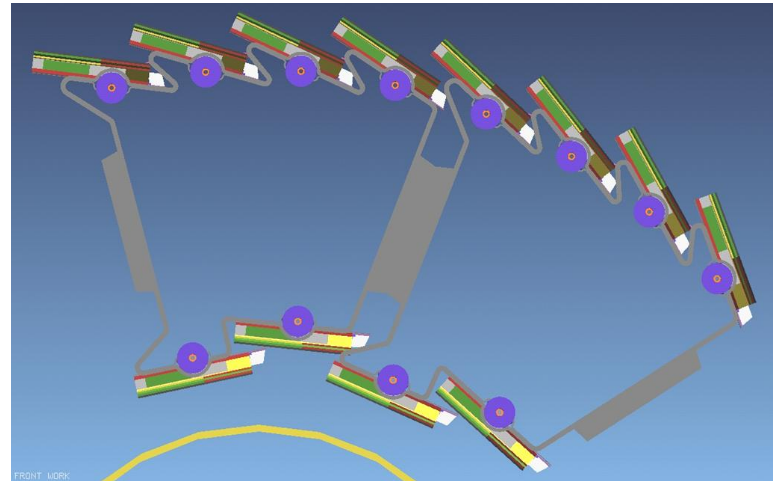
- ALICE readout chip



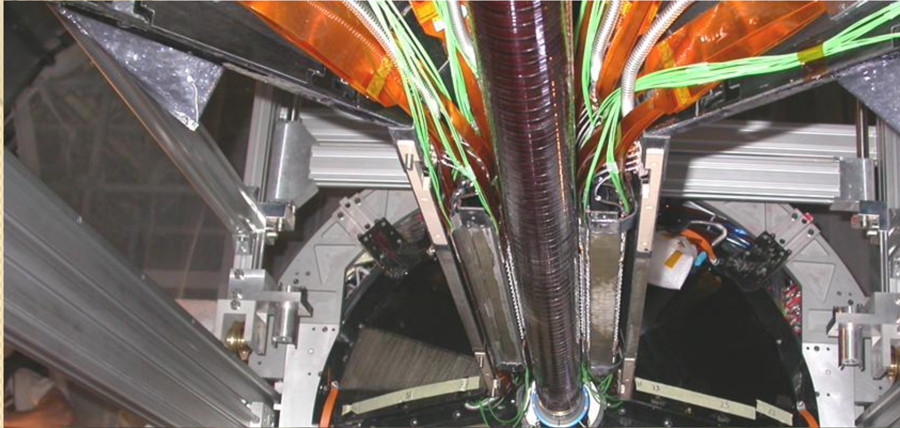
S.Vahanen

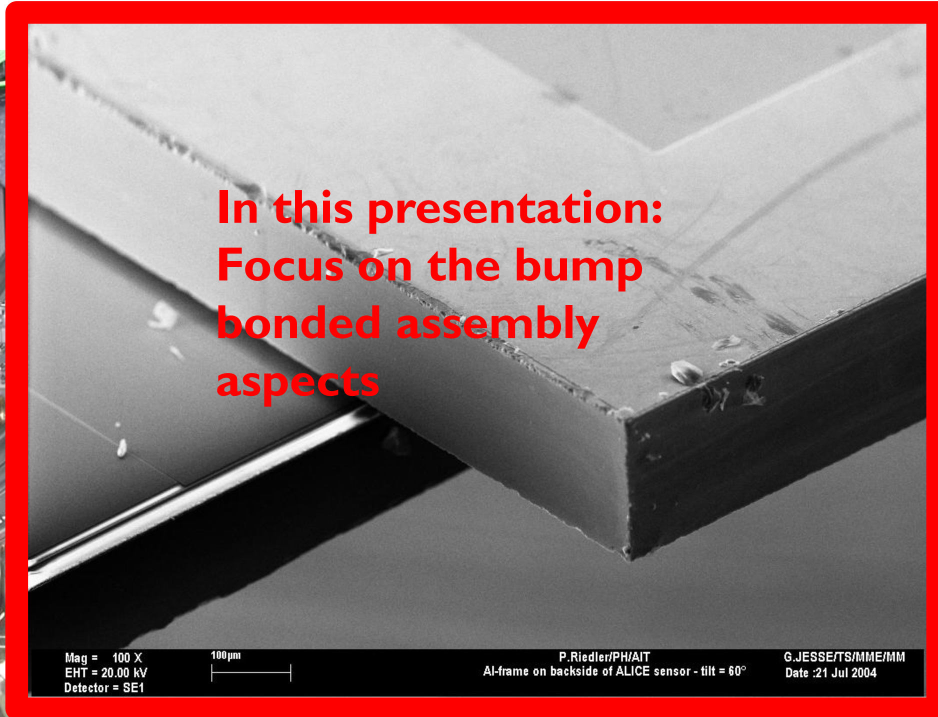
Hybrid Pixel Detectors

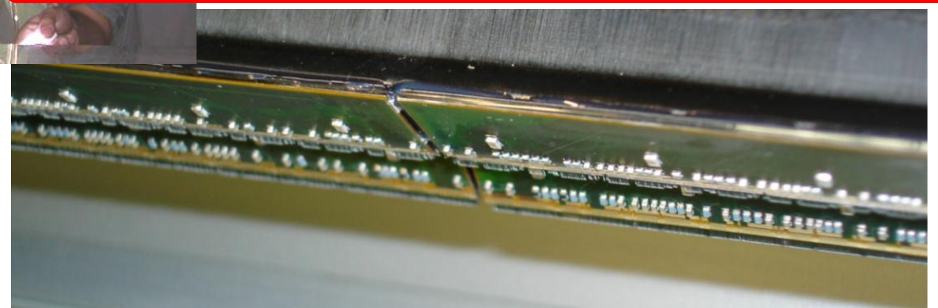
- Extending the view to the system, there are many other issues to consider:
  - Module assembly
  - Interconnect structures to the on-detector electronics
  - Mechanics
  - Cooling
  - …..



Hybrid Pixel Detectors





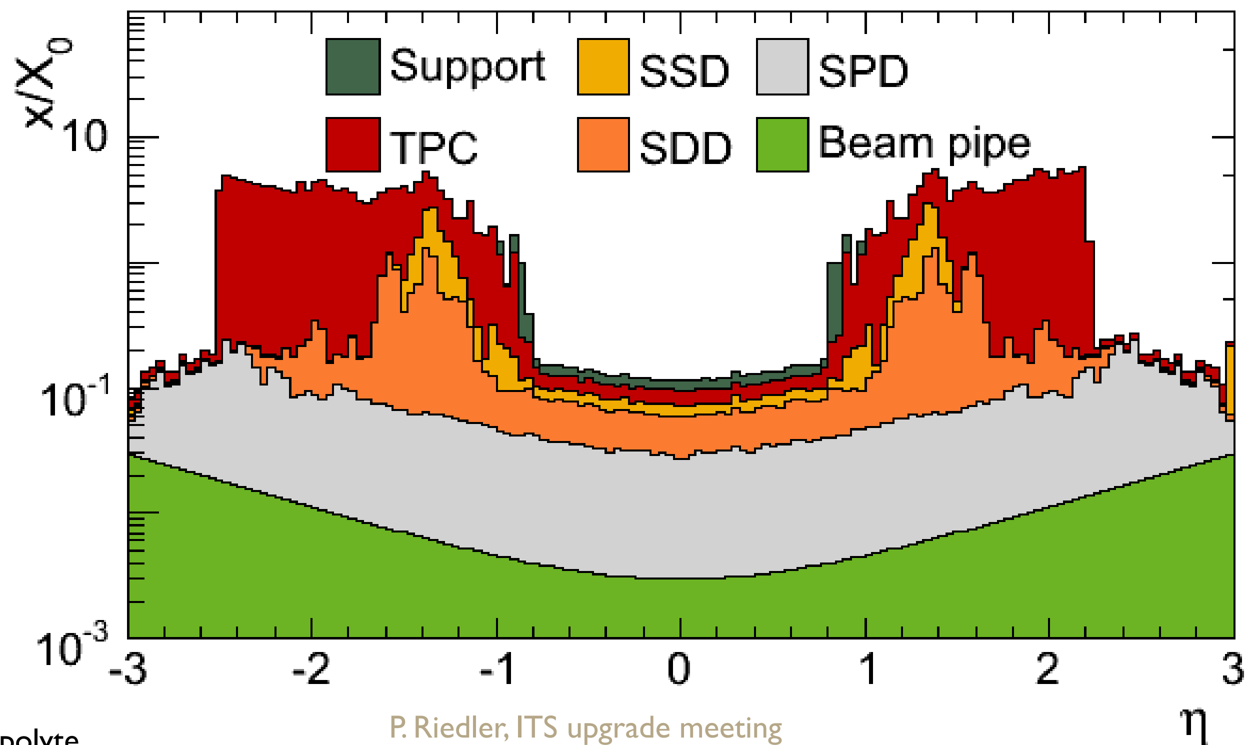


Some Key Questions

- REQUIREMENTS: pixel size, trigger, time information, ….
- MATERIAL
- COST

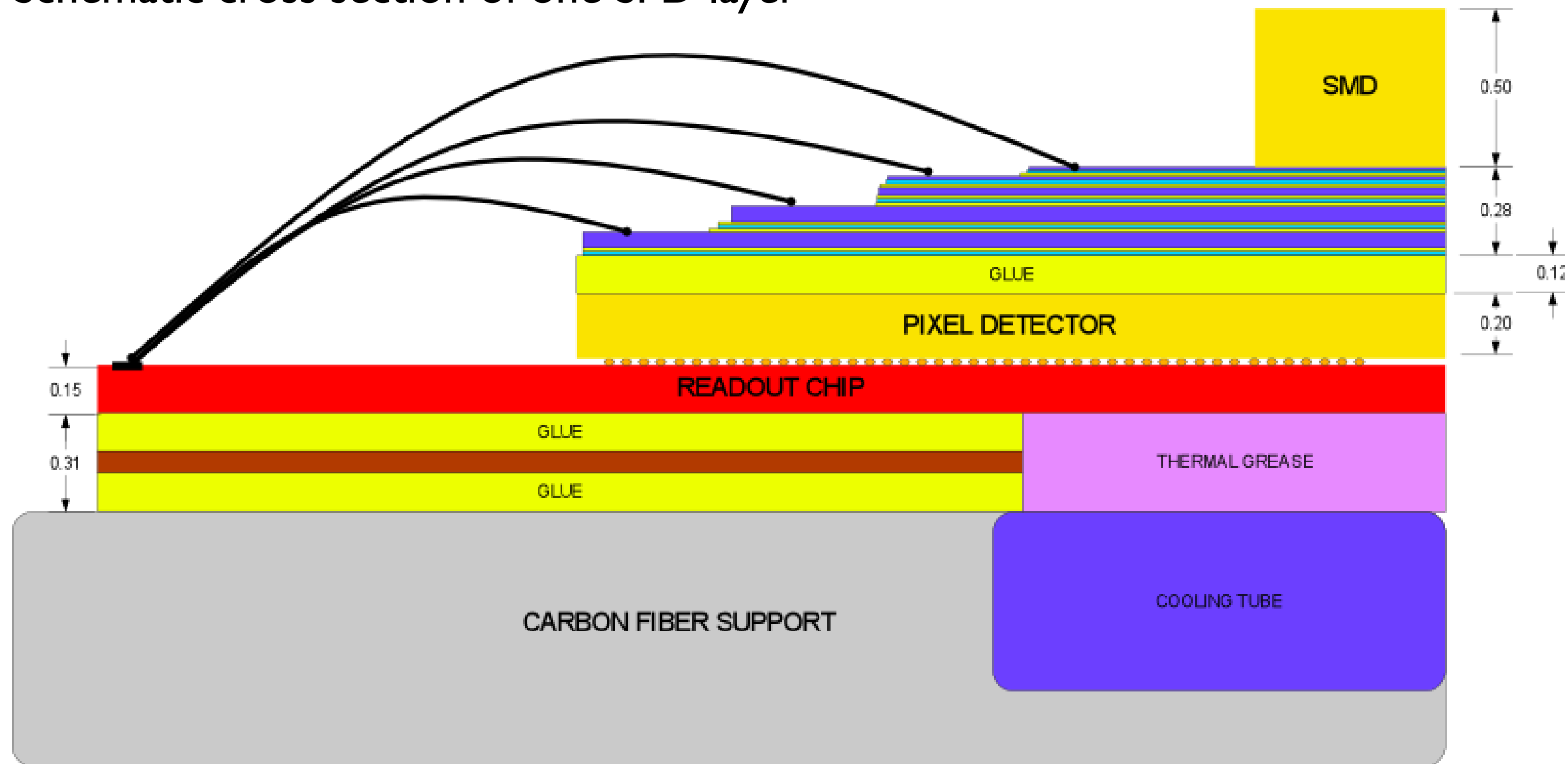
Material

- Current status in ALICE:
  - About 1.1% X0 per layer in the central region



Material

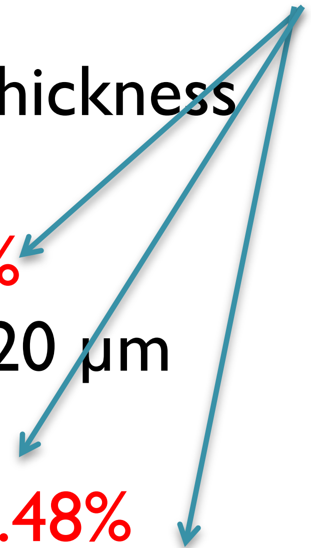
Schematic cross section of one SPD layer



Material

In one SPD layer:

- Carbon fibre support: 200 μm
- Cooling tube (Phynox): 40 μm wall thickness
- Grounding foil (Al-Kapton): 75 μm
- Pixel chip (Silicon): 150 μm >> 0.16%
- Bump bonds (Pb-Sn): diameter ~15-20 μm
- Silicon sensor: 200 μm >> 0.22%
- Pixel bus (Al+Kapton): 280 μm >> 0.48%
- SMD components
- Glue (Eccobond 45) and thermal grease



Material

- 2 main contributions: silicon and interconnect structure (bus)
- Compare silicon contribution:

	Si sensor [µm]	X_0 [%]	ASIC [µm]	X_0 [%]
ALICE	200	0.21	150	0.16
ATLAS	250	0.27	180	0.19
CMS	285	0.30	180	0.19

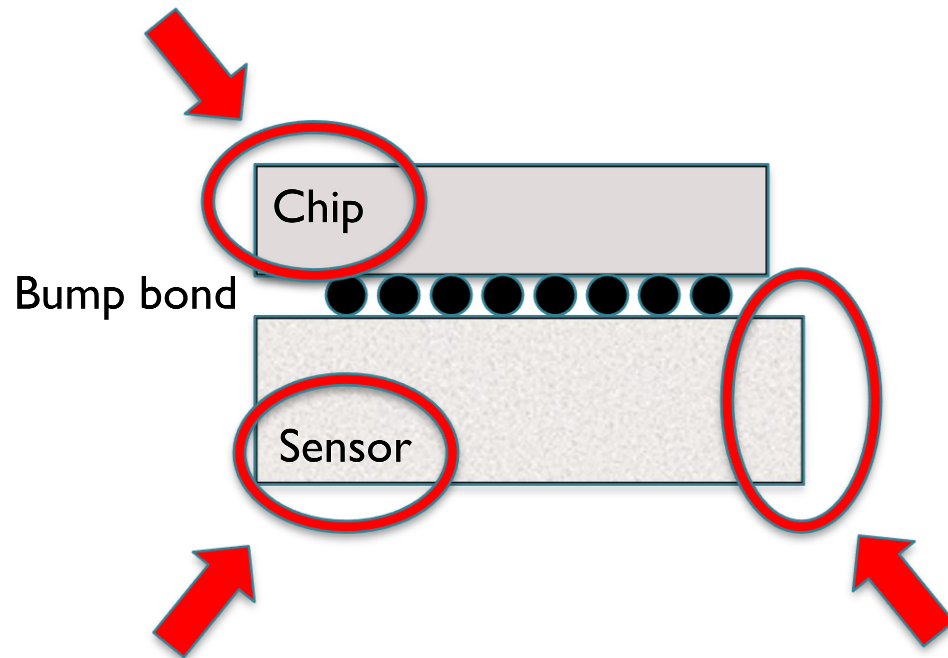
Material

- How can the material budget be reduced?
  - Reduce silicon chip thickness
  - Reduce silicon sensor thickness
  - Reduce bus contribution
  - Reduce edge regions on sensor
  - Review also other components (but average contribution 0.01-0.02%)

Material

Reduce frontend chip thickness

Maintain high bump bonding yield (>99%) with reduced thickness components



Reduce sensor thickness

Reduce insensitive area at sensor edge, reduce overlap of modules, avoid gaps

Material – Thinner Sensor

- Current ALICE sensors: 200 um p-in-n FZ
- Reduce thickness (keep in mind to have enough signal for the electronics!)
- Challenge:
  - Get thin blank wafers (FZ!)
  - Process them at a foundry (4" preferred, 6"?)
  - Process and handle them during bump bonding
- Target: 100-150 um
- Tests, e.g.:
  - Thin float zone wafers
  - Epi wafers which are thinned during bumping

Material – Thinner Sensor

- First trials in 2010:
  - Purchase of 16 epi wafers (epi thickness 100 um and 120 um)
    - Processing of epi wafers ongoing
    - Bump bonding and thinning of epi sensors to existing ALICE pixel chips to be done at VTT; expect first single chip assemblies back in Nov./Dec. 2010
  - Purchased 25 thin FZ sensor wafers (180 um, 150 um)

Material – Thinner Chips

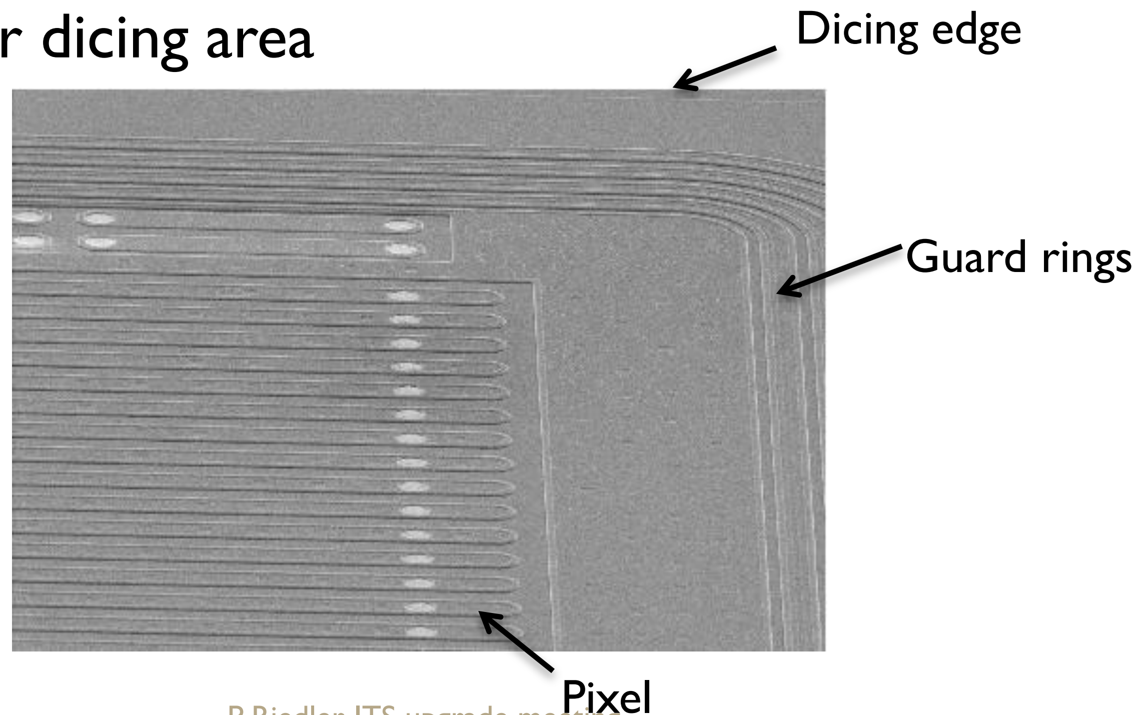
- Current ALICE chips: 150 um thinned during bump bonding process
- Challenge:
  - thickness reduction will make inherent stresses come out stronger >> detachment of bump bonds could appear during process
  - Process needs to be well studied and developed
- Target: 50 um thick chips
  - Will probably require intermediate step: e.g. 80 um

Material – Thinner Chips

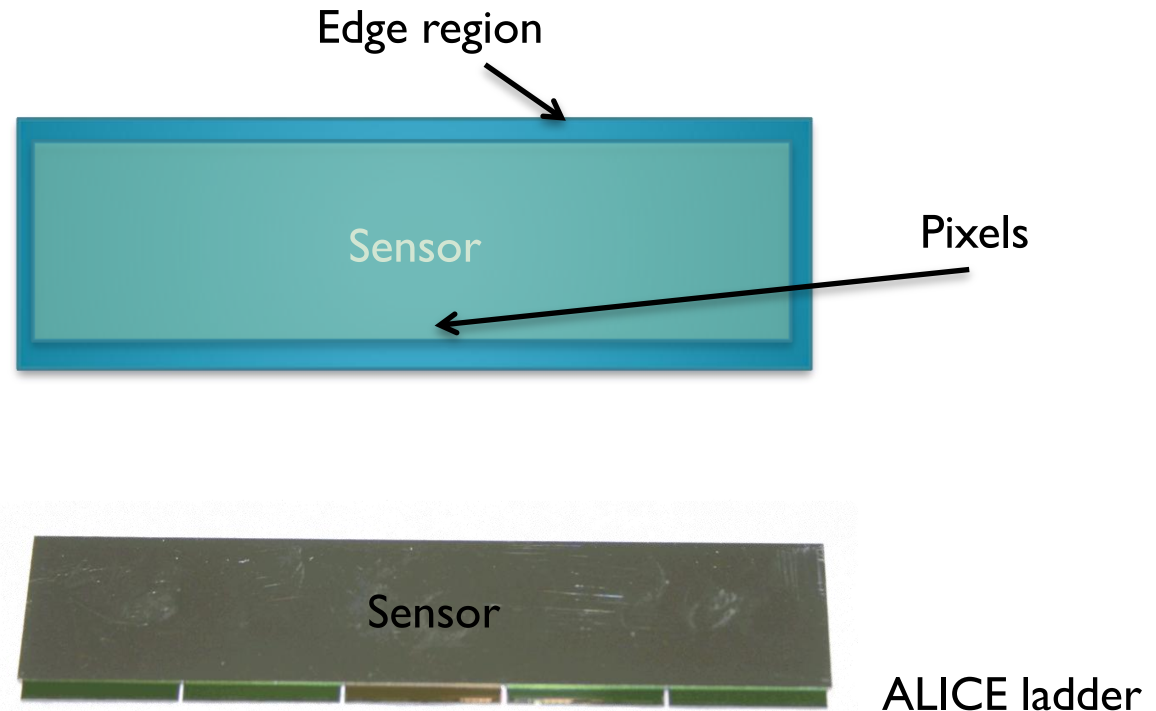
- First trials in 2010:
  - Work plan defined in several phases:
    - Process tests with dummy wafers to demonstrate thinning capability
    - Assembly of thin dummy components
    - Validate process by thinning and assembly of real ALICE sensor and chip components
  - Dummy sensor wafers produced using ALICE layout
  - Work starting ~ few weeks

Material – Reduce Edge Region

- Current ALICE sensors: ~1.2 mm (rϕ), ~1.2 mm (z) edge region on each sensor where particle signals are not registered
- Used to degrade the voltage to the edge (guard rings) and for dicing area

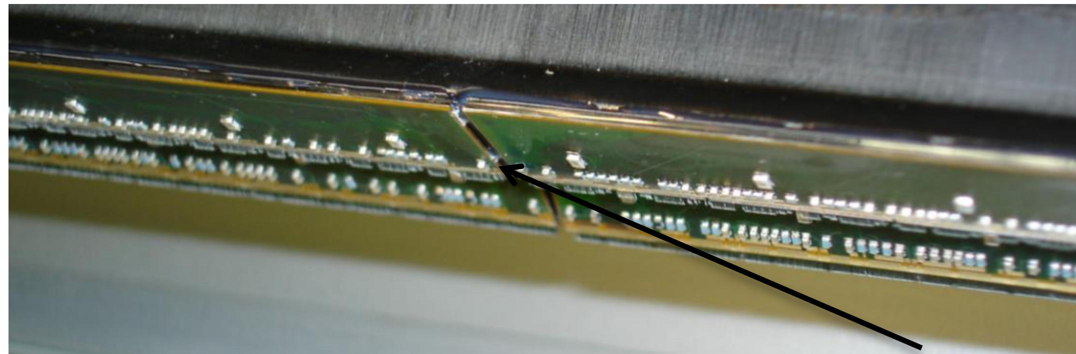


Material – Reduce Edge Region



Material – Reduce Edge Region

Gap between sensors (ladders)



Gap between half-staves

Material – Reduce Edge Region

- First trials in 2010:
  - Received first bump bonded 3D sensors with ALICE layout beginning of 2010
    - Successfully tested in the lab
  - Participated in MPW edgeless sensor test at FBK (no material back yet); could potentially reduce edge region to few microns!
- Other interesting options:
  - Discuss alternative sensor layout using 3D techniques
  - Investigate laser dicing
  - …

Material - Interconnect

- Current bus presents ~0.48% of X_0
- Several aspects can be studied for a future bus:
  - Reduce the number of layers by routing e.g. power on the back side of the chips (TSVs necessary)
  - Design frontend electronic chips so that the number of traces/planes on a bus can be minimized
  - Could the mechanics support carry some traces (maybe crazy)?

Cost

- Cost driver in current configuration: bump bonding
- Several initiatives to reduce bb costs, e.g. using fine grain solder paste
  - See talk by Michael Campbell!
  - Requirements (pixel size >> bump bond size) will have also an impact on available choices

Cost

- Other contributions:
  - "clever" sensor/chip wafer layout to reduce handling steps during processing at the bump bonding site (e.g. reduce dicing steps to minimum)
  - Under-bump-metallization could be already deposited by the sensor manufacturer (need close collaboration with sensor manufacturer and bump bonding producer!)
- Using thin components decreases usually the yield in processing >> increases cost

Summary

- Hybrid pixel detectors are one option to study for an ITS upgrade.
- Several strategies can be studied to further reduce material and cost for such a detector