The VFC-HD
The BI common back-end board

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Andrea Boccardi on behalf of SY-BI
Result of a BI effort to standardise its instrumentation back-ends and increase synergies in the group
A bit of history: from the VFC to the VFC-HD

For BI the VFC project was a success because:
1) Big-volume projects created mass (and inertia!)
2) Small-volume projects were listened to
The numbers and the systems

1150 boards produced (and is not enough…)

The back-end for the following instruments (some in place, some to come):

- **BPM**: AWAKE, ALPS/SPS & TT2/TT10, LHC interlock
- **BLM**: diamond and standard for injectors and LHC
- **Tune**: all machines
- **BCT**: fast and 24bit-DC for all the machines and transfer lines
- **Luminosity monitor**
- **Wire-Scanners**: LHC and injectors
- **Motor controller** (sub system)
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11/04/2008

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Note: Not enough...
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A multi-section effort

- Specifications discussed and agreed in dedicated **BI technical boards**
- Work and inputs from many sections:
  - **BI-BP**: main design, production test, system HDL design
  - **BI-IQ**: design review, system HDL design
  - **BI-BL**: power supply modules design, burn-in test design
  - **BI-PM**: test and validation from ‘power-users’
  - **BI-SW**: driver and low level SW

Participation in the process makes it easier to understand and accept the compromises.
Not just HW, the creation of synergies

Common back-end

Common ‘system’ part of the Gate-Ware (GW)

Common ‘system’ drivers

Development of BI wide GW libraries

Development of a base project to speed up new developments and keep consistency
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Creation of the BI-Digital Designers forum
Summary: What made it a success and the challenges

- Big-volume projects lead creating mass, but smaller ones are listened to
- Clear formal specification process, with wide participation
- Consultation in a ‘safe’ environment (BI-DD forum)

Timing is critical:
- Need a lead project
- Takes time to produce a common platform due to the production volume
- Hard to finance all the production....
What’s next...

We have long term projects needing a new platform

We have shorter term projects needing VFC-HD but we have few to spare

We need to investigate suitable standards for a new platform.

Probable lead projects:

- LHC-BPM consolidation (LS4)
- Pre-injector chain BPM consolidation (LS4+)
References

Best practices: https://edms.cern.ch/ui/file/2135617/1/
Best_practices_for_electronics_design_at_CERN.pdf


BI-DD meetings: https://indico.cern.ch/category/10180/

VFC-HD git: https://gitlab.cern.ch/bi/VFC