
CERN
HSE
Occupational Health & Safety
and Environmental Protection unit

CROME

Hardware/Software Co-Simulation of a Zynq SoC inside the CROME Measurement and Processing Unit

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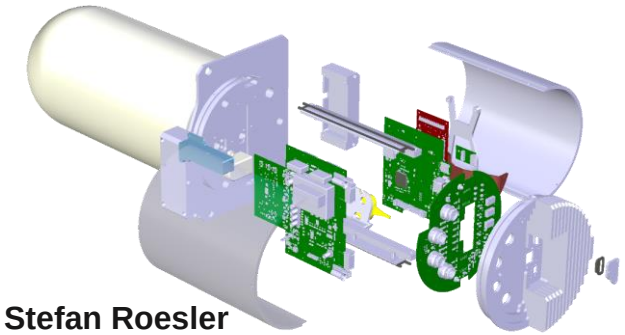


23/11/2021 - System-on-Chip Interest Group Meeting - CERN

https://crome.web.cern.ch

Daniel Perrin, Gael Ducos, Markus Widorski, Michel Pangallo, Sarath Kundumattathil Mohanan, Doris Forkel-Wirth, Stefan Roesler

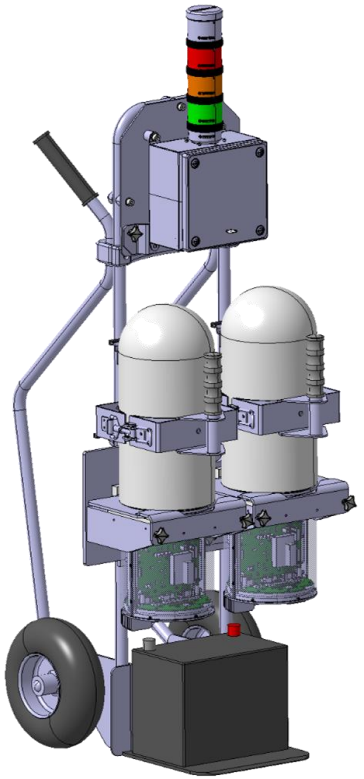
Agenda

Hardware/Software Co-Simulation of a Zynq SoC inside the CROME Measurement and Processing Unit

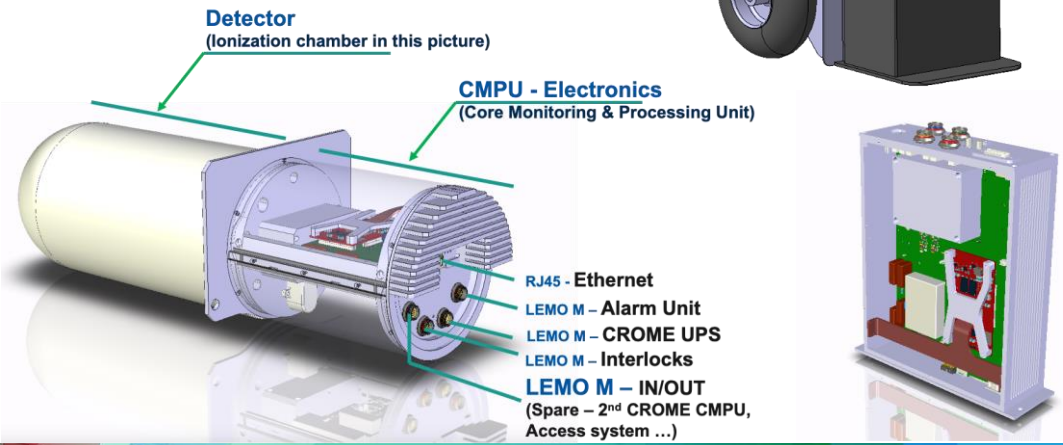
- What is CROME?
- HW/SW Co-Simulation
- Short Demo

CERN Radiation Monitoring Electronics (CROME)

New in-house developed and produced radiation monitoring system for CERN Radiation Protection



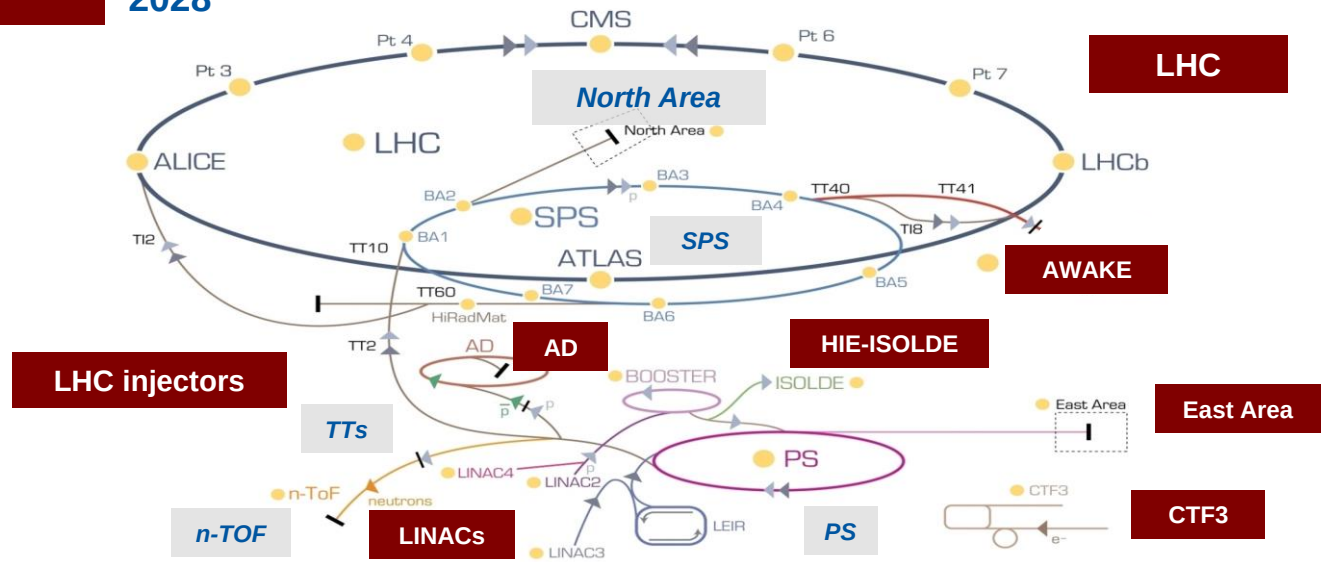
- Real-time monitoring of the ambient dose equivalent rate over **9 decades (from nSv/h to Sv/h)**
- Alarm and interlock functionality with a probability of failure down to **10e-7** (Link)
- Edge computing (an SoC FPGA based system)
- Long-term, permanent reliable data logging
- Unified solution for RP and environmental monitoring



TOWARDS A NOVEL MODULAR ARCHITECTURE FOR CERN RADIATION MONITORING
Radiat Prot Dosimetry. 2017 Apr; 173(1-3): 240–244.

Radiation & Environmental Monitoring System at CERN

CROME	2021
CROME	2028



Currently we have replaced :

153 radiation monitors, 78 alarm units, 107 Power Supplies

(532 pieces of equipment)

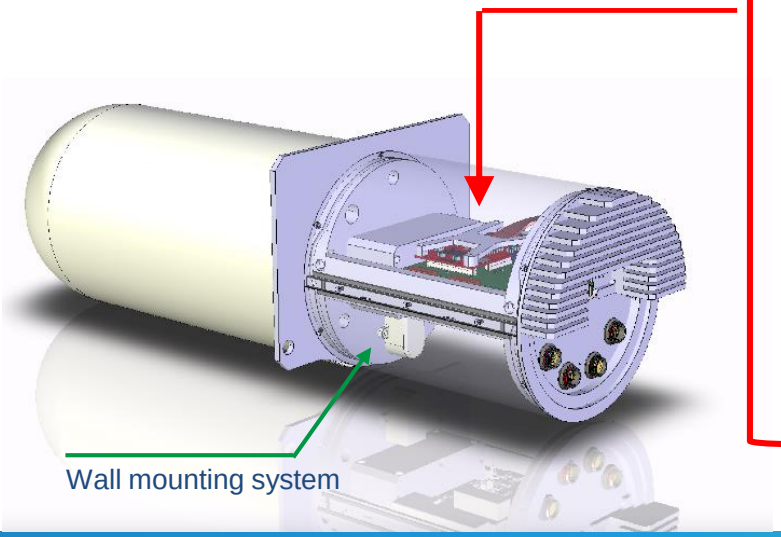
In-house design of CROME

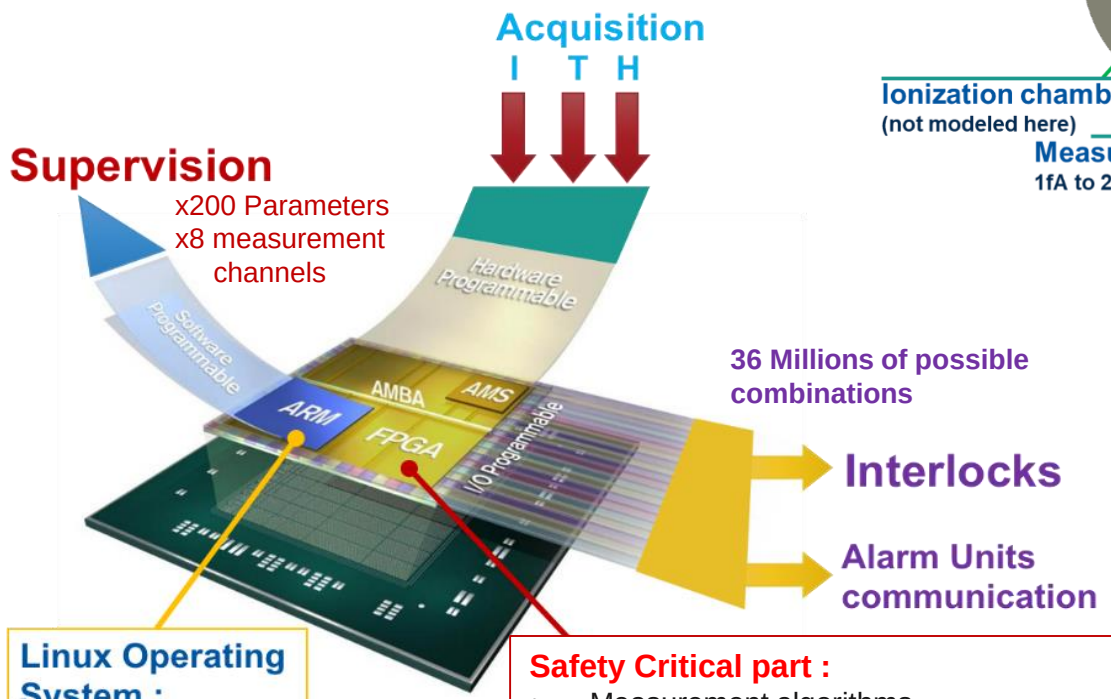
Self production capabilities

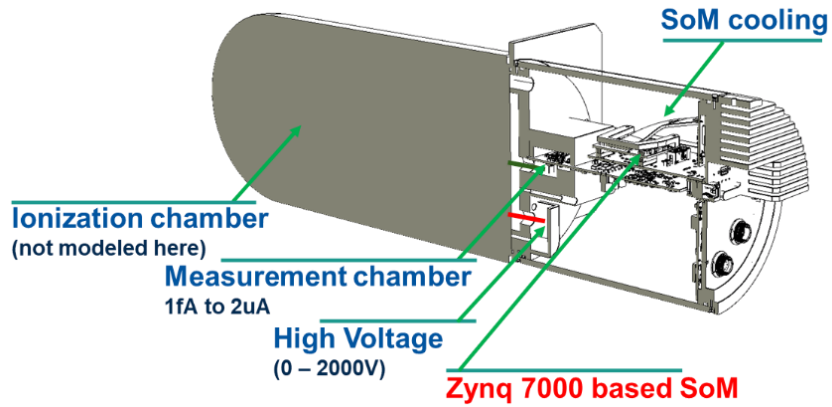
ARCON replacement by CROME EHN2

CERN Radiation Monitoring Electronics (CROME)

Highly Integrated Solution :







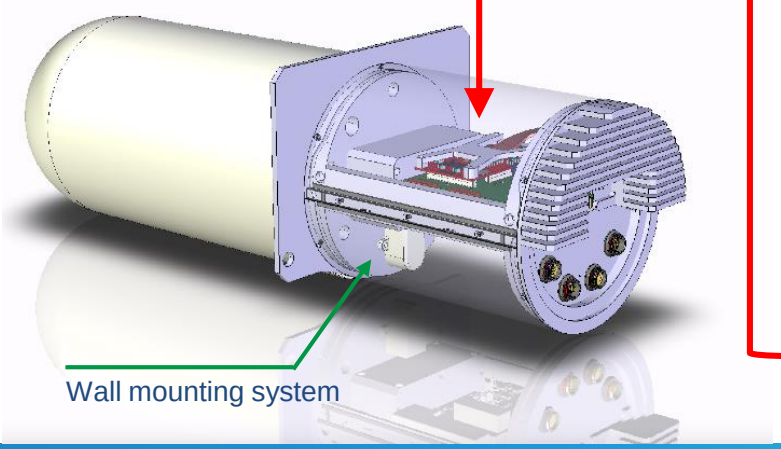
Linux Operating System :
- Data storage and management
- Supervision
- …

Safety Critical part :
- Measurement algorithms
- Real Time temperature compensation
- Dose rate calculations
- Cumulated dose calculation
- Interlock generation
- …

Fault Resilient Design for 28nm ZYNQ SoC based Radiation Protection Monitoring System Fulfilling Safety Integrity Level 2
First System-on-Chip Workshop – CERN – June 12, 2019

CERN Radiation Monitoring Electronics (CROME)

Highly Integrated Solution :

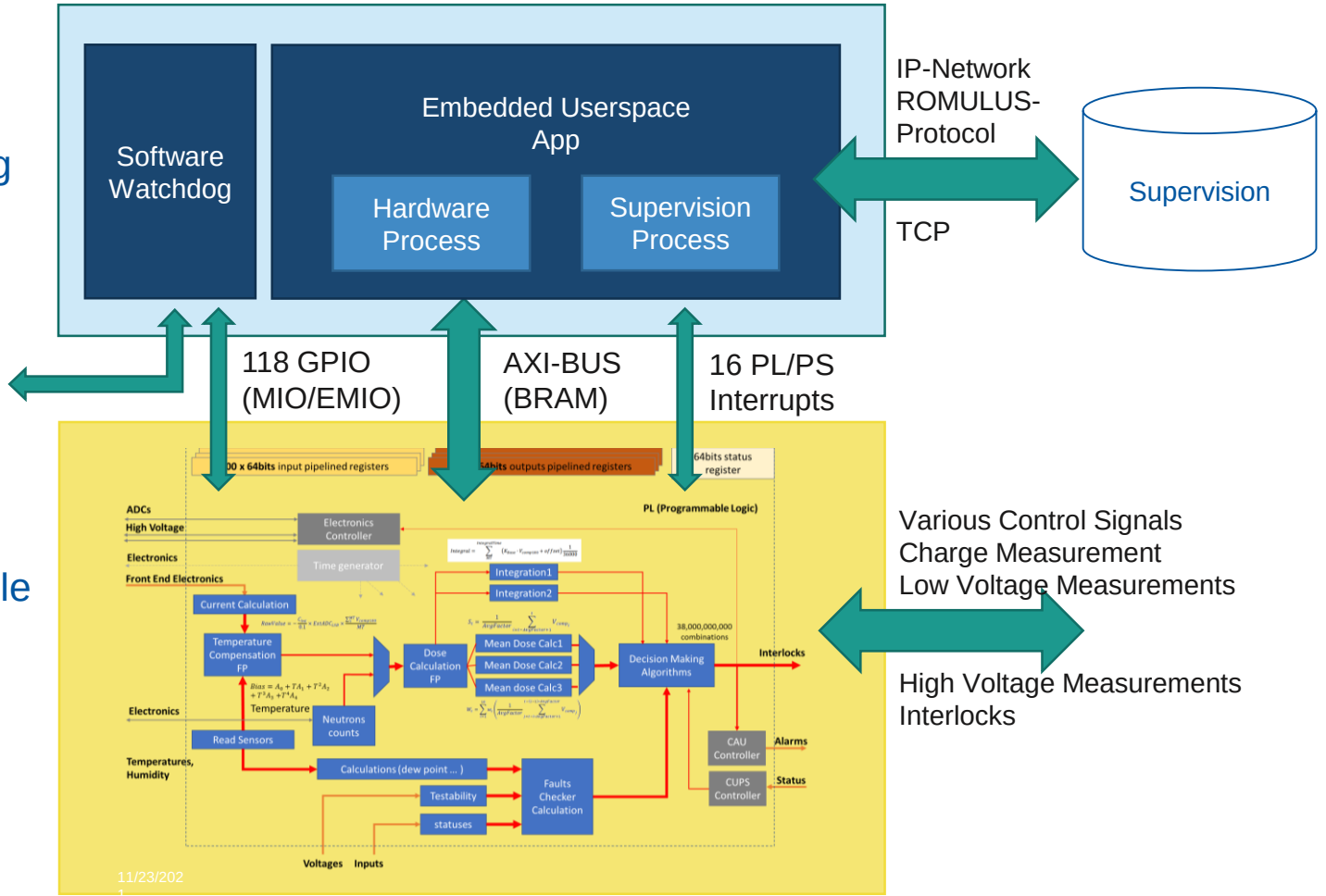


Processing **S**ystem

ARM

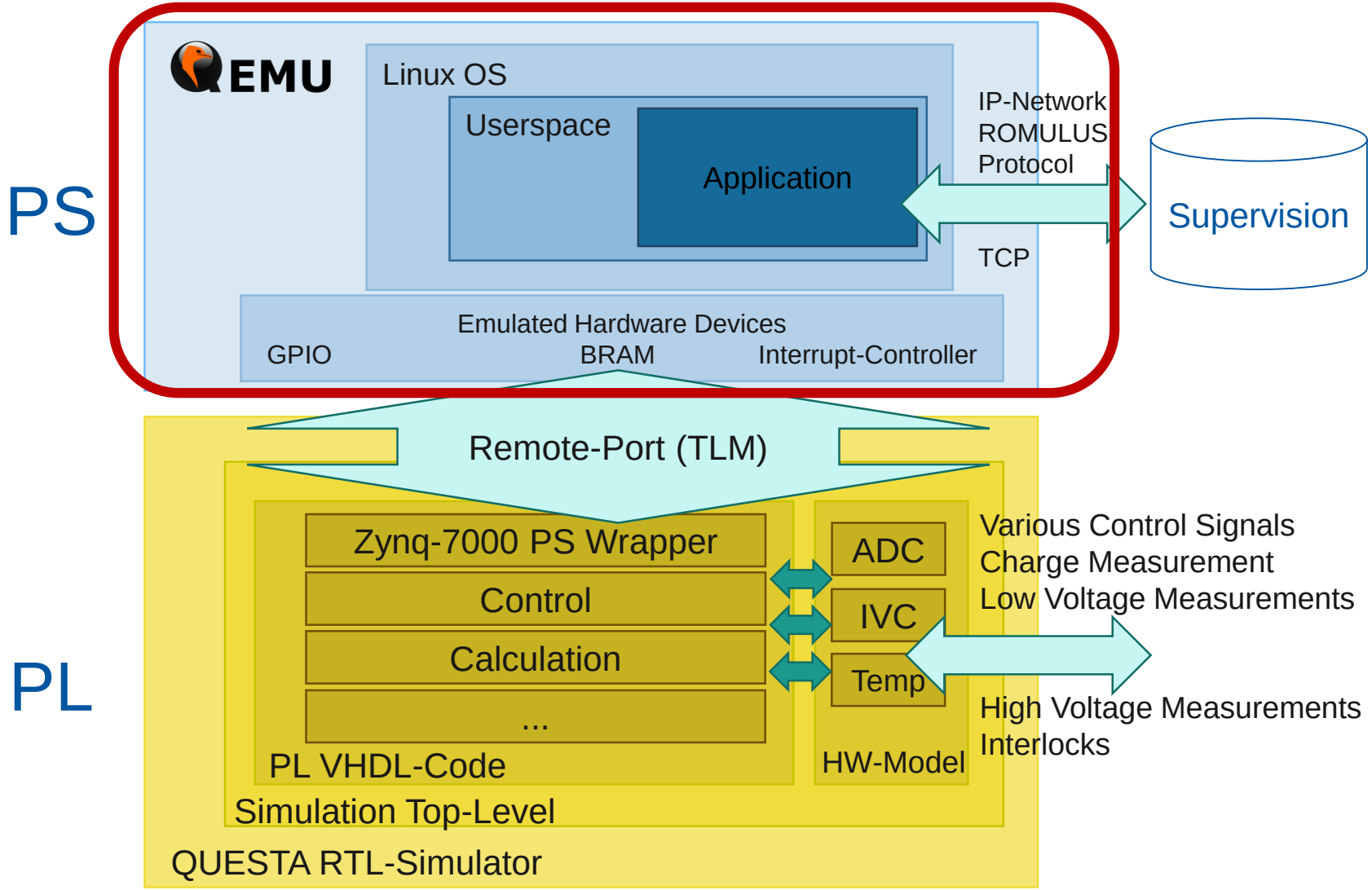
Programmable **L**ogic

FPGA



Hardware-/Software Co-Simulation

- **What?**
  - Simulation of software and hardware at the same time
- **Why?**
  - System level verification
  - Simplifies development because of visibilty of signals
  - Much faster than simulation of CPU in RTL → feasible
  - Virtual Prototyping. Hardware does not need to be available yet *(not applicable for us)*
- **How?**
  - Two simulators connected together to allow for simulation of entire system, so: one for Software and one for Hardware
  - QEMU simulating Linux and Questa for RTL


PS
QEMU
Linux OS
Userspace
Application
IP-Network
ROMULUS
Protocol
TCP
Supervision
Emulated Hardware Devices
GPIO
BRAM
Interrupt-Controller
Remote-Port (TLM)
PL
Zynq-7000 PS Wrapper
Control
Calculation
...
PL VHDL-Code
ADC
IVC
Temp
HW-Model
Various Control Signals
Charge Measurement
Low Voltage Measurements
High Voltage Measurements
Interlocks
Simulation Top-Level
QUESTA RTL-Simulator

QEMU

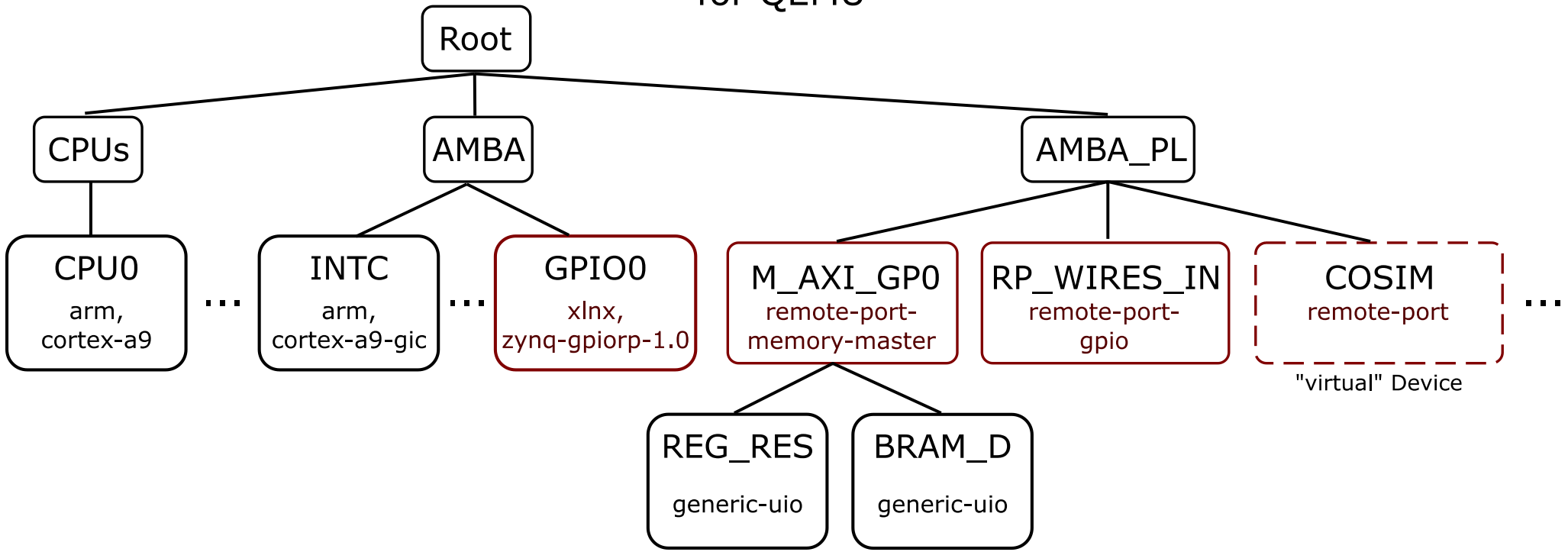
- “A generic and open source machine emulator and virtualizer”
- “provides a virtual model of an **entire machine** (CPU, memory and emulated devices) to run a guest OS”
- Translates Guest instructions dynamically to Host instructions

Our case

- Emulates the two ARM Cores and (implemented) peripherals on a desktop PC
- Runs Linux and embedded application

QEMU

HW - Device Tree
for QEMU



Register XGPIOPS_DIRM_OFFSET Details

This register controls whether the IO pin is acting as an input or an output. Since the input logic is always enabled, this effectively enables/disables the output driver.

Each bit of the bank is independently controlled.

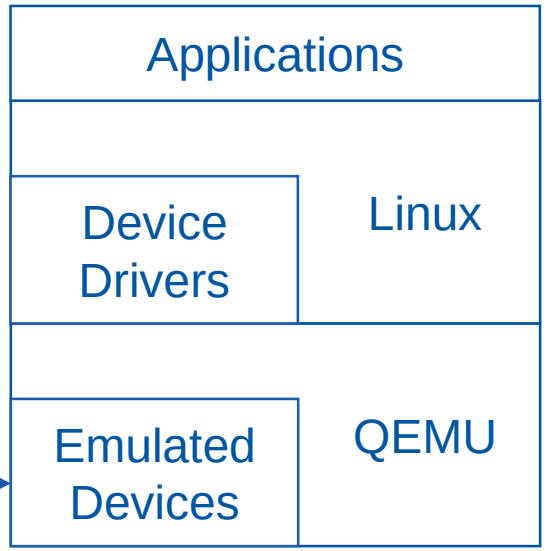
This register controls bank0, which corresponds to MIO[31:0].

Field Name	Bits	Type	Reset Value	Description
DIRECTION_0	31:0	rw	0x0	Direction mode 0: input 1: output Each bit configures the corresponding pin within the 32-bit bank NOTE: bits[8:7] of bank0 cannot be used as inputs. The DIRM bits can be set to 0, but reading DATA_RO does not reflect the input value. See the GPIO chapter for more information.

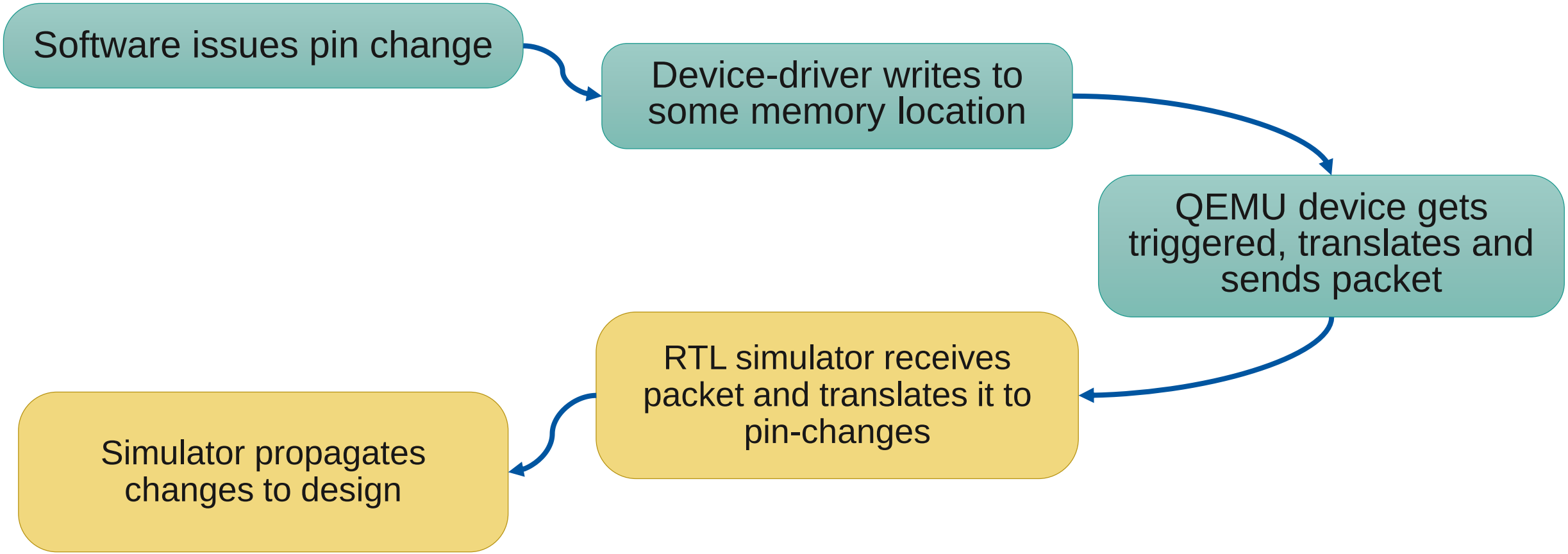
Xilinx Zynq-7000 SoC Technical Reference Manual Page 1338

QEMU GPIO Device

```
static uint64_t gpio_dir_prew(RegisterInfo *reg, uint64_t val)
{
    ZynqGPIOState *s = ZYNQ_GPIO(reg->opaque);
    uint32_t data = (uint32_t) val;
    uint32_t data_old = *(uint32_t *)reg->data;
    int bank = gpio_get_bank(reg->access->addr);
    int width = bank==1 ? 22 : 32;
    uint32_t mask = data ^ data_old; //all bits where something changed
    gpio_update_pins(s, bank, 0, width, mask,
                     (s->regs[R_GPIO_DATA_X(bank)]),(s->regs[R_GPIO_OEN_X(bank)]),
                     data,data_old);
    return val;
}
```



Overview of communication, simplified

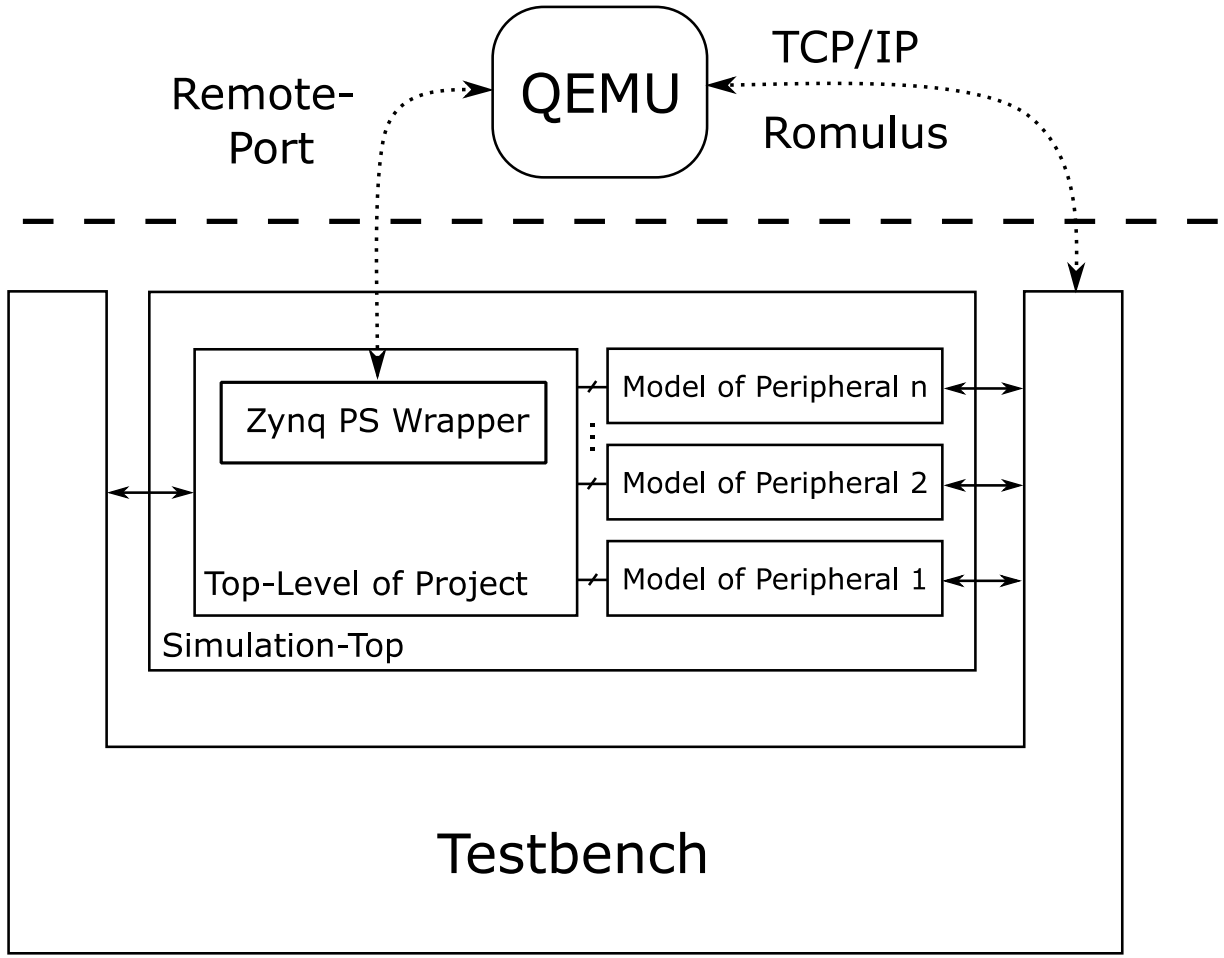


libsystemctlm-soc / remote-port

- **Communication between two simulators**
  - RTL: SystemC library for sending and receiving remote-port packets
  - QEMU: C counterpart, “Virtual QEMU device”
- **TLM semantics**
- **SystemC bridges, which translate packets from tlm to pin changes**
  - AXI, ACE, CHI, CXS, PCI
  - GPIO
- Provides **time synchronisation** between simulators
- Uses unix-socket or tcp

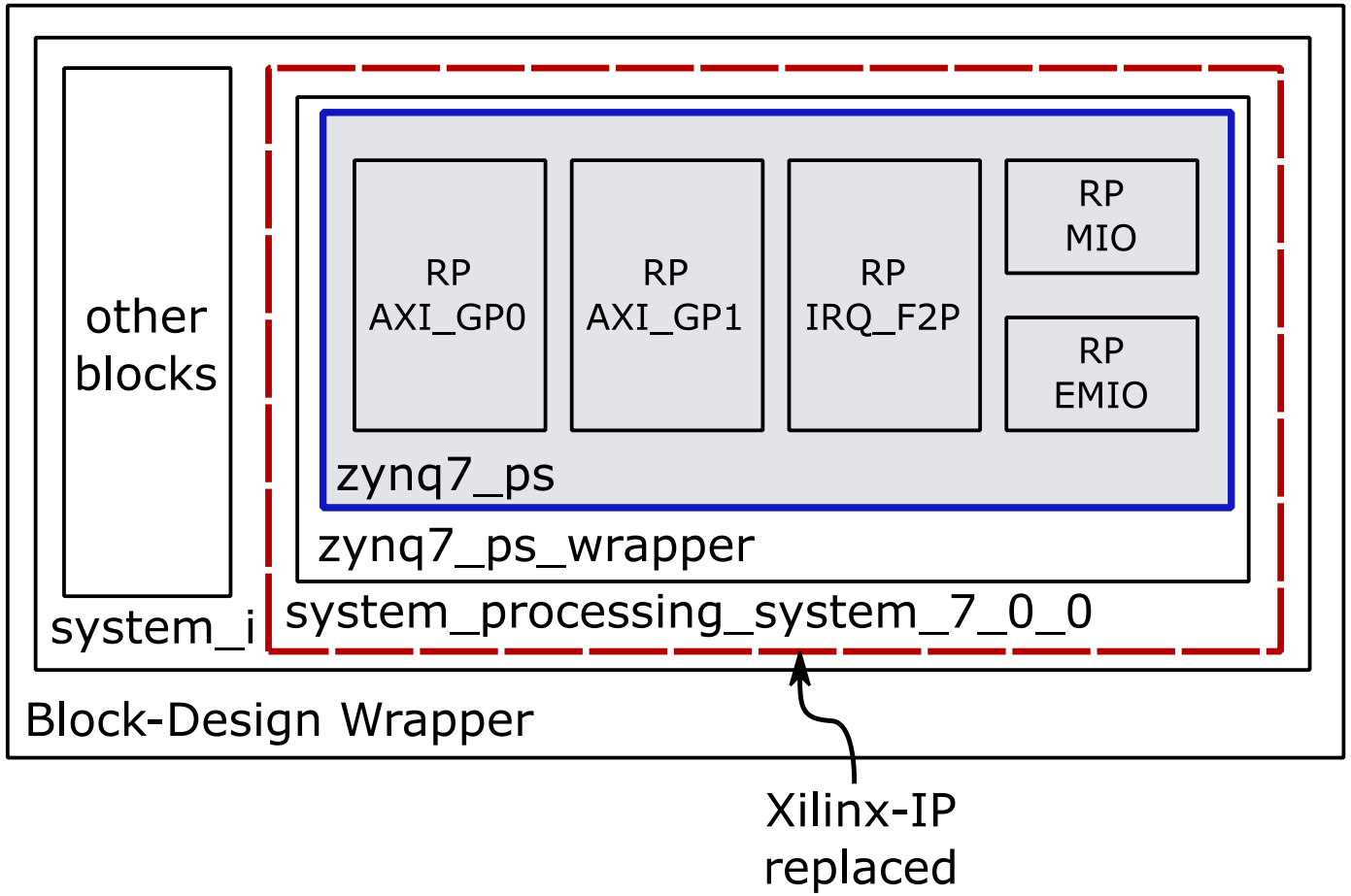
RTL-Simulation

- **Run simulation on Top-Level**
  - Exchange the Zynq component
- Implement Models of Peripherals
  - Our Case: ADCs, Temp Sensor, Measurement electronics
- **Current Objective: writing a system-level testbench using UVM**



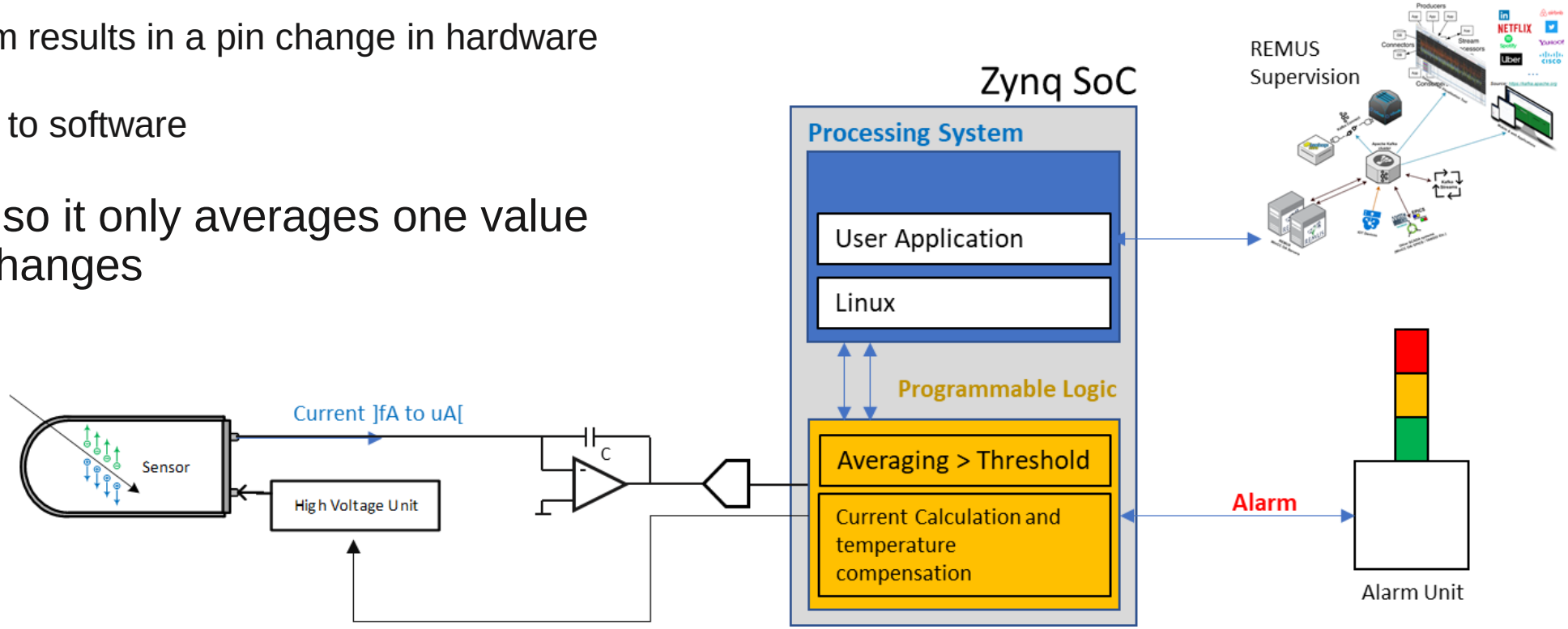
RTL-Simulation

- **Replacing instance system_proccessing_system7_0_0 with custom instance**
  - Exposes AXI busses GPIO and other connections to VHDL
  - Translates messages from remote-port to RTL pin changes and vice versa
- **Needs Mixed Language Simulator (SystemC, VHDL and/or Verilog)**
  - Developed with Questa



Demo Setup

- When average input current is **above** a threshold an **alarm is triggered**
  - This alarm results in a pin change in hardware
  - Also sent to software
- Configured so it only averages one value
  → instant changes



```
[2021-09-07:13:46:06.592: TID 3069267984 - Output Hardware Loop]        src/hw_loop.c:298:runHW
Loop(): Survived to here 5
[2021-09-07:13:46:06.594: TID 3069267984 - Output Hardware Loop]        src/hw_loop.c:321:runHW
Loop(): Survived to here 5.5
[2021-09-07:13:46:06.594: TID 3069267984 - Output Net Loop]     src/supervision_loop.c:252:supe
rvisionLoop(): Recieve network hwloop
[2021-09-07:13:46:06.594: TID 3069267984 - Output Net Loop]     src/supervision_loop.c:240:supe
rvisionLoop(): Polling hwloop
[2021-09-07:13:46:06.594: TID 3069267984 - Output Hardware Loop]        src/hw_loop.c:344:runHW
Loop(): Survived to here 6
[2021-09-07:13:46:06.595: TID 3069267984 - Output Hardware Loop]        src/hw_loop.c:361:runHW
Loop(): Survived to here 7
gpio out lsw mask: fffd data: fffd0002 bank 0
Bank: 0
Mask:     0x2
Data:     0x2
OEN:      0x2
DIR:      0x2
gpio out[1] set to 1 on bankoffset 1 with oe 1 and dir 1
Done Remote Packet
Last Time Sync =       1631022359967   kRaw          = -3.933907e-16  kBase          = 3.9339
06e-08
xADC Data
dieTemp = -2.730275e+02 vccInt  = 0.000000e+00  vccAux  = 0.000000e+00  vccBRAM = 0.000000e+00v
ccPInt = 0.000000e+00
vccPAux = 0.000000e+00  vccODDR = 0.000000e+00  vRefP   = 0.000000e+00  vRefN   = 0.000000e+00
--------------------------------------------------------------------------------
--------------------------------
Low voltage measurments:
minus 5v a    = -4.999168e+00   minus 15v a   = -1.499750e+01   minus 12v a   = -1.199996e+01 m
inus 2v5 a    = -2.499584e+00   plus 15v a    = 1.499750e+01
plus 5v zynq  = 4.999168e+00    plus 3v3 d    = 3.299011e+00    plus 5v d     = 4.999168e+00  p
lus 12v hv    = 1.199751e+01    plus 12v a    = 1.199751e+01
plus 5v a     = 4.999168e+00    vRef hv       = 4.999168e+00    vRef comp     = 2.499584e+00  v
Ref ADC Meas = 3.299011e+00
--------------------------------------------------------------------------------
--------------------------------
Alarms:
alert         = 0       alarm         = 0       specialAlarm   = 0       integralAlarm1 = 0    i
ntegralAlarm2 = 0
--------------------------------------------------------------------------------
--------------------------------
Intermediate measurments:
baseValueUncomp = 1.999998e-02  rawValueUncomp  = -1.999998e-10 baseValue100ms  = 1.999994e-02r
awValue100ms    = -1.999994e-10  adcWindowValue  = 2.401005e-01
--------------------------------------------------------------------------------
--------------------------------
[2021-09-07:13:46:06.598: TID 3069267984 - Output Hardware Loop]        src/hw_loop.c:262:runHW
Loop(): Survived to here 3
[2021-09-07:13:46:06.598: TID 3069267984 - Output Downstream]   src/downstream.c:431:createPLRe
setsAndTime(): Sync Clock
[2021-09-07:13:46:06.599: TID 3069267984 - Output Hardware Loop]        src/hw_loop.c:286:runHW
Loop(): Survived to here 4
```

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Wave - Default

/sim_top/ivc/chargePerSecond

Now

Cursor 1

Wave | Ranked | Structural

Now: 33,351,751,500 ns Delta: 2 | sim:/sim_top/ivc - Limited Visibility Region

Results

- **Working Co-Simulation** for the ZYNQ and furthermore the CMPU
- Currently used for debugging of additional features
- Simulation speed is only ~**30** times **slower** than **realtime** **@1MHz** for our design

Outlook

- Could likely be adjusted to **other projects**
- If SystemC Model exists, RTL part could be replaced to further increase simulation speed
- Other open source tools like **Verilator** could be interesting to further speed up simulation

Open Source Projects Used

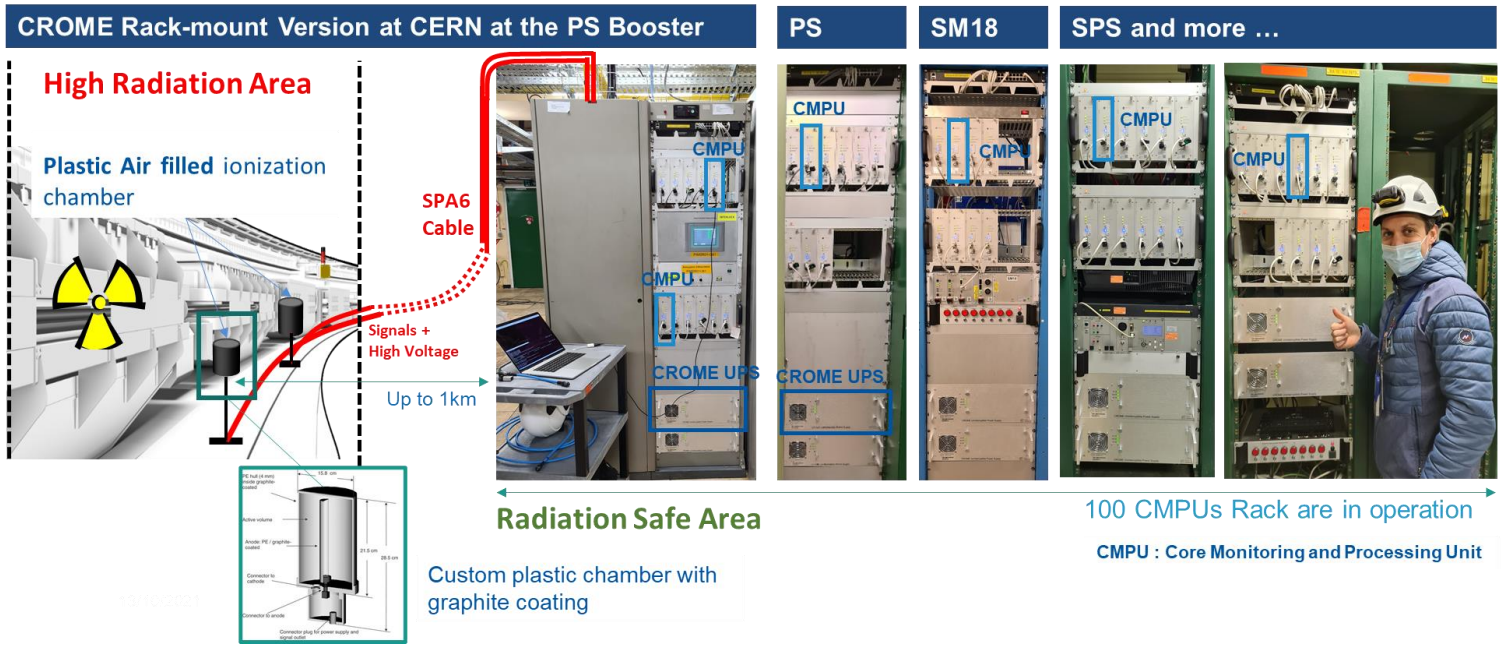
- Xilinx Qemu https://github.com/Xilinx/qemu
- Xilinx libsystemctlm-soc https://github.com/Xilinx/libsystemctlm-soc
- Xilinx qemu-devicetrees https://github.com/Xilinx/qemu-devicetrees
- **Rick Wertenbroek, CoSimulation https://blog.reds.ch/?p=1180**

www.cern.ch

CERN Radiation Monitoring Electronics (CROME)

Two configurations :

CROME Rack Version – High radiation Areas



CROME Bulk Version – Low radiation Areas