Zynq MPSoC for beam profile monitoring at the CERN accelerators

H. Sandberg (SY-BI-XEI), 2021-11-23, SoC Interest Group Meeting,
https://indico.cern.ch/event/1090205/

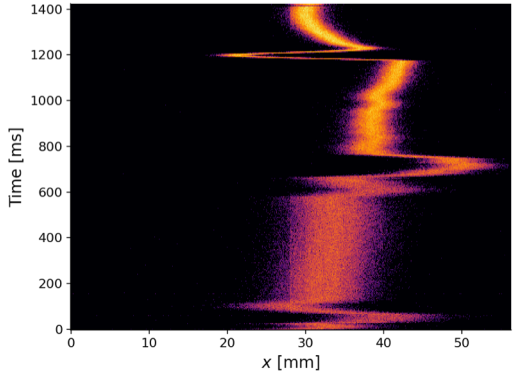
Beam profile monitoring - the “what” and “why”

Short answer:

- Smaller beam “size” -> higher luminosity in LHC

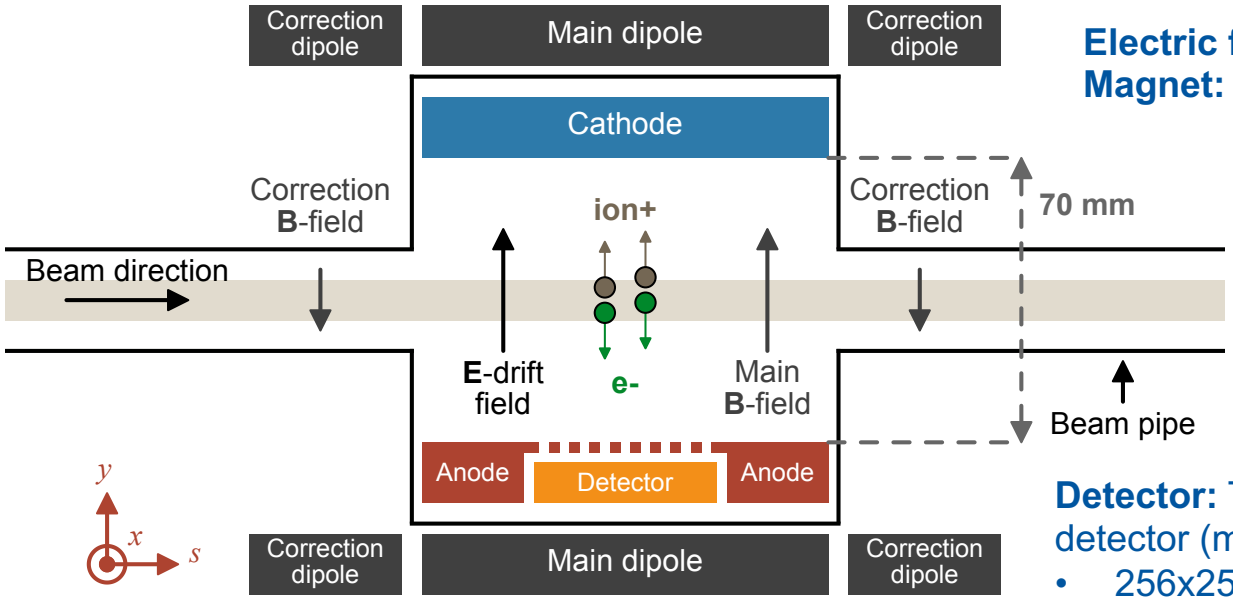
Longer answer:

- Observability important for operators: “If you can see it you can tune it”
- Ideally: the monitoring should not affect the beam -> non-invasive
- Beam emittance can be inferred from the beam profile



Beam gas ionization (BGI) profile monitor

Measures the transverse beam profile from the distribution of ionization electrons



Electric field: 280 kV/m
Magnet: 0.2 T

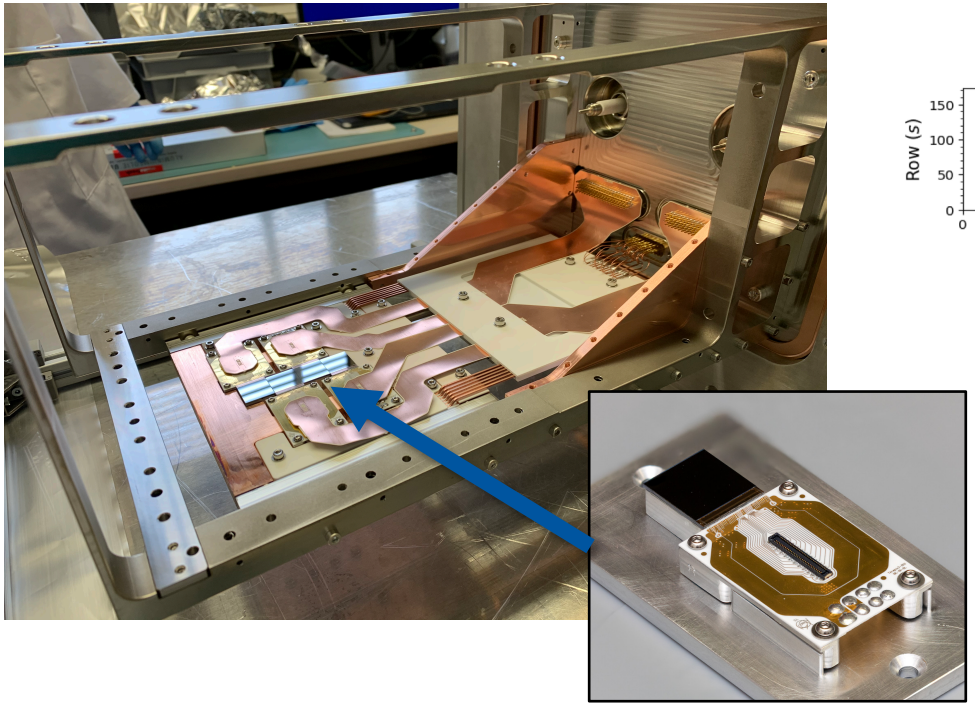
Detector: Timepix3 hybrid pixel detector (medipix.web.cern.ch)

- 256x256 pixels, 55 µm pitch
- 1.5625 ns time resolution

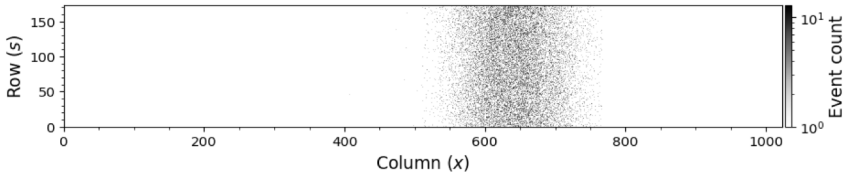
More info on: bgi.web.cern.ch

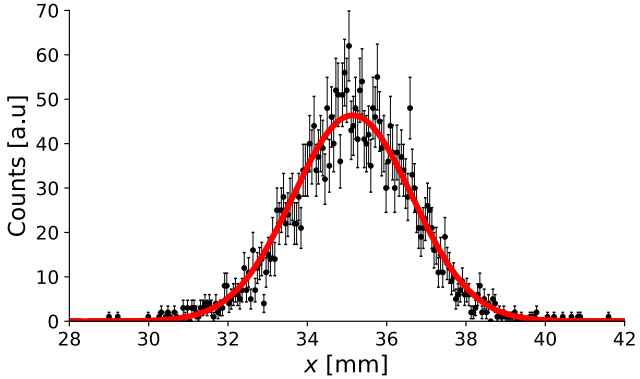
Beam profile monitoring with Timepix3

Timepix3 used inside the ultra-high vacuum of the PS, ~35 mm below the beam

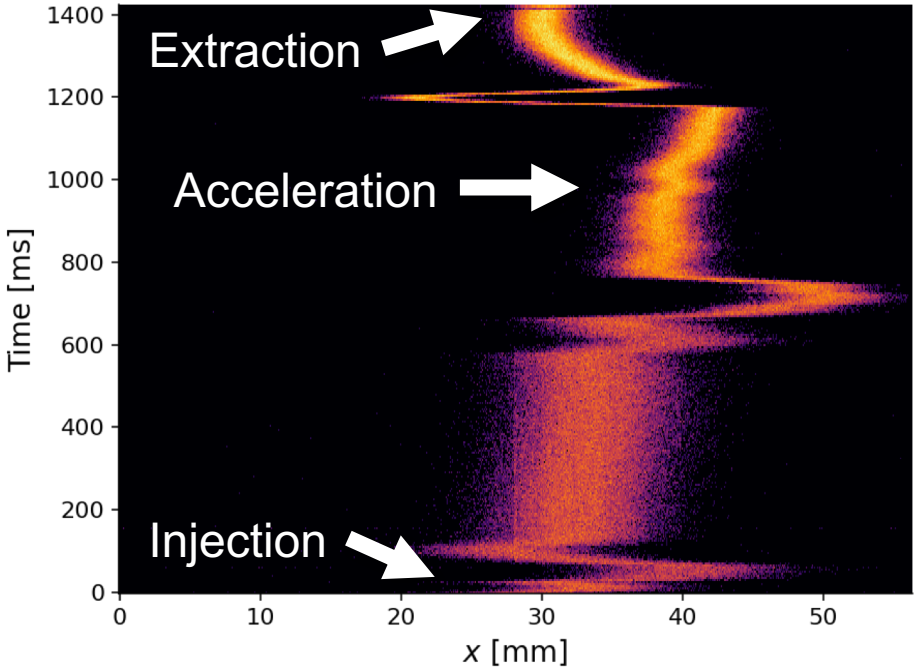


4x Timepix3 detectors side-by-side





Beam profiles in an accelerator cycle



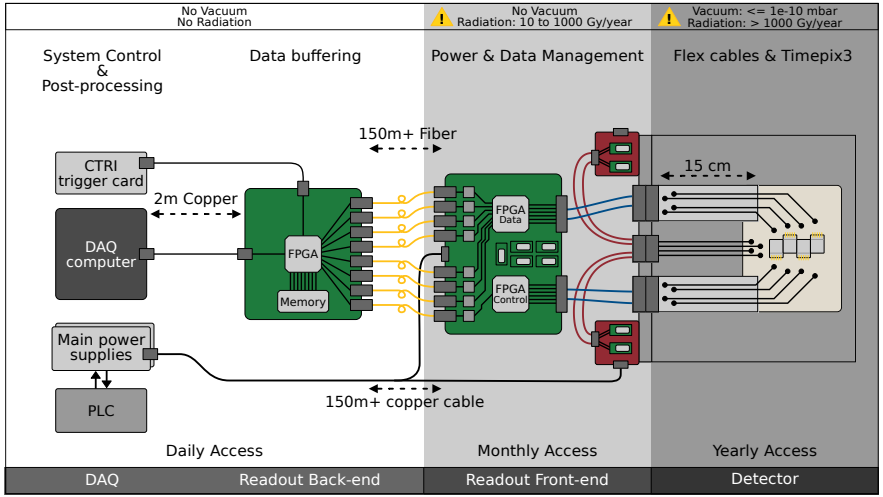
- Each time-slice here is a beam profile
- 2 ms integration time per profile
- 700 profiles in total in the cycle

Time-resolved non-invasive beam profile monitoring

Current readout system

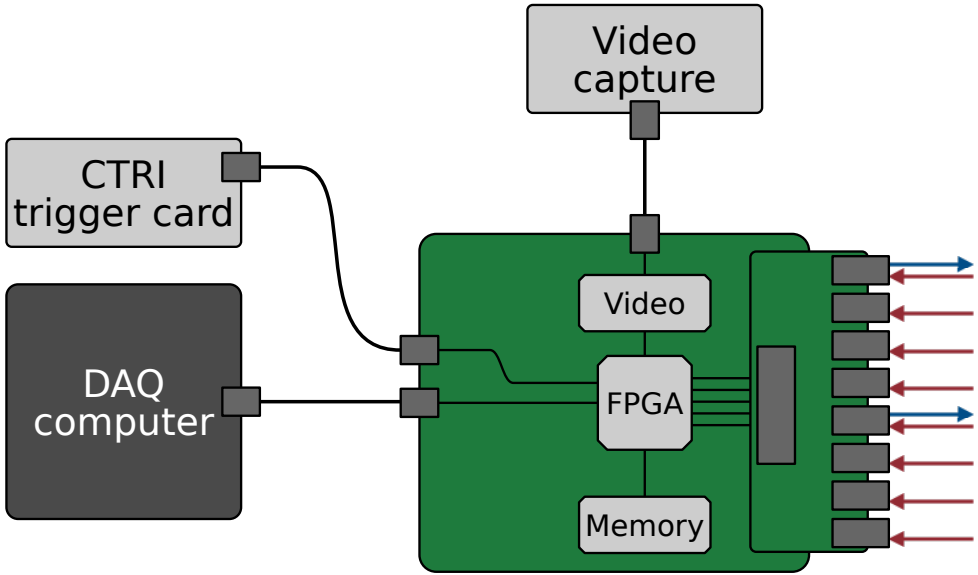
Built around EP-ESE components:

- Timepix3
- GBTx
- GBT-SCA
- FEASTMP
- VTRx
- GBT-FPGA



- The front-end FPGAs send commands to the Timepix3 detectors and synchronize the event packets that are produced
- The packets are routed to 8 optical GBT-links to the back-end FPGA
- The back-end FPGA process and store the events it receives over the links in a buffer memory that is read out by the computer
- A PLC controls all the power supplies and cooling for the in-vacuum Timepix3

Current back-end FPGA-only solution



- VC707 board
  - Virtex-7 FPGA
  - 1 GB DDR3
  - HDMI output
  - 1G ethernet
- 10-port SFP FMC mezzanine
- Beam profile construction done in logic
- Limited event filtering
- Soft-core RISC-V for simple monitoring and control

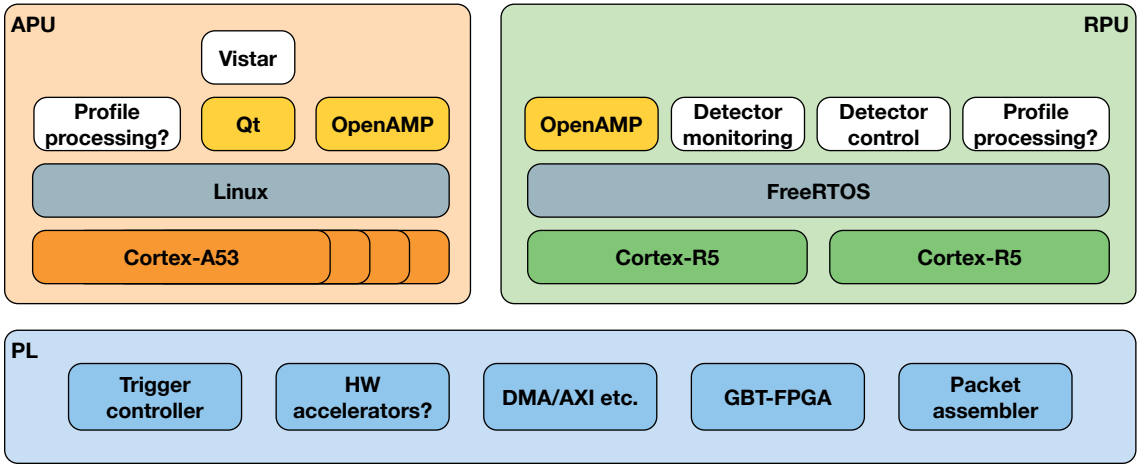
Motivation for SoC

- We will upgrade the SPS with the same Timepix3 based profile monitor
- Current FPGA-only based back-end is “not enough”
- Use software for processing of data
  - More event filtering (beam losses vs ionization electrons)
  - Lots of interesting libraries/algorithms out there, e.g. DBSCAN
  - Aim to provide real-time bunch-by-bunch measurements
- Future-proofing
  - Take advantage of both hardware & software expertise
  - SoC seems to be the direction
  - Long-term: remove computer and run it all on the SoC!

New MPSoC based readout

- ZCU102 board
  - Zynq UltraScale+ MPSoC
  - 4+0.5 GB DDR4
  - HDMI/DP output
  - 1G ethernet (PS)
  - 4 SFP
  - Other interesting features:
    - PCIe
    - SATA
    - USB3
- 4-port SFP FMC mezzanine (EDA-04252)

MPSoC readout architecture



APU: application processing unit
RPU: real-time processing unit
PL: programmable logic

- APU runs Linux with high-level applications (communication, vistar, etc)
- RPU runs time-critical detector monitoring and control (lock-step mode)
- OpenAMP for RPU <-> APU communication
- TBD: Profile processing in either APU, RPU or both
- PL has hardware interfaces, trigger inputs, data buffers, etc.

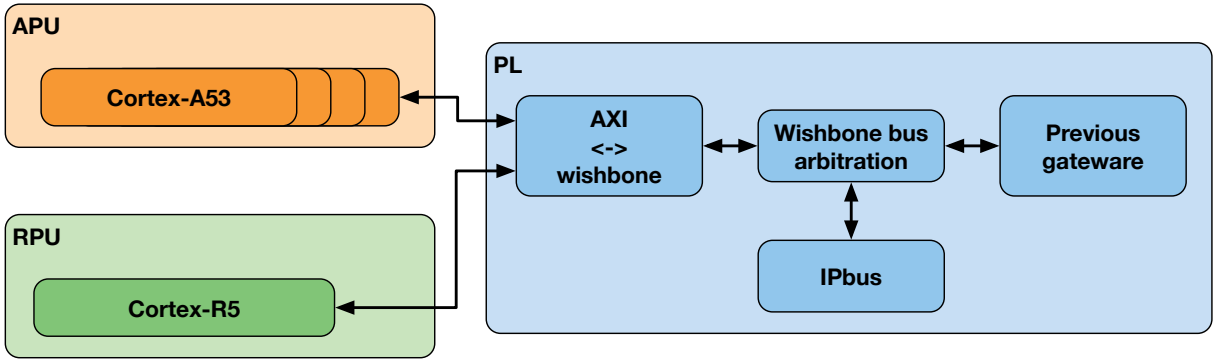
Protocol between SoC and computer?

Objective: transfer commands and data with *reasonable* latency at ~1 Hz repetition rate over 1G Ethernet

- ROMULUSlib
  - Lightweight with get/set/streaming/history capabilities
  - In contact with CROME team to evaluate this for our application
- gRPC
  - Open source and well documented
  - Yocto recipe available -> to be tested
  - Integration with operational computers at CERN?
- Ironman
  - “IPbus on SoC” -> drop-in replacement
  - IPbus is *only* get/set

Current status

- FPGA-only gateware up and running on MPSoC
- PL-IPbus connection still available and working as before
- Processors also have access to Wishbone bus and can operate in parallel with computer



Next steps:

- Write RPU firmware and APU applications
- Create dedicated interface between PL and PS for faster data transfer

Questions and comments?