MEASURING SINGLE EVENT UPSET CROSS SECTIONS AND OTHER RADIATION EFFECTS IN READOUT ELECTRONICS FOR THE ATLAS INNER TRACKER UPRGADE

(LHCC Poster Session – Online, November 18, 2021)

Introduction

- ATLAS Inner Tracker (ITk) Upgrade: all-silicon replacement of ATLAS's existing inner tracker for the High-Luminosity LHC (HL-LHC) [1] – enhanced granularity and radiation hardness for harsh HL-LHC conditions
- For strip modules (localized detector units), the readout electronics utilize **ATLAS Binary Chips (ABCs)**, which are responsible to digitizing 256 channels and performing cluster finding
- ASICs, like ABCs, are susceptible to **radiation effects which could impact performance** – important to understand these effects in order to maintain data quality and ensure reliable operation of the ITk

Single Event Upsets and the ABCStar

- **Single event upsets (SEUs)**: change of state (0→1 or 1→0) in memory/logic due to an electrical disturbance from **radiation**, resulting in **wrong data** and **misconfiguration**
- SEUs are an *integrated* effect: more fluence/dose means more SEUs

- ABCStars are the production version of ABC, with two subversions: V0 and V1
- Primary change: V1 has fully implemented **triple modular redundancy (TMR)** [2] of all registers – protects memory via *voting*

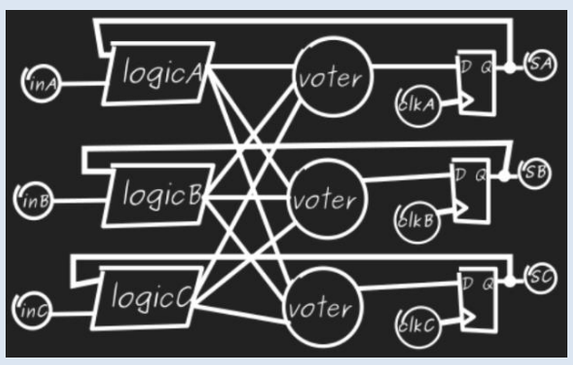
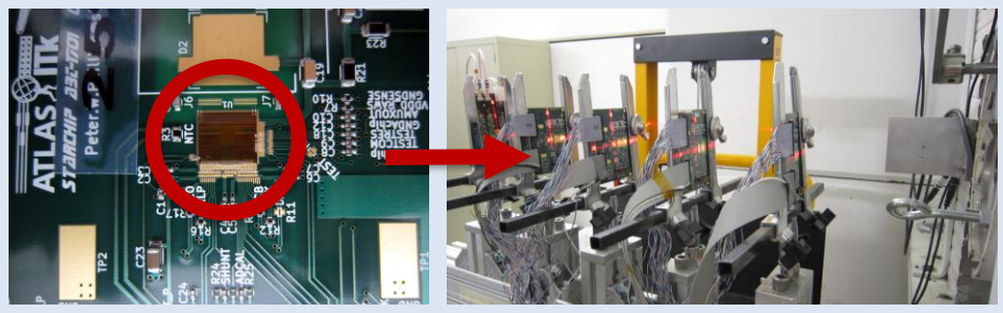


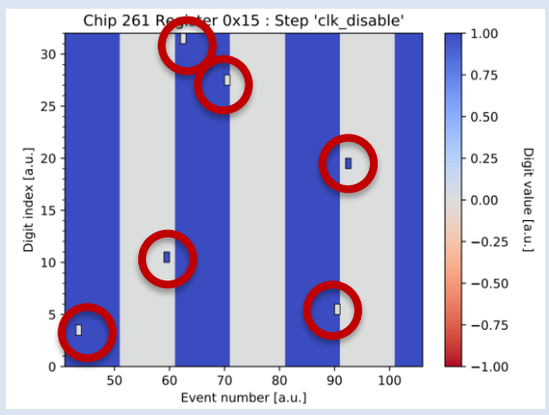
Image obtained from Slide 32 of S. Biereigel's and S. Kulis' presentation, "How to Design Highly Reliable Digital Electronics" (2019, Leipzig)

Experimental Setup



- Two testbeams were conducted at TRIUMF using 480 MeV protons in August & December 2020, each with four chips
- ASICs (**circled**) were mounted to Single Chip Boards (top-left) and mounted in beam (top-right), four at a time
- ASICs were connected to Nexys Video FPGA boards and read out using the ITk Strips DAQ software on a single PC

Results: Register Read Packet SEU Cross Section



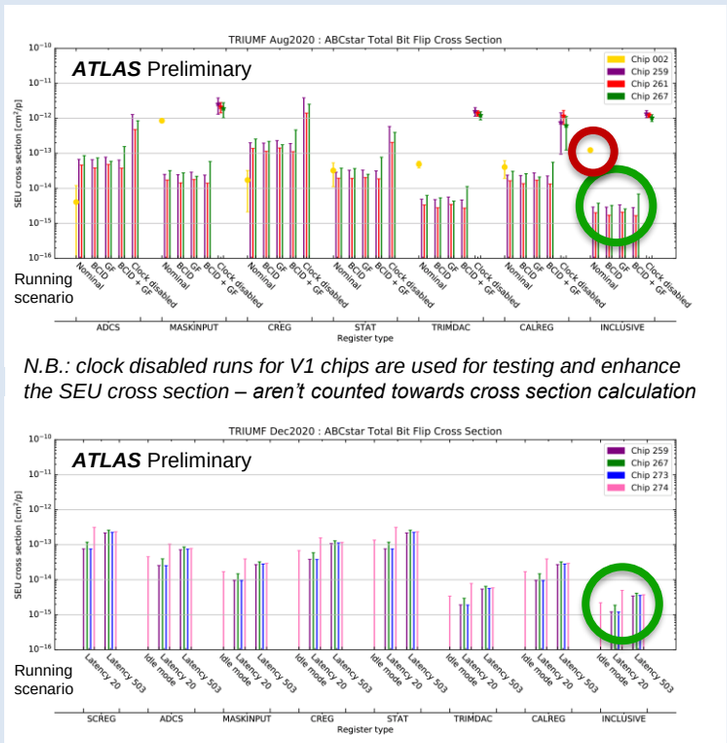
N.B.: while Chip 261 is a V1 chip, the above is taken from a clock disabled run, hence the SEUs

$$\sigma_{\mathrm{SEU}} = \frac{n_{0\to1} + n_{1\to0}}{\int d\phi}$$

SEU cross section formula

- ABCStar registers store configuration and counters
- By filling the registers in a predictable way and comparing this to what is measured, we can identify SEUs (e.g., see upper-left plot: **red circles** indicate SEUs)
- N.B.: only *one* ABCStarV0 chip (upper-right: **Chip 002**) was tested between both campaigns – *all* others are V1

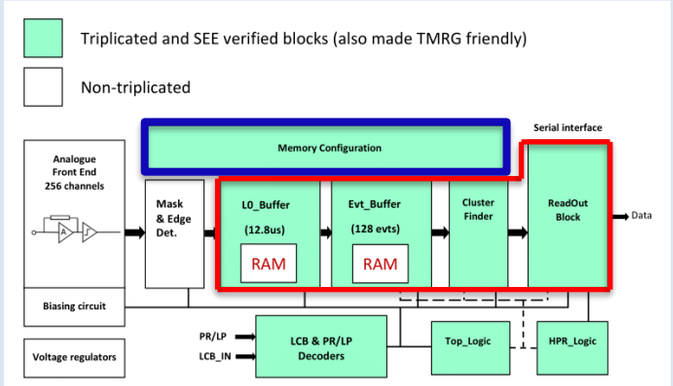
- SEU cross section is calculated by summing the numbers of 0→1 ($n_{0\to1}$) and 1→0 ($n_{1\to0}$) bit flips and normalizing to the integrated fluence ($\int d\phi$) between write/read times of register
- Cross sections per chip per running scenario per register type shown to the right (top: August; bottom: December)
  - Lines **without** datapoints are 95% upper confidence bounds (i.e., no SEUs)
- Cross section for the V0 chip (**red circle**) is **(1.24 ± 0.12) × 10^{-13} cm^2/proton**; V1 chips (**green circles**) saw **no SEUs**: 95% upper confidence bound of **1.17 × 10^{-16} cm^2/proton**– **TMR works!**



N.B.: clock disabled runs for V1 chips are used for testing and enhance the SEU cross section – aren't counted towards cross section calculation

Results: Physics Packet SEU Cross Section

- Level-0 trigger: front-end hit data in the L0Buffer is transferred to the EventBuffer, grouped into clusters, and returned as "physics" packets
- This pipeline (**red**) is susceptible to SEUs like the register memory (**blue**)

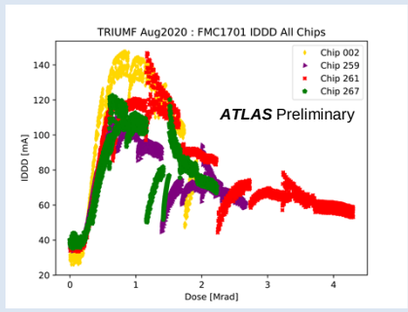


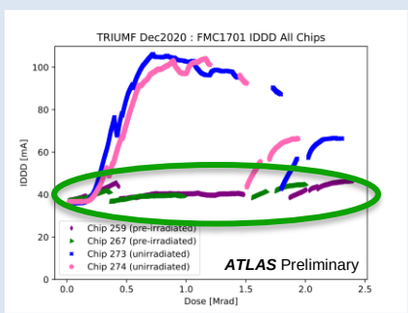
- SEU cross section for errors in physics packets is estimated in same was as for register reads: L0Buffer is filled in a predictable way (all 0's, all 1's, or a "realistic" pattern) and read out repeatedly – the returned clusters may be compared to the expected clusters

- Cross sections are found to be **(3.69 ± 0.03) × 10^{-12} cm^2/proton** and **(5.32 ± 0.02) × 10^{-12} cm^2/proton** for V0 and V1 chips, respectively
- Assuming hadron fluxes of 10^7 hadrons/cm^2/s and readout durations of 10 μs at the HL-LHC, this yields 10^{-10} errors/trigger/ABCStar
- With 230K ABCStars and a 1 MHz trigger rate, this yields **20 errors/s** – **insignificant** in comparison to the noise occupancy (10^{-4} to 10^{-3} of all channels) and so **negligible** impact on data quality

Results: Digital Current Measurements

- Measurements of the digital (IDDD) current for each chip were performed
- From the prototype version of the ABCStar, the ABC130 [3], the digital current increases by 100% near 1 Mrad dose: "Total Ionizing Dose (TID) Bump"
  - Leads to **detector cooling problems** at runtime
- **Mitigation strategy**: pre-irradiate ASICs past the TID bump
- Chips irradiated in August (top: **259** and **267**) do not see IDDD increase when operated in December (bottom) – **pre-irradiation works!**





References

[1] The ATLAS Collaboration, "Technical Design Report for the ATLAS Inner Tracker Strip Detector", Tech. Rep. CERN-LHCC-2017-005, ATLAS-TDR-025, CERN, 2017.
[2] S. Kulis, *Single Event Effects mitigation with TMRG Tool*, JINST **12** (2017) C01082.
[3] L. Poley, C. Sawyer, *et al.*, *The ABC130 barrel module prototyping programme for the ATLAS strip tracker*, JINST **15** (2020) P09004.

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