

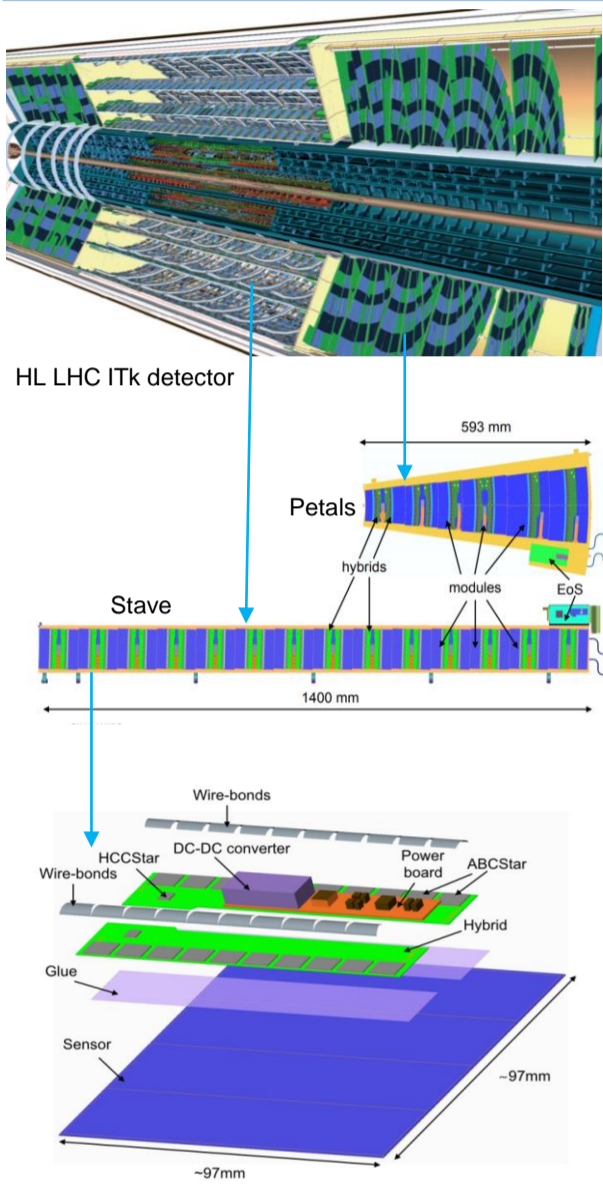
Thermal and Electrical Performance of ATLAS ITk Strip Module Testing Setup at BNL



Introduction

- The new all Silicon, **ATLAS Inner Tracker (ITk)** will replace the current ATLAS inner Detector for the High Luminosity LHC.
- HL-LHC** : nominal luminosity $\mathcal{L}_{\text{peak}} \sim 7 \cdot 10^{34} \text{ s}^{-1} \text{ cm}^{-2}$, $\mathcal{L}_{\text{integrated}} \sim 3000(4000) \text{ fb}^{-1}$ and Pileup of ~ 200 per 25 ns.
- The ITk is made up of barrels and endcaps centered around the interaction point, covering the pseudo rapidity range from -4 to +4

HL-LHC ATLAS ITk Detector (1)



ITk Pixel Detector

- 5-barrel layers with inclined sensors
- End-Cap system with individually located rings

ITk Strip Detector

- 4-barrel layers
- End-Cap(EC) system with 6 rings on both sides

ITk Strip Staves & Petals

- Staves (Barrel) and Petals (End-cap) are the support structure for the modules.
- It hosts the common electrical, optical connections and cooling services.
- 28 Barrel modules on each stave (14 modules per side)
- 18 End-Caps modules on each petal (9 modules per side, R0-R5)

ITk Strip Modules

- Building blocks of the ITk strip detector.
- Consists of the **sensor**, one (for long strip, LS) or two (for short strip, SS) PCBs called **Hybrid** and one **Power board**.
- The hybrid hosts the readout ASICs: the **ABCStar** and the **HCCStar**.

Thermal & Electrical Performance (3)

Thermal Performance

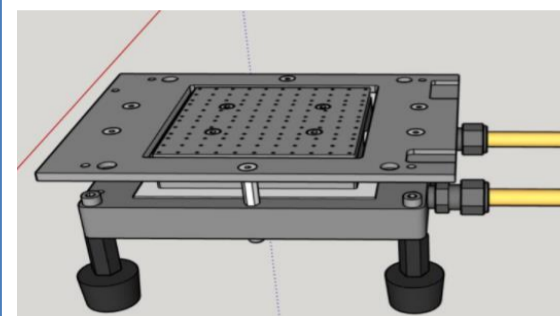


Fig: Drawing of the cooling setup on which modules are held.

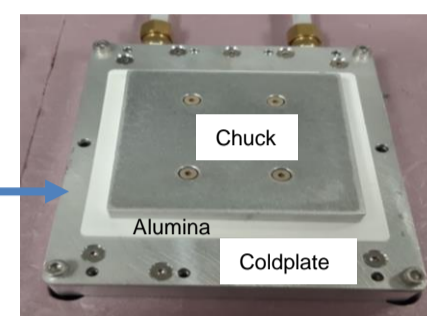


Fig: Image of a cooling setup

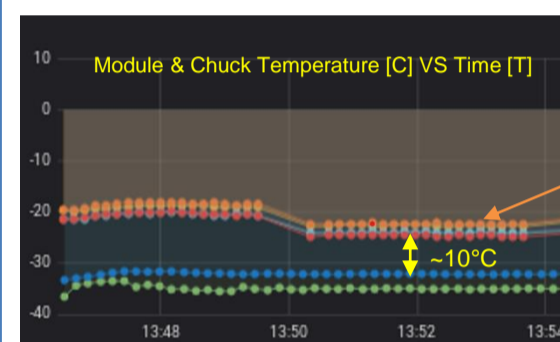


Fig: Grafana plot for 4 hybrids and chuck temperatures.

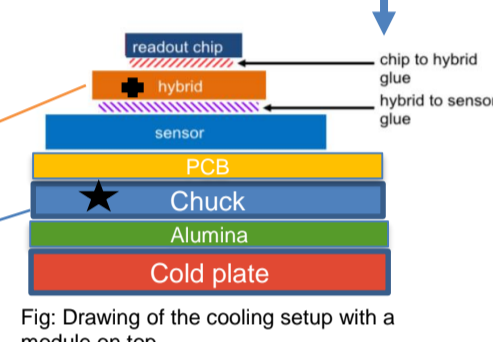


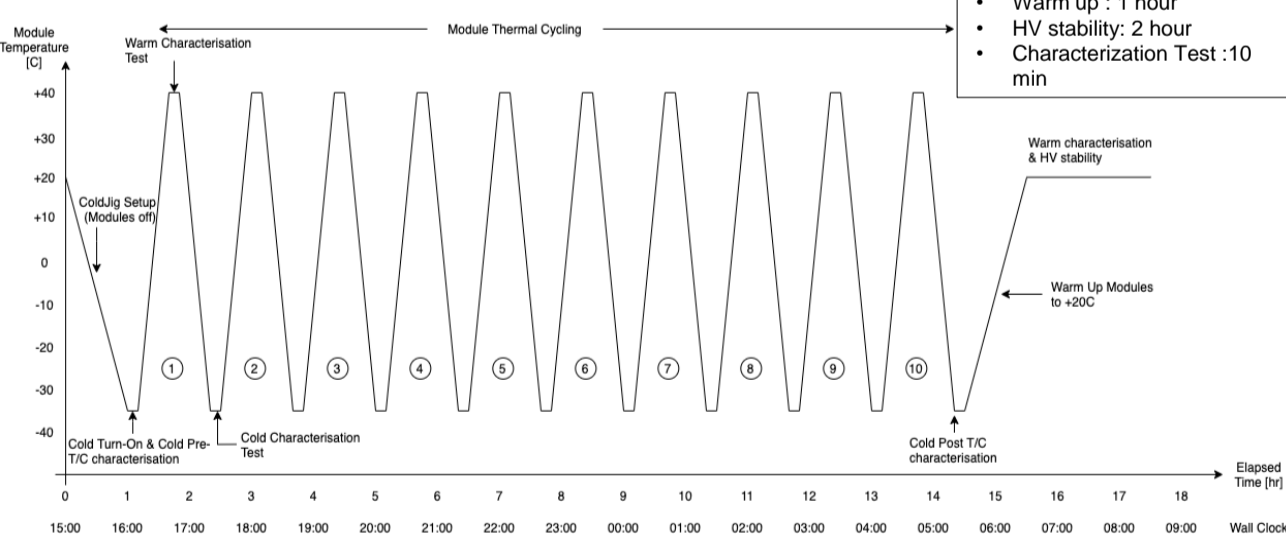
Fig: Drawing of the cooling setup with a module on top

- We have been able to thermal cycle modules from +40°C to -35°C and do DAQ scans at each step.
- When cold ($\sim -35^\circ\text{C}$ chiller temperature), we observed that the hybrid is $\sim 10^\circ\text{C}$ warmer than the chuck.

Module QA/QC Requirements & Testing Setup (2)

ITk Strips Module QC Thermal Cycle Sequence

04 May 2021



- Timing Assumptions**
- Cool down : 1 hour
 - Warm up : 1 hour
 - HV stability: 2 hour
 - Characterization Test : 10 min

- Between Module production and Stave assembly, each Module undergoes electrical and thermal quality control (QC) testing.
- Each module will be thermal-cycled 10 times from -35 °C to +40 °C to -35 °C, as measured by the Hybrid NTC.
- At each temperature change, **DAQ tests (Strobe Delay, 3-point gain, Noise Occupancy, IV scan)** are performed to evaluate the module.
- Modules that don't qualify with these tests are handled accordingly and tested again if possible after repair.

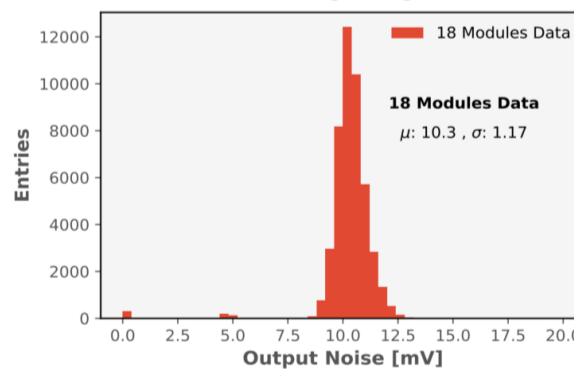
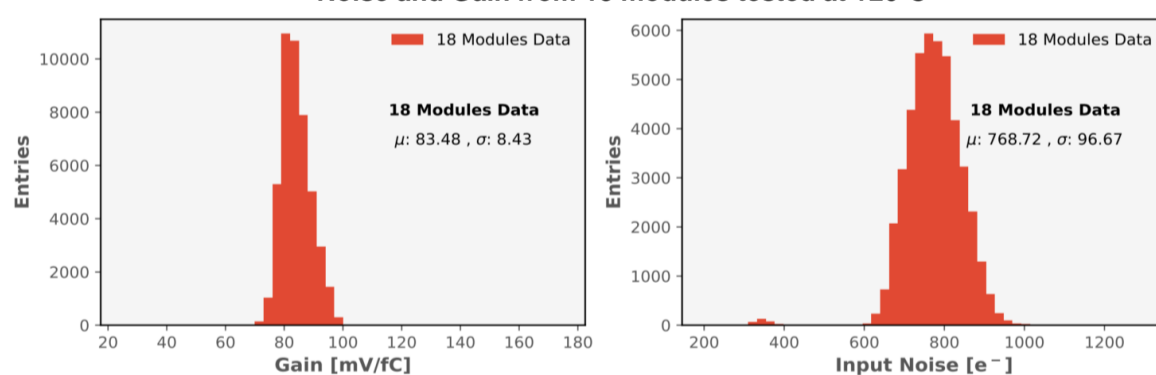


US Thermal Cycling Setup (Coldbox)

- It has chucks [0:3], modules are tightly screwed down through the frame for a good thermal contact.
- Each chuck has an 10k NTC and chuck 1,2 have SHT85s placed strategically to probe the coldest air in the box.
- 2 floating 10k NTCs and an Airflow meter to measure the ambient air temperature and airflow, respectively.
- A Python based software for control and readout.

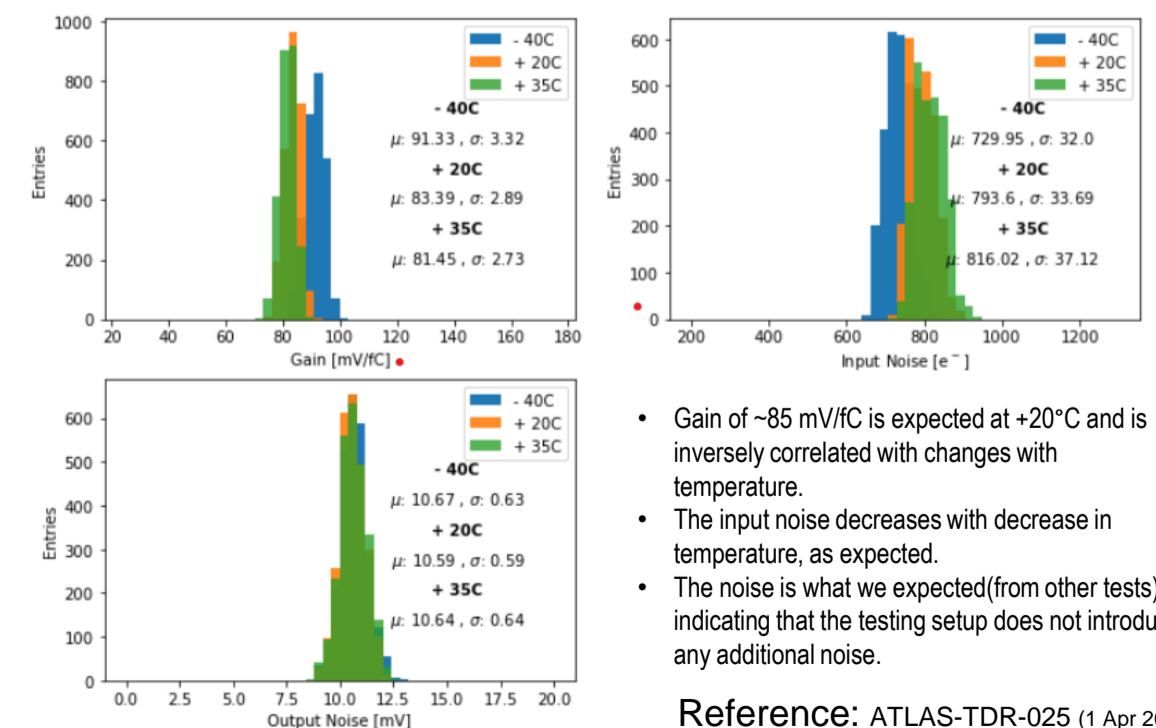
Electrical Performance

Noise and Gain from 18 modules tested at +20°C



- For testing purpose, response curve is used to measure the response of the front end (in mV or DAC counts) to the injection of a calibration charge.
- The response curve is then used to calculate the output noise and VT50 (mark is where the hit occupancy drops to 0.5).
- Gain, Input noise and output noise are used for the characterization of a module.

Single Module Tested at Different Temperatures



- Gain of $\sim 85 \text{ mV/fC}$ is expected at +20°C and is inversely correlated with changes with temperature.
- The input noise decreases with decrease in temperature, as expected.
- The noise is what we expected (from other tests) indicating that the testing setup does not introduce any additional noise.

Reference: ATLAS-TDR-025 (1 Apr 2017)