R&D on Upgrades for the ATLAS Muon Detector and Trigger Systems

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Research Experience

PostDoc, Project Scientist (UC Irvine)

- Trigger algorithm & Firmware development for the Phase-2 MDT Trigger Processor
- Design and performance studies of the Phase-2 Muon Trigger architecture
- NSW Micromegas Electronics Integration and Commissioning
- NSW Micromegas Wedges Validation and testing with cosmic rays
- Integration and Commissioning of the NSW in the ATLAS experiment

- Muon Run Coordinator
- Member of the Muon Steering Group
- Member of the NSW Steering Group
- NSW Integration & Commissioning Coordinator
- NSW Electronics Integration Coordinator

ATLAS NSW & MUON, TDAQ

PhD (NTU Athens & BNL)

- Organisation and operation of NSW Micromegas test beams
- Design and performance studies of NSW Micromegas detectors
- ATLAS MUON DCS development and maintenance

- Muon Run Coordinator
- CSC DCS Coordinator
- CSC Operation Contact Person

ATLAS NSW & MUON, RD51

Undergrad (NTU Athens)

- HV stability studies of resistive-strip Micromegas (MM) under neutron irradiation
- Performance study of resistive-strip Micromegas (MM) in hadron beams

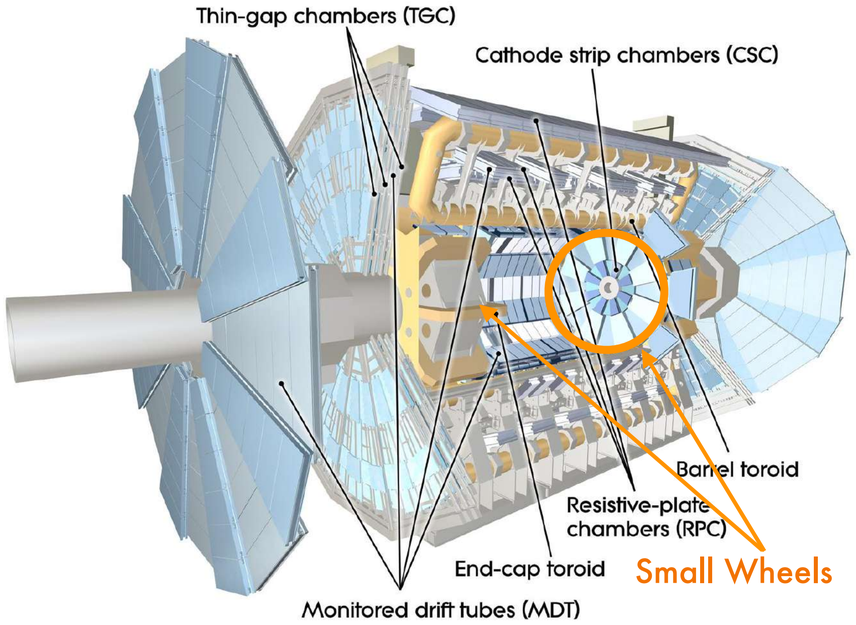
ATLAS NSW

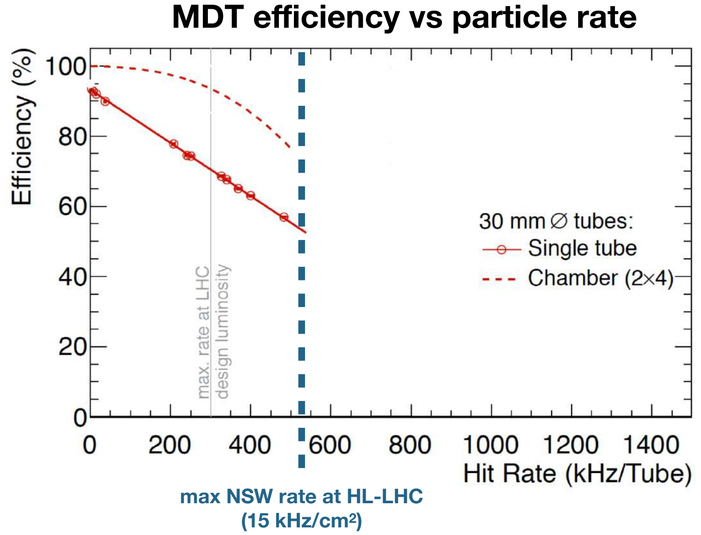
2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021

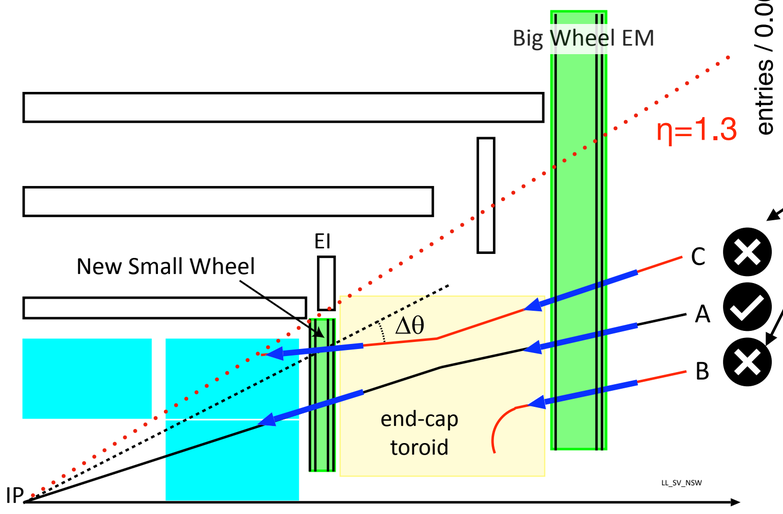
The New Small Wheel Upgrade of the ATLAS Muon System

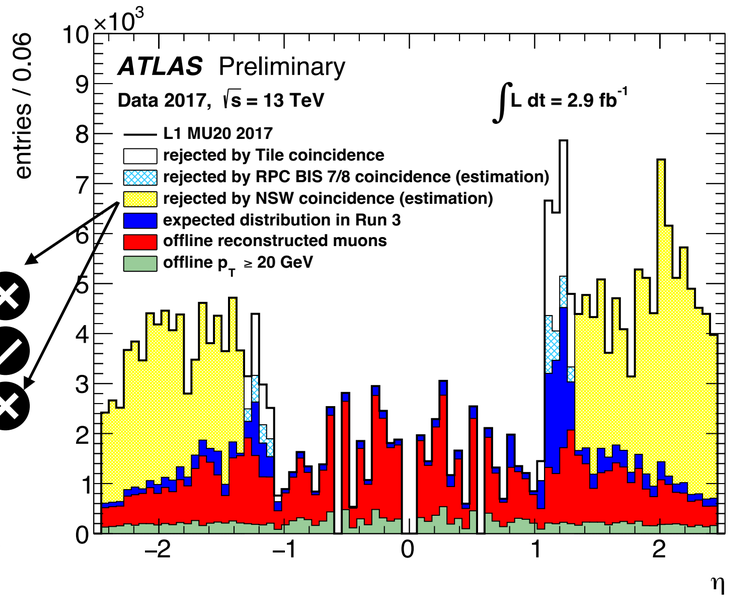
Motivation for the ATLAS New Small Wheel Upgrade Project (NSW)

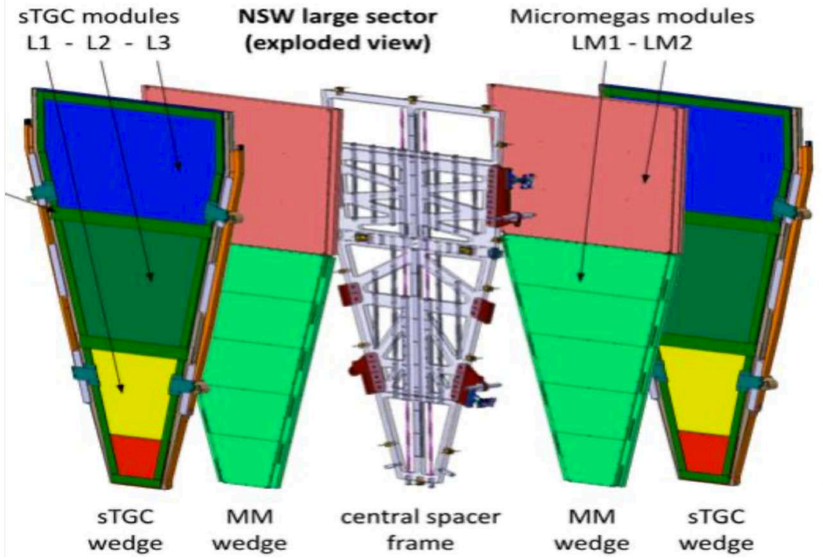
1. **Performance limitations of the current detectors (CSC, MDT, TGC) at increased particle rated**
   - Replace with new detectors able to cope with high particle rates (<15kHz/cm²)
2. **Endcap Muon trigger rate will exceed the available bandwidth (currently based only on Big Wheel, fakes triggers for |η|>1.3)**
   - Include the small wheel in the muon trigger decision to keep the trigger rate under control (<20kHz)







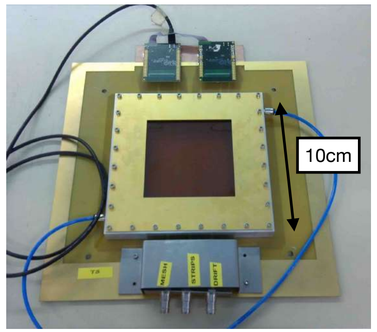




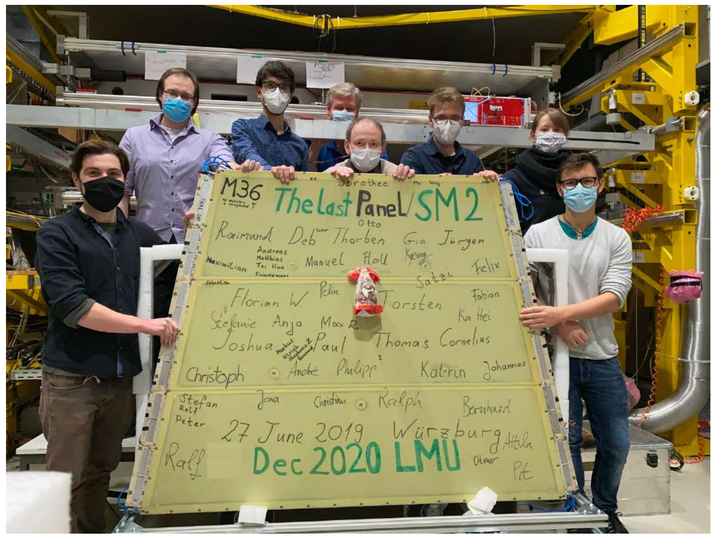
NSW Micromegas Detectors (MM)

- **16 sectors per wheel with 8 MM detection layers per sector**
  - >1000 m^2 of detection surface
- **First time application in such large scale and at high rate environment**
  - Huge R&D effort for optimising the detector properties and performance (2007-2016)

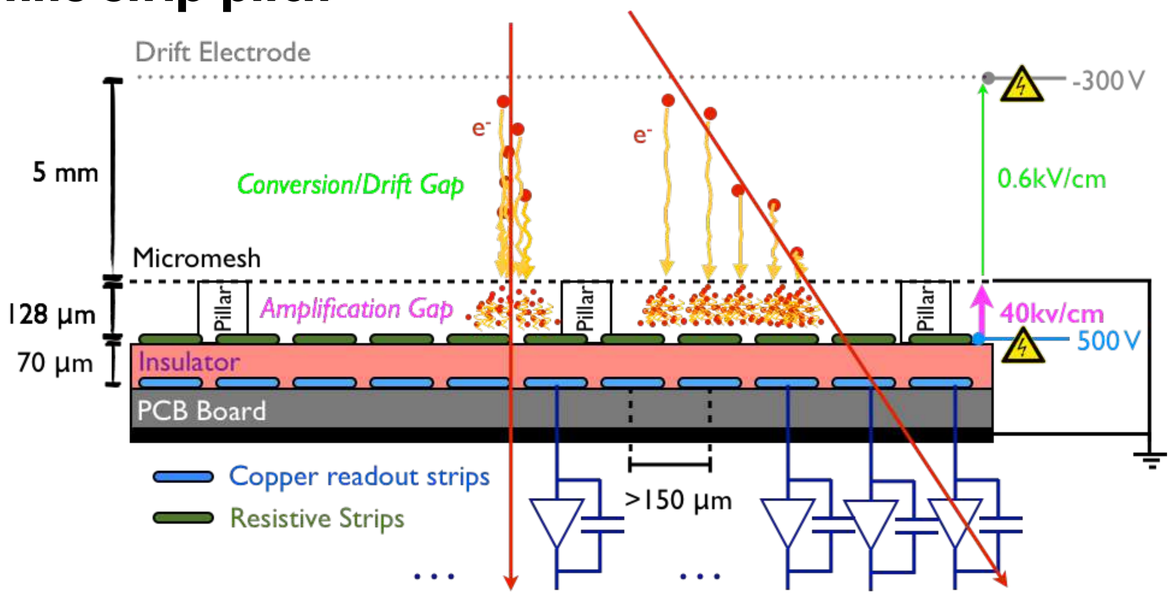
2010



2020



- **Novel detector technology based on MPGD, first time used in such a large scale and at high-rate environment**
  - Asymmetric drift and amplification regions
    - Fast ion evacuation and high amplification achieved with reasonable voltages
  - An additional layer of resistive strips makes the detector tolerable to discharges (high-rate capable)
- **Excellent spatial resolution (0.1mm) due to the very fine strip pitch**



NSW MM R&D - Test Beams

- **Contributed in the design, set-up and operation of the experimental apparatuses including scintillator trigger, detectors, front-end electronics, DAQ/DCS systems and services**
- **Co-Developer and maintainer of the Offline reconstruction software recoMM**
  - Used widely within the RD51 collaboration for data acquired with MM and GEM detectors using APV25 FE via the SRS system
- **Test-beam campaigns have been essential to prove that the MM technology fulfils the ATLAS requirements for the NSW and to optimise the detector's design and performance**

MM detector assembly

Typical NSW MM test-beam apparatus

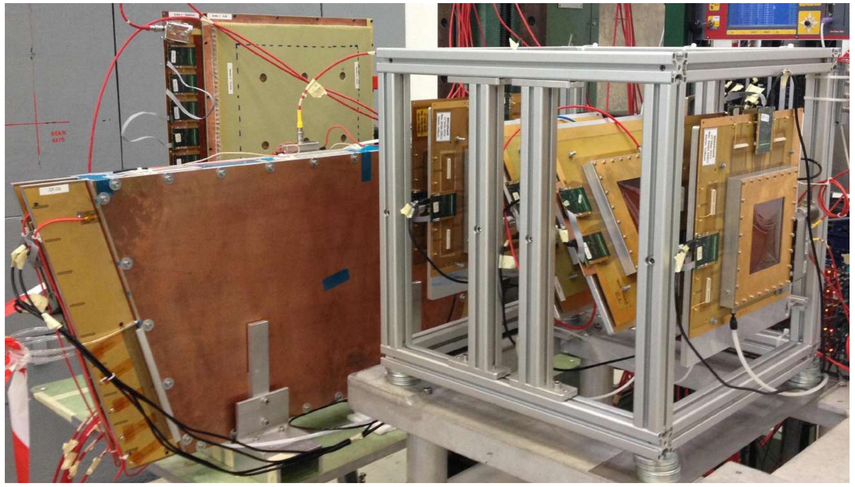
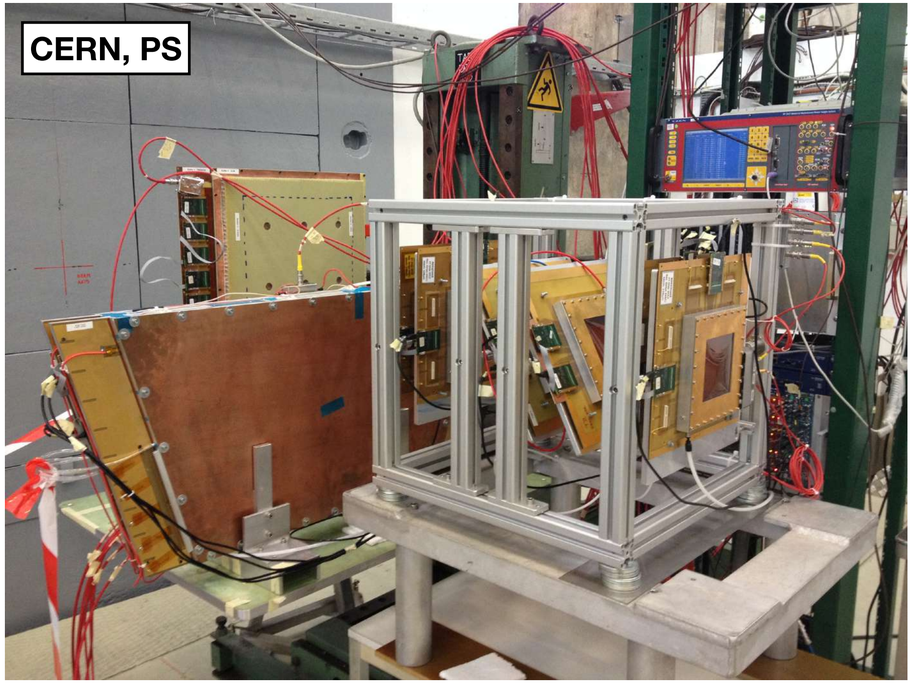


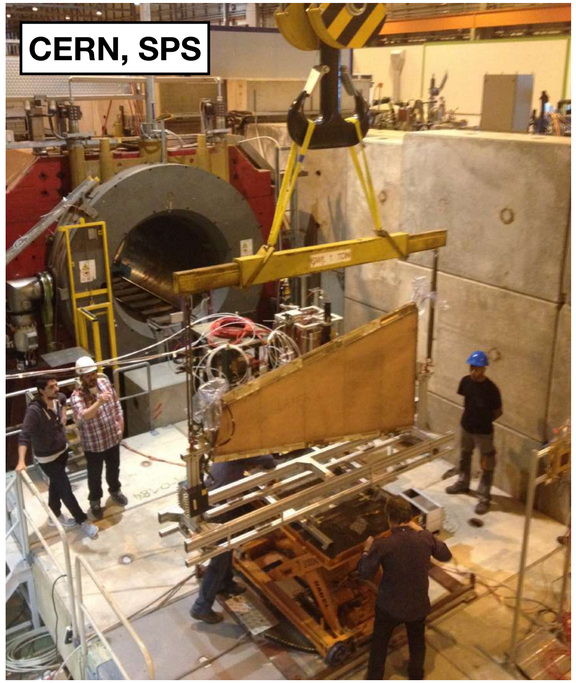
Table B.1: Specifications of the MM chambers that have been used in the beam tests of the ATLAS New Small Wheel MM activity.

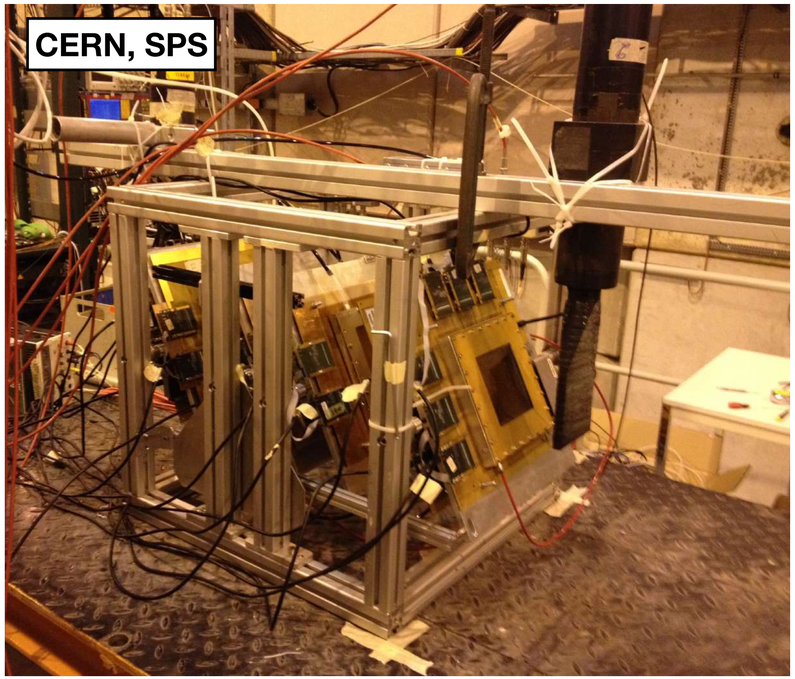
MM Name	Readout Width/Pitch (mm)	Resistivity (MΩ/cm)	Mesh Wire Diameter/Opening (mm)	Pillars Diameter/Pitch (mm)	Active Area (cm^2)
Tmm X Tmm Y	0.15/0.25 0.08/0.25	25	0.018/0.045 (403 lpi)	0.3/2.5	100
Tmb X Tmb Y	0.15/0.25 0.08/0.25	25	0.018/0.045 (403 lpi)	0.5/5.0	100
Mux X Mux Y	0.15/0.25 0.08/0.25	40	0.018/0.045 (403 lpi)	0.3/2.5	64
T1-4	0.30/0.40	25	0.018/0.045 (403 lpi)	0.3/2.5	100
T5-8	0.30/0.40	8	0.018/0.045 (403 lpi)	0.3/2.5	100
TQF	0.30/0.40	25	0.018/0.045 (403 lpi)	0.5/5.0	100
T4C	0.32/0.40 0.22/0.40 0.12/0.40 0.08/0.40	25	0.018/0.045 (403 lpi)	0.3/2.5	100
ExMe	0.30/0.45	25	0.028/0.050 (326 lpi) 0.030/0.070 (254 lpi)	0.5/5.0 0.5/7.0 0.5/8.5 0.5/10	2500
MMSW	0.30/0.415	1	0.030/0.050 (318 lpi)	0.3/2.5	5000

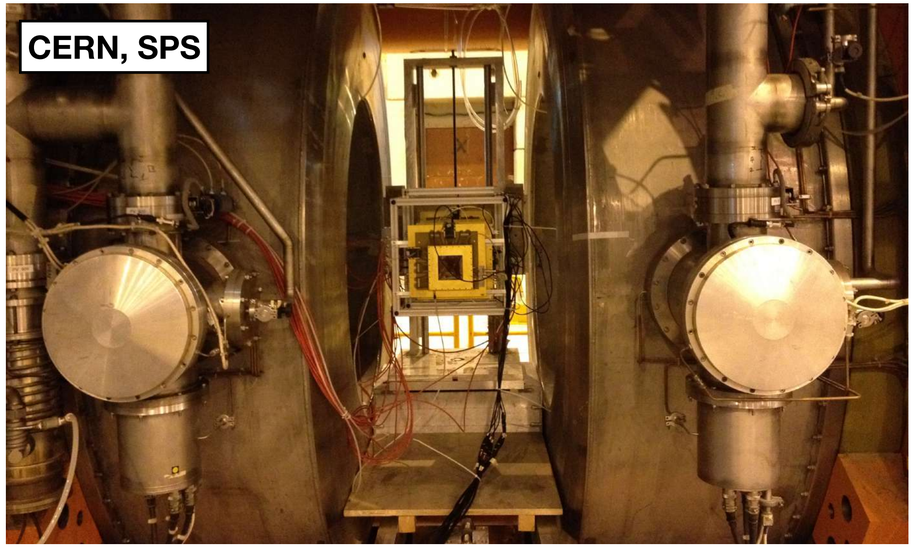
NSW MM R&D - Test Beams

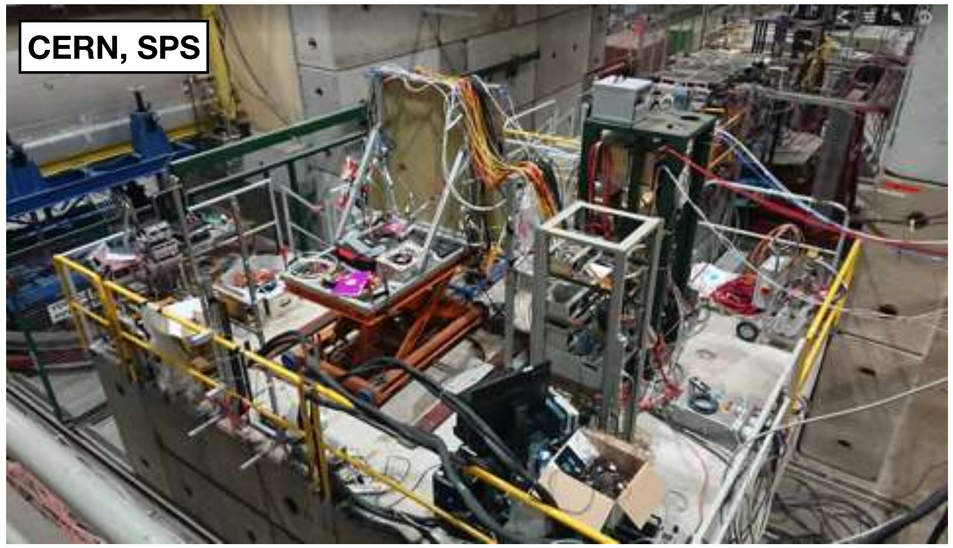
Accumulated more than 50 weeks of test-beam time

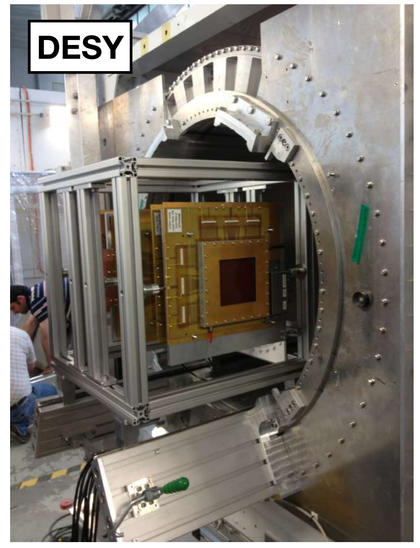






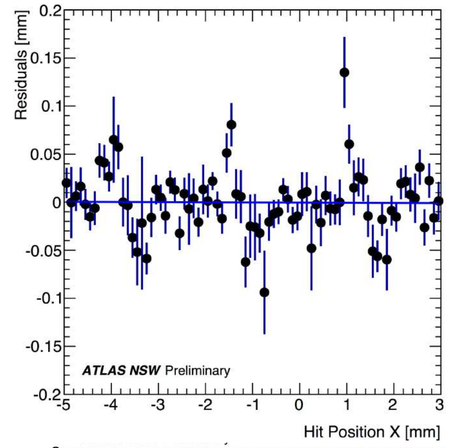






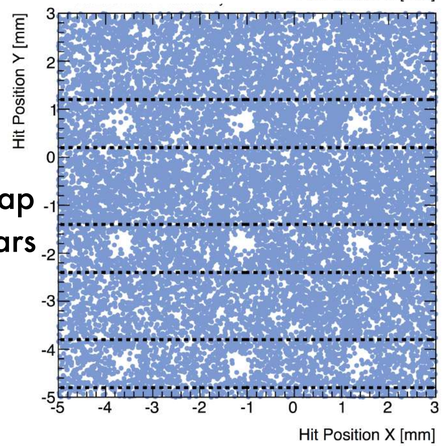
NSW MM R&D - Optimise the detector layout

- **Tested numerous MM prototypes and studied their performance as a function of their structural and operational characteristics**
  - **Stereo readout geometry (1.5° degrees tilt between the strips of the different layers) for 2nd coordinate reconstruction**
  - **Different pillar configurations for minimising their effect in the detector efficiency and resolution**
  - Different HV distribution schemes and gas mixtures
  - Orientation of resistive vs readout strips, strip pitch and resistivity optimisation
  - Varying sizes and different mechanical structure of detectors (i.e. mechanically floating mesh)
- **The final layout of the NSW MM detectors and their operational parameters were shaped through these studies**

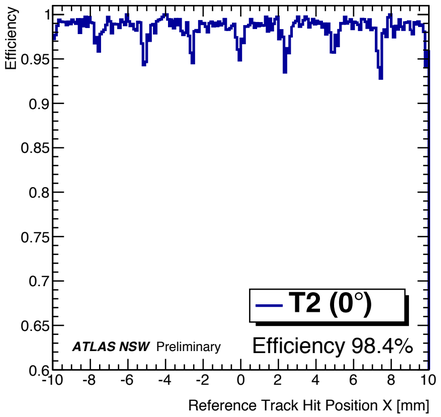


Bias in the hit position reconstruction

Proceedings MPGD 2015

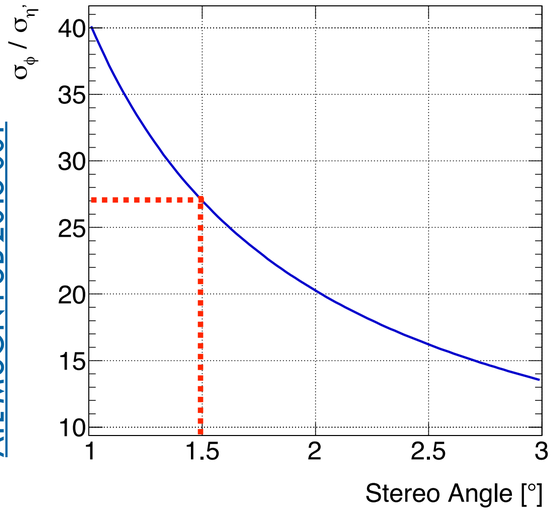


2-D map of pillars

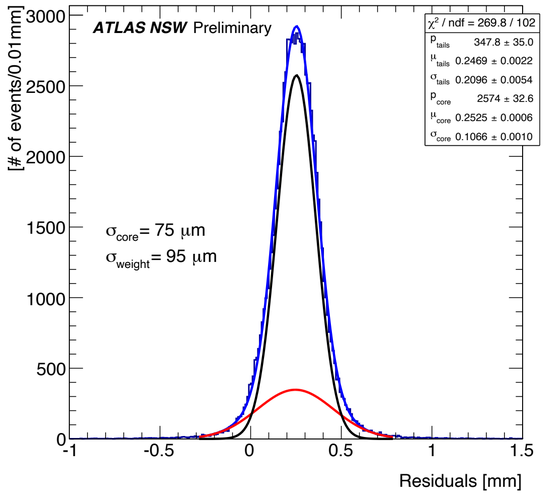


Geometrical Inefficiency

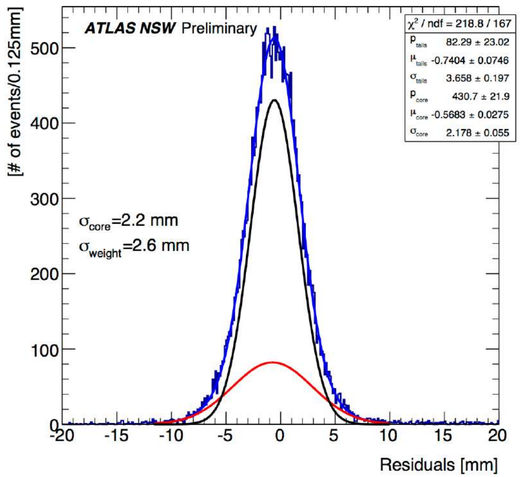
Stereo R/O (Simulation)



Stereo R/O (Data) - σ_η



Stereo R/O (Data) - σ_ϕ

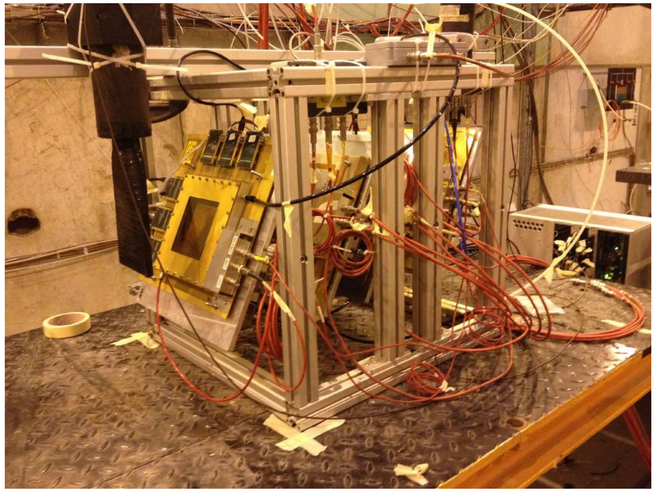


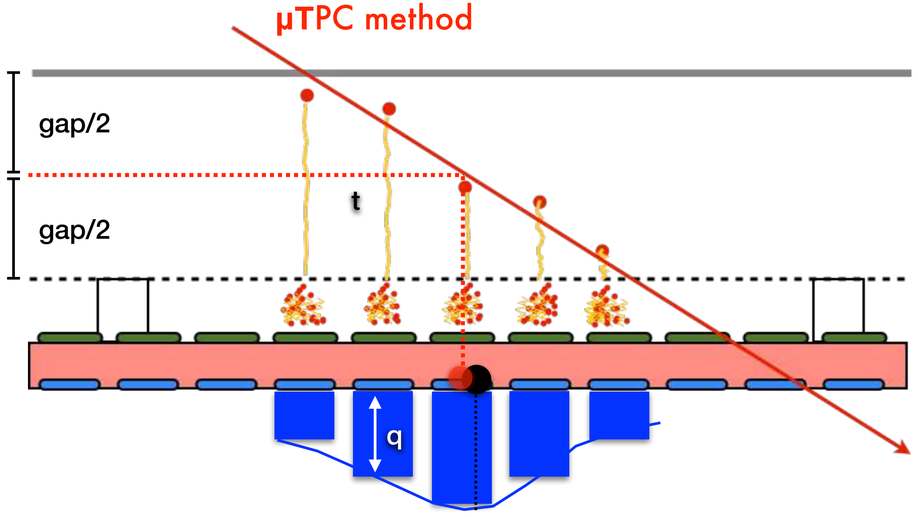
ATL-MUON-PUB-2015-001

NSW MM R&D - Novel hit reconstruction methods

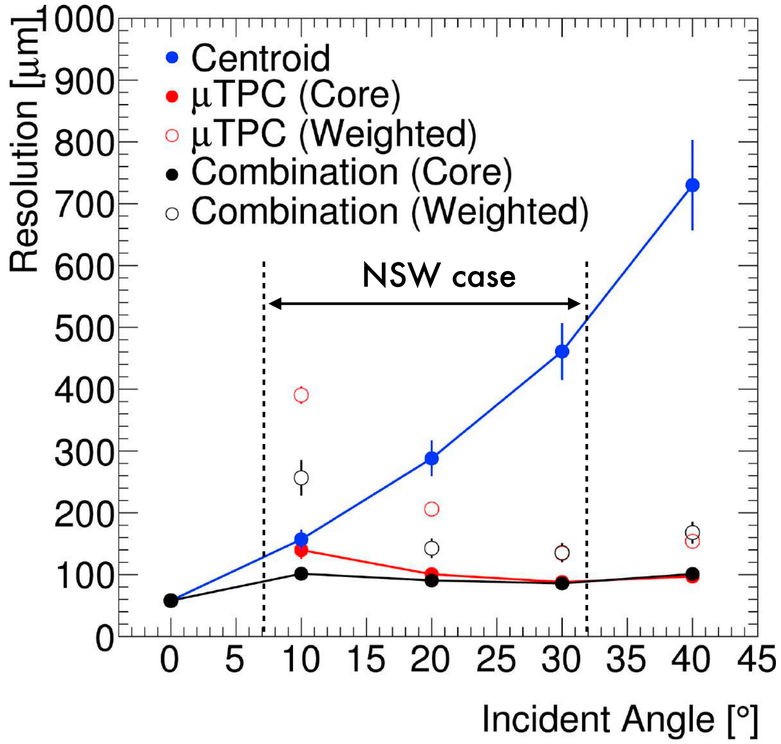
- **Charge centroid method performance deteriorates with increasing the track angle**
  - Issue for the NSW MM since muon tracks will be mostly inclined
- **Due to the fine strip pitch a single MM gap can work as TPC (μTPC method)**
  - Reconstruct the muon track by using the (drift) time measurement
  - Spatial resolution <100μm for track angles > 10°
- **Centroid & μTPC measurements can be combined to extract a single measurement with σ<100μm independently of the track angle**
  - Requirement for the NSW upgrade and milestone for the NSW MM detectors
- **The new reconstruction methods have since been used in other experiments with MM and GEM detectors (RD51)**

10.1016/j.nima.2019.04.050





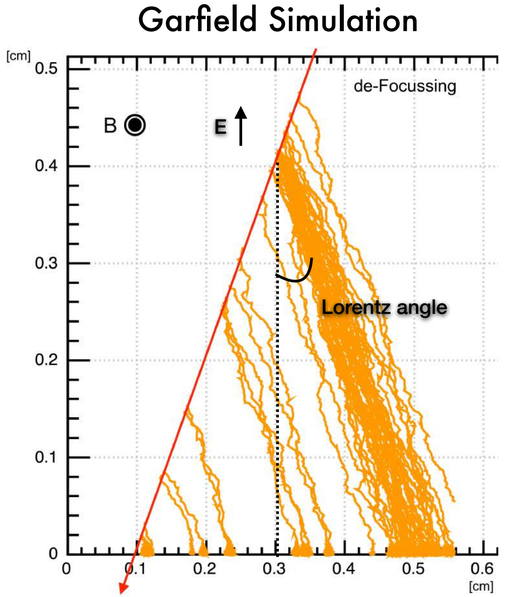
Charge centroid method

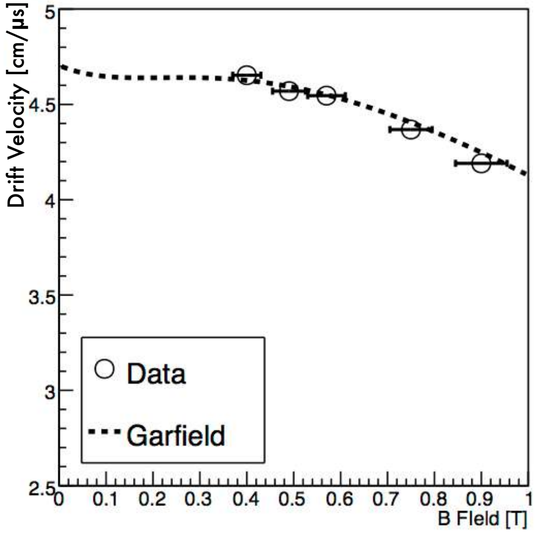


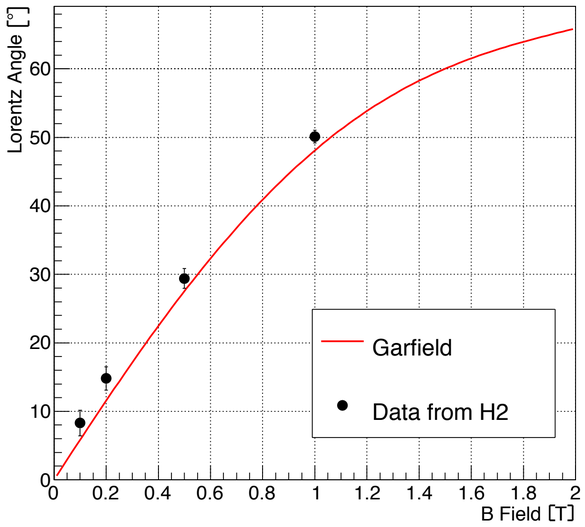
NSW MM R&D - Operation inside a magnetic field

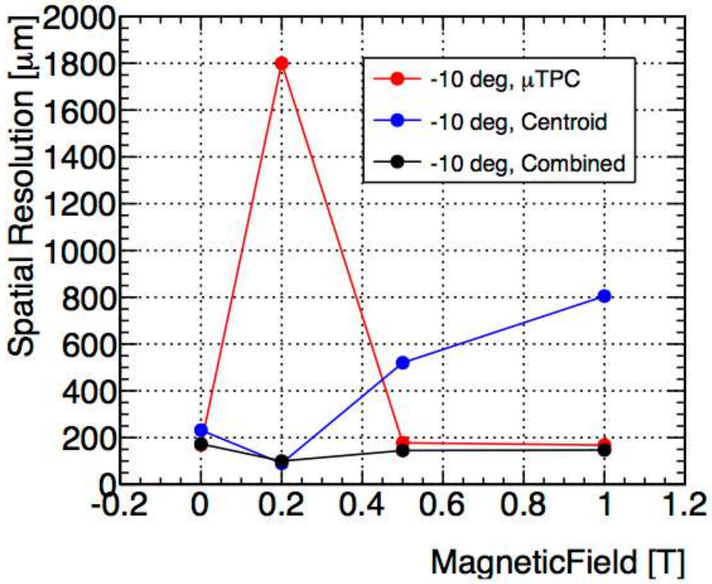
Internal note ATL-COM-MUON-2018-043

- **Multi-directional and non-uniform magnetic field in the ATLAS SW region (<0.4T)**
  - Mostly unexplored field for the MM technology
- **Ensure that the performance of the detector inside a magnetic field is well-understood and its excellent characteristics are not maintained**
  - Studies in simulation as well as using data acquired in test-beams with magnetic field
  - Requirement for the NSW upgrade and milestone for the MM technology









The NSW MM R&D - Other performance studies

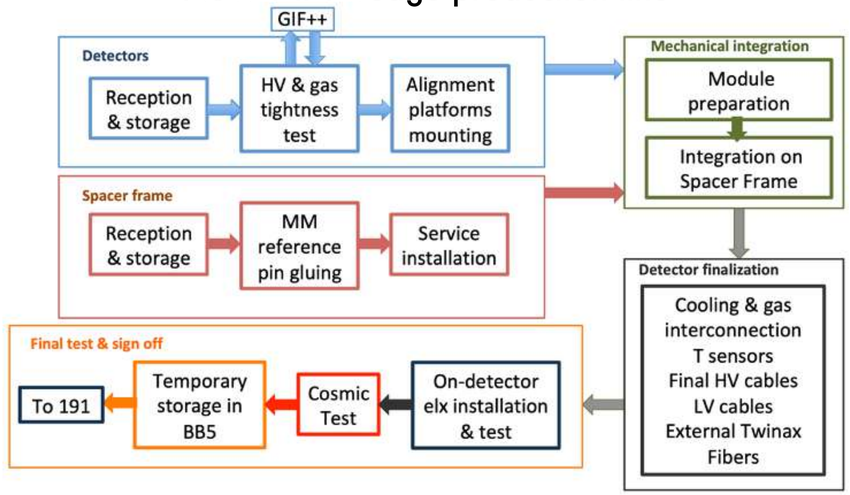
- **Characterisation of the timing performance**
  - Timing resolution depends on the track angle (limited by the strip readout geometry and the gas properties)
  - The MM can be used for triggering in the NSW
- **Performance characterisation of the MM detectors using the first version of the VMM ASIC for FE chip**
  - Proved that timing and position resolution are within specs
  - All NSW FE cards are equipped with VMM(3A) chips
- **Noise measurements and studies with different detector prototypes for estimating the expected noise in the NSW MM detectors**
  - Noise is a function of the strip capacitance (length)
  - Noise values predicted by extrapolation from measurements on small detectors agree with the actual measurements on the NSW MM chambers
- **Performance studies of MM chambers with multiplexed (x5) readout strips**
  - Reduced number of electronic channels
  - Hit reconstruction accuracy remains ~unaffected by the multiplexing however the noise per electronic channel scales up with the multiplexing factor

ATL-UPGRADE-PUB-2014-001

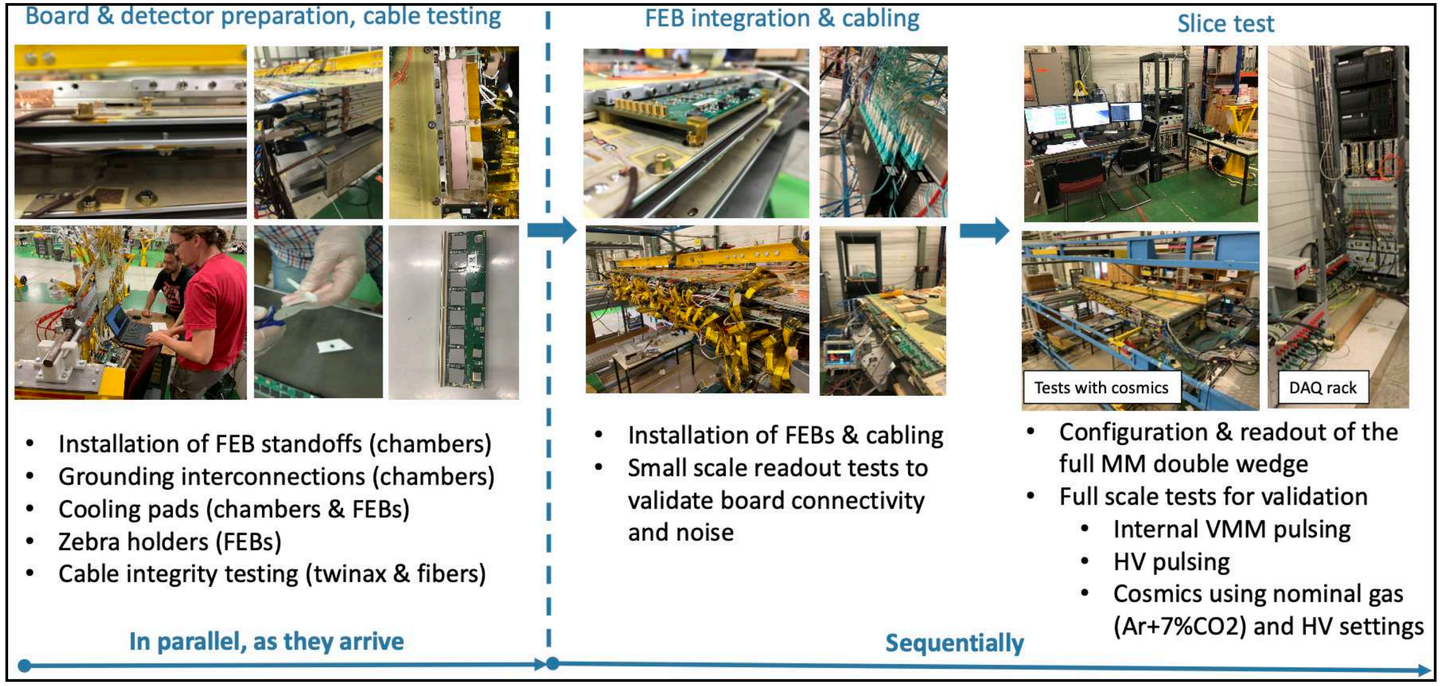
NSW MM wedge integration

- **Co-coordinator of the NSW MM electronics integration and of the final validation of the NSW MM double wedges with cosmic rays**
  - >5K boards, >2M readout channels
- **Development, operation and maintenance of the test-benches and all the related services and infrastructure**
- **Definition of tests and acceptance criteria, workflow organisation and training of students/technicians**
- **Guiding students on the development of the required software tools for the test-benches as well as for the analysis of the cosmic ray data**

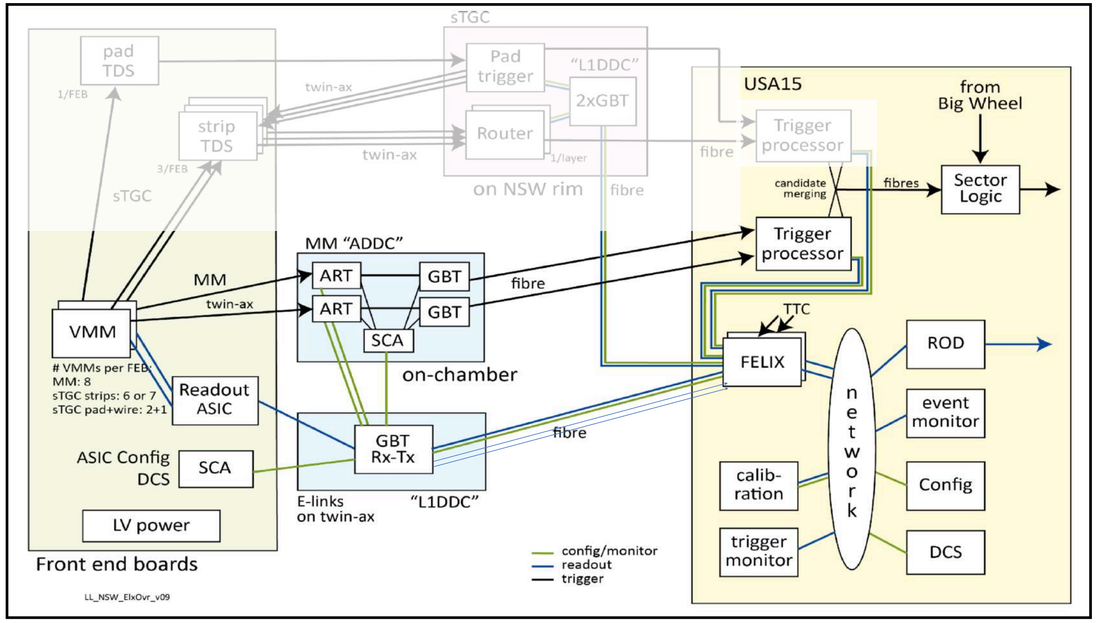
NSW MM wedge production line



NSW MM Electronics Integration Workflow

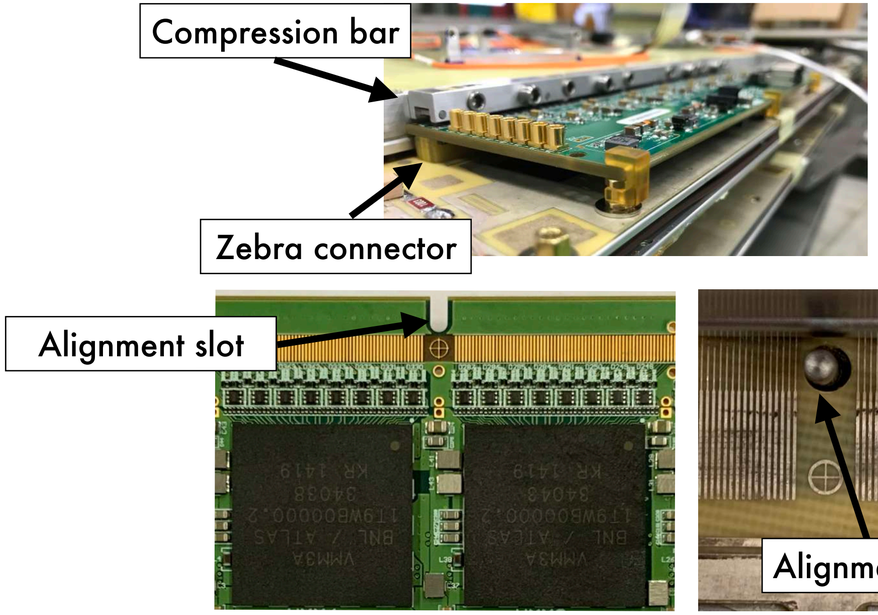


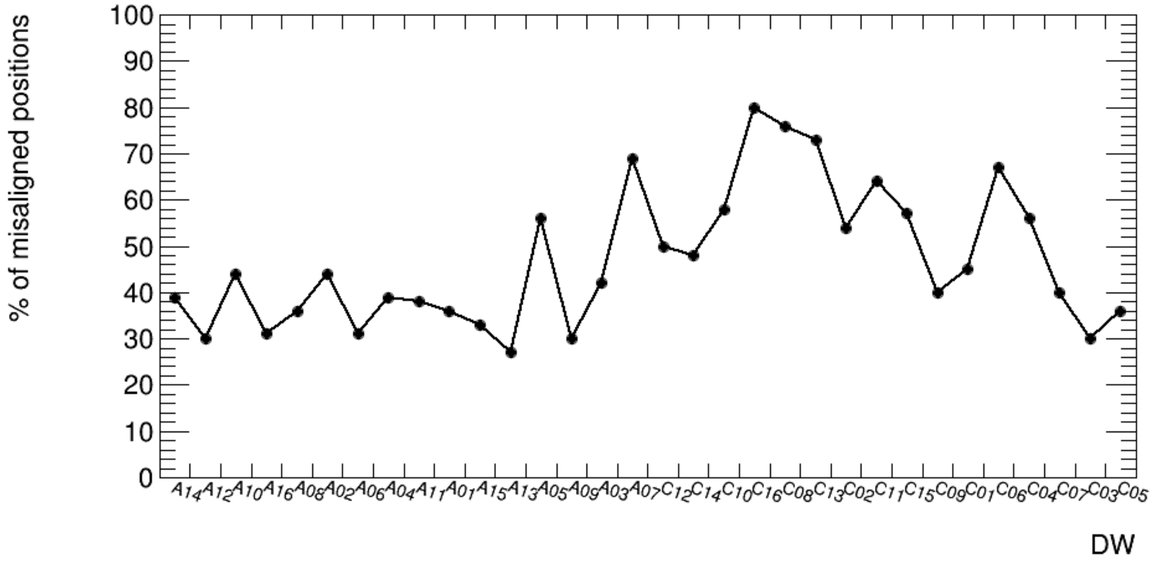
NSW DAQ & Trigger Architecture (MM-centric)

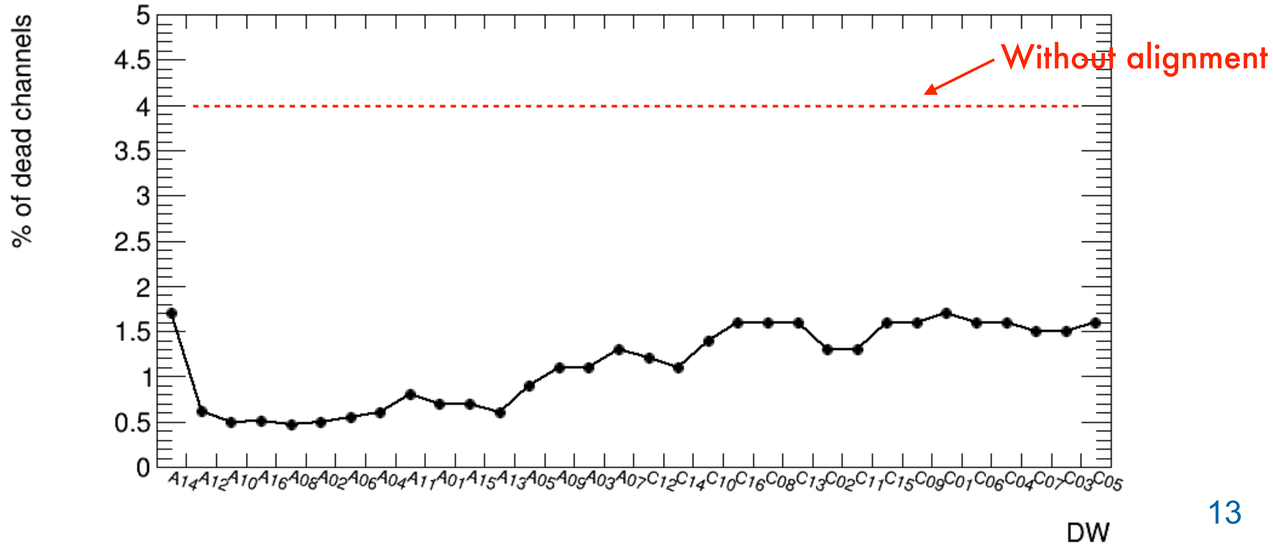


NSW MM electronics integration - FE board misalignment

- **Unexpectedly high number of "dead" electronic channels in the first MM wedge**
- **Sorted FE channels caused by relative misalignment between the FE board and the detector strips**
  - >4% effectively dead channels if boards are not mechanically aligned
- **Investigation and development of mitigation actions**
  - Board quality, chamber quality, alignment pit precision, zebra connector; they all play a role
  - Contributed in the conceptual design of a LED tester board that can be used as a guide for aligning the boards during installation



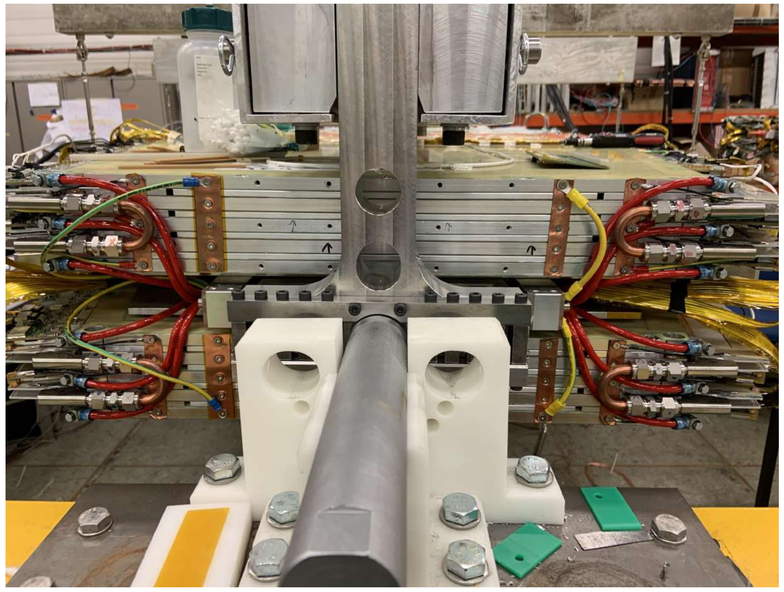




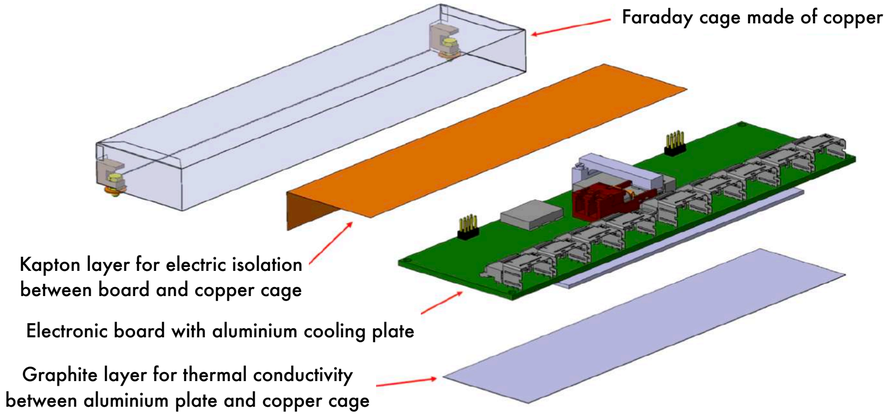
NSW MM electronics integration - Noise investigations

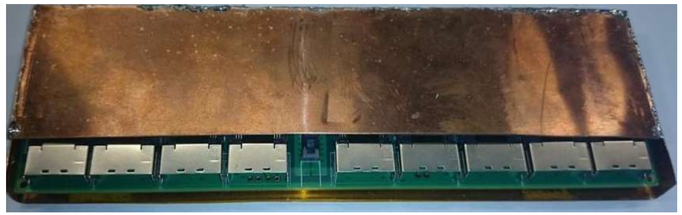
- **Excessive localised noise has been observed in the first NSW MM wedges**
- **Contributed in the noise investigations and in the development of mitigation actions**
  - Necessary refurbishment of electronics and detectors established in the routine operation of the MM electronics integration

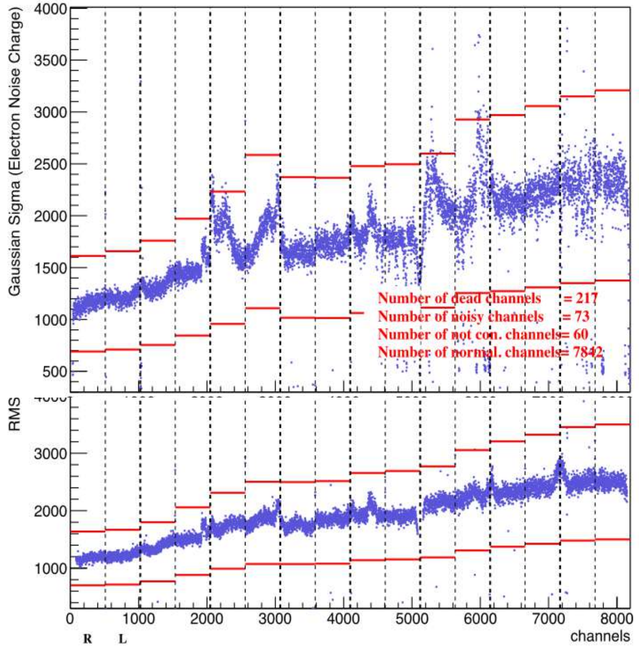
Improved grounding



Improved shielding of the ADDC boards

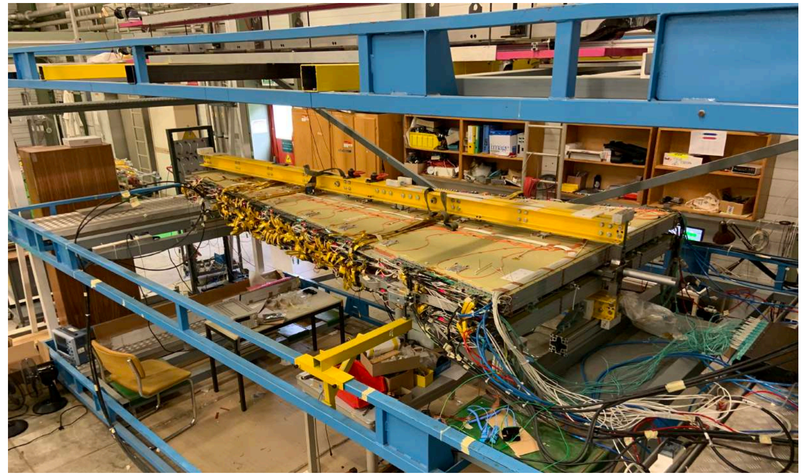




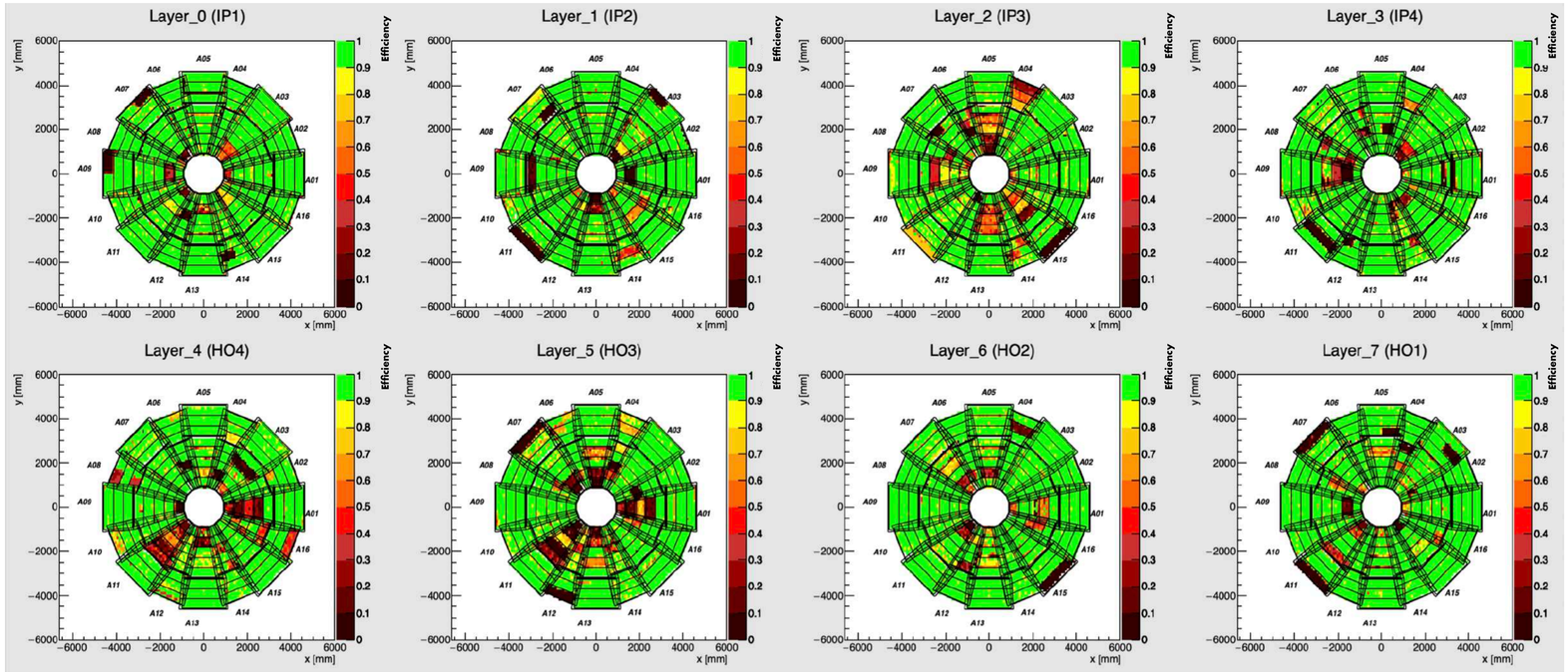


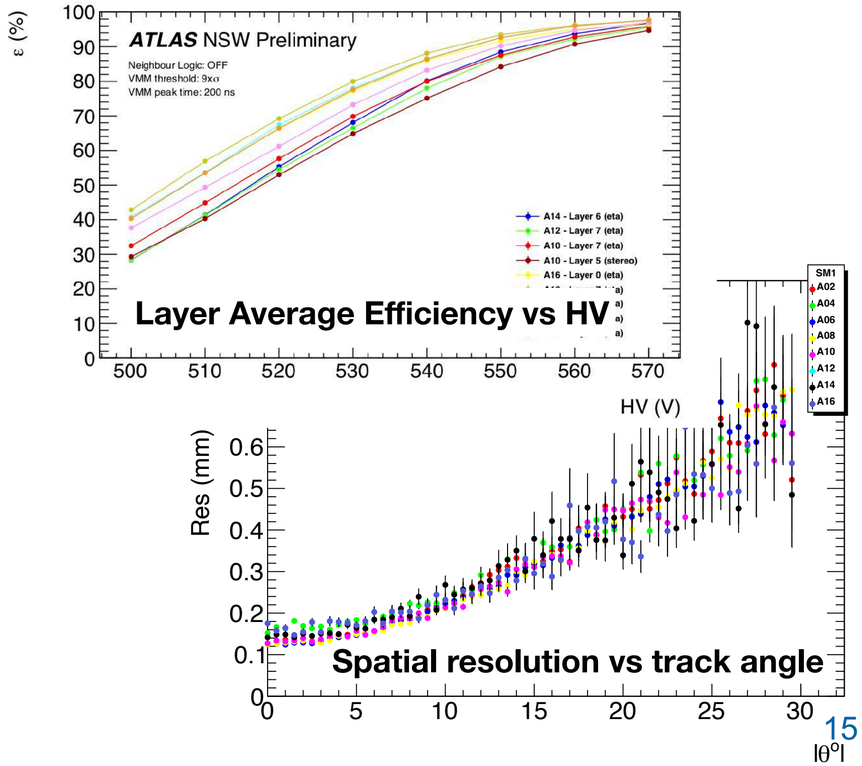
NSW MM Wedge final validation with cosmics

- **Coordinated the development and operation of the cosmic-ray test stand at CERN**
- **Definition of Data Quality monitoring plots and improvements in the offline analysis framework**
- **Guidance of students in realising detector performance studies**



2-D map of the MM efficiency per layer for NSW-A
(areas with reduced efficiency have lower HV)

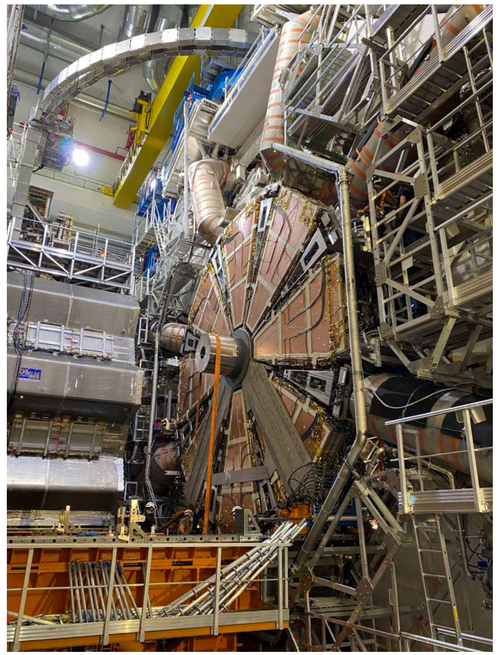




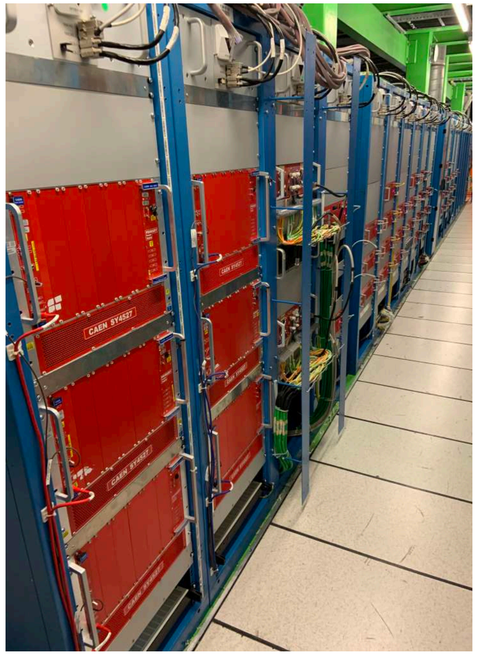
Integration and Commissioning of the NSWs with the ATLAS experiment

- **Responsible for the preparation of NSW racks and equipment installation**
- **Organisation of the services preparations and connections to the NSWs**
- **Organisation of NSW-related activities at P1 and contact person with ATLAS Technical Coordination and Safety**
  - Definition and distribution of work-packages, preparation of schedule and coordination of all underground activities and their safety aspects
- **Development of NSW Detector Safety System (DSS)**
  - Architecture definition, hardware connections and implementation of the DSS Alarm-Action Matrix (pre-requisite for the operation of the NSWs in the ATLAS cavern)
- **Coordinating the integration of the NSWs in the Muon System Operations**
- **Coordination of the NSW commissioning activities at P1**

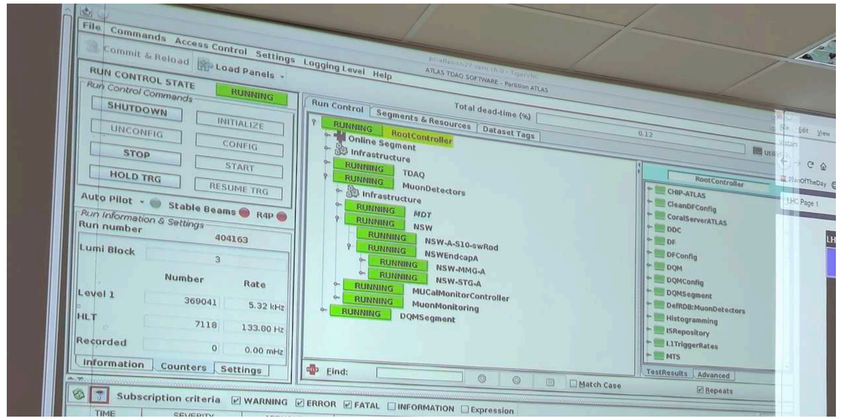
NSW-A installed and connected



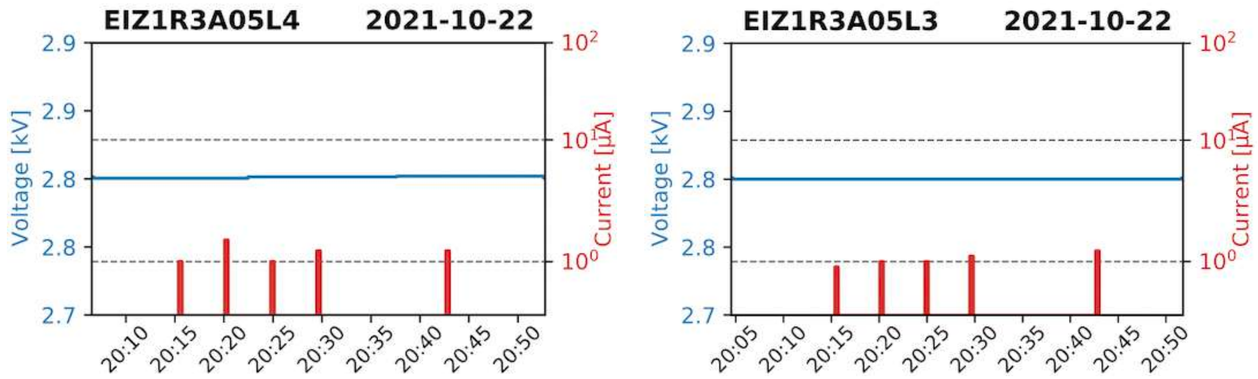
NSW Power System



Integration of NSW in the ATLAS combined DAQ partition



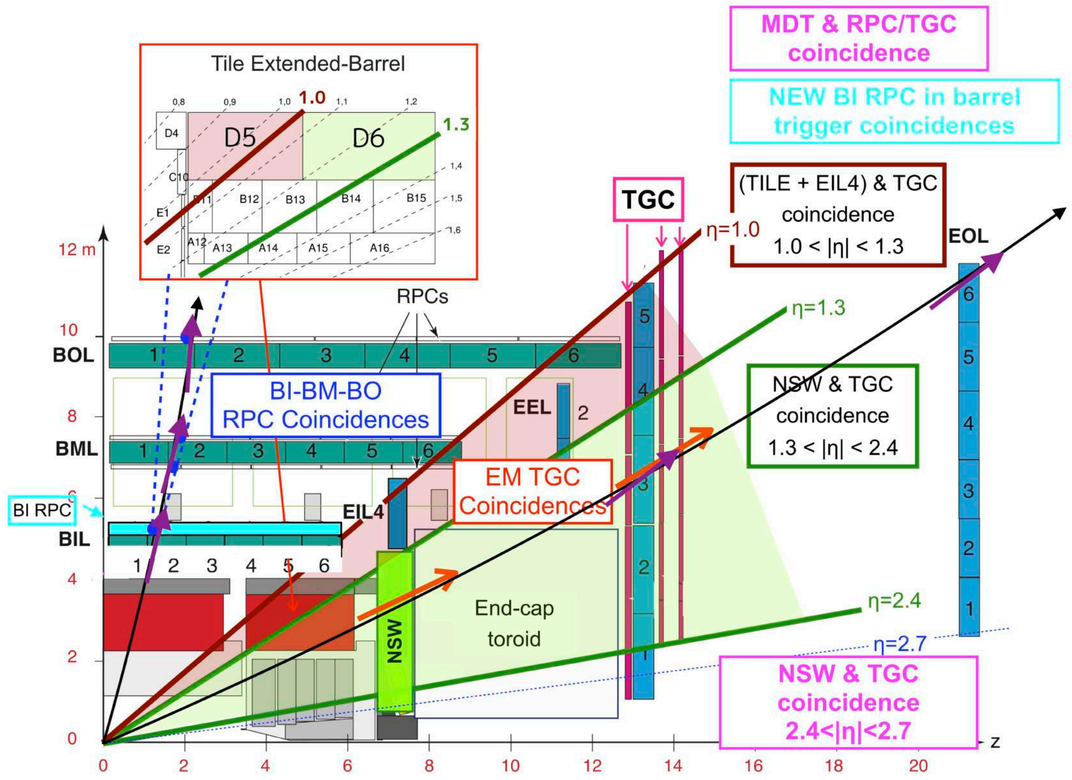
Beam Splashes observed in the monitored HV current of the NSW detectors



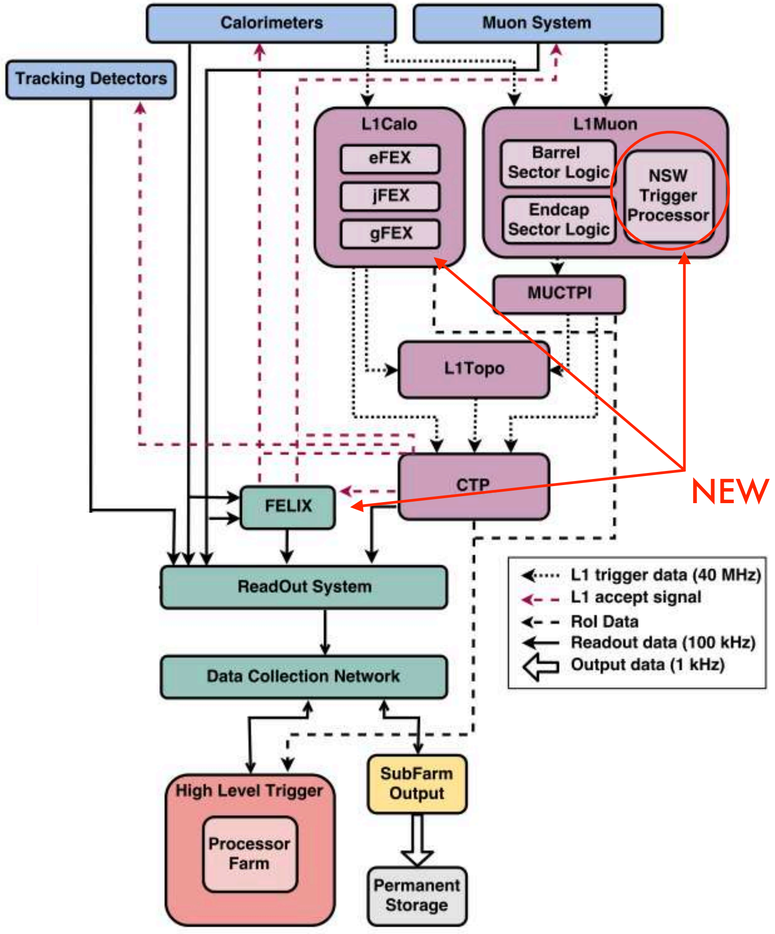
The Phase-2 Upgrade of the ATLAS Muon Trigger System

The Upgrade of the ATLAS TDAQ System

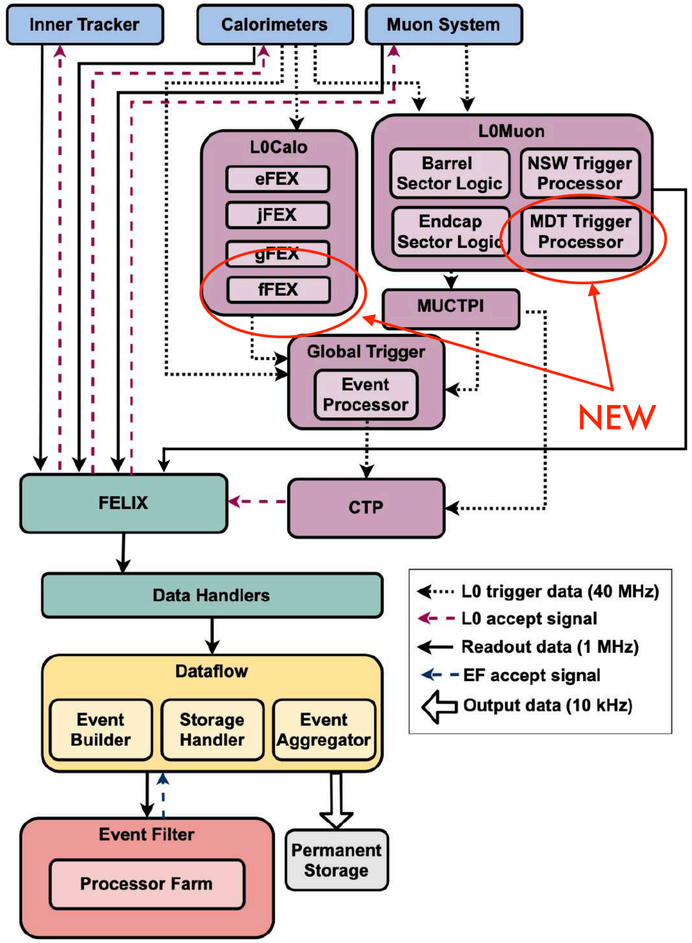
- **Single-level hardware trigger with detector readout rate of 1MHz and 10μs latency for Run-4**
- **Keep thresholds low to fully exploit the physics potential while keeping the rate under control**
- **Include MDTs in the L0 muon trigger system (possible due to increased latency)**
  - Exploit superior spatial resolution (compared to RPC/TGC) for improving the accuracy in the muon pT measurement



RUN-3

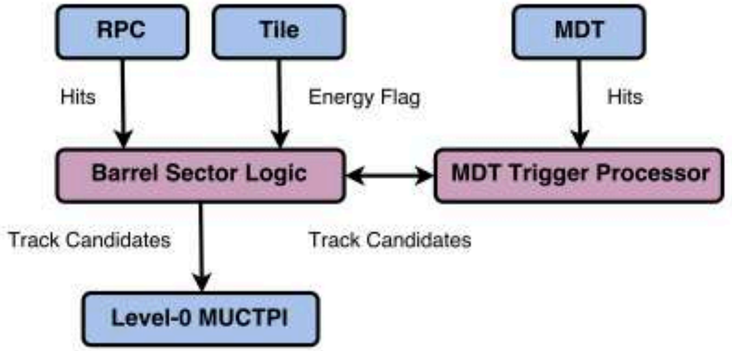


RUN-4



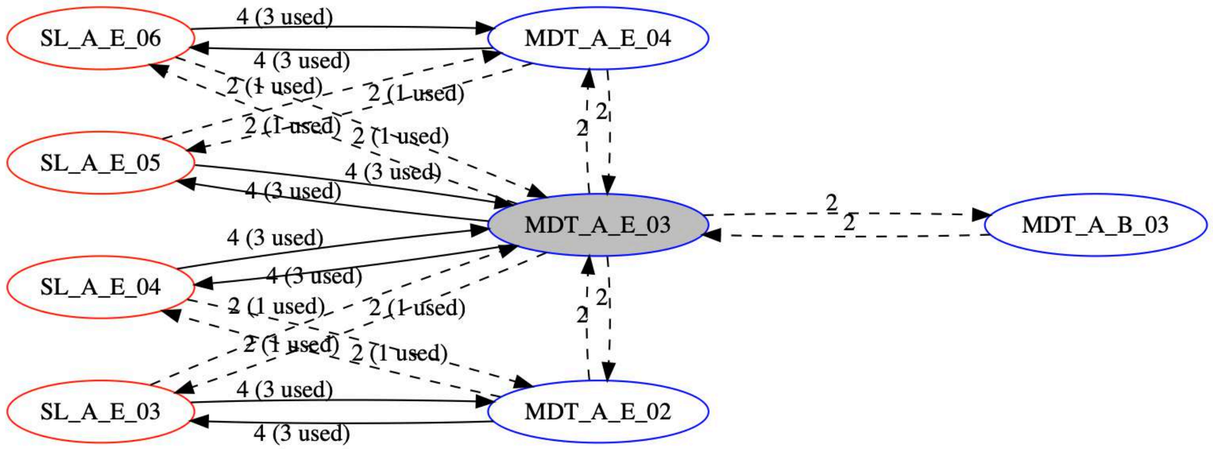
L0 Muon Trigger System Architecture

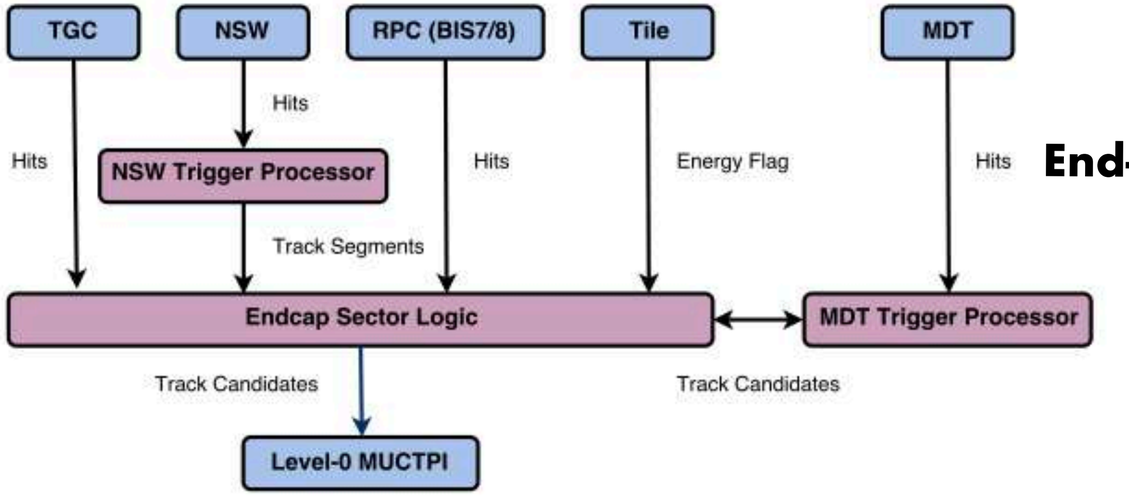
- **Contributed to the finalisation of the L0Muon Trigger High-level architecture**
  - Number and type of links between the different components
- **Contributed to defining the specifications of the system**
  - Data-formats for all the new interfaces



Barrel

Endcap large sector optical links for the MDT Trigger Processor (not 1-1 TGC vs MDT sector geometry)



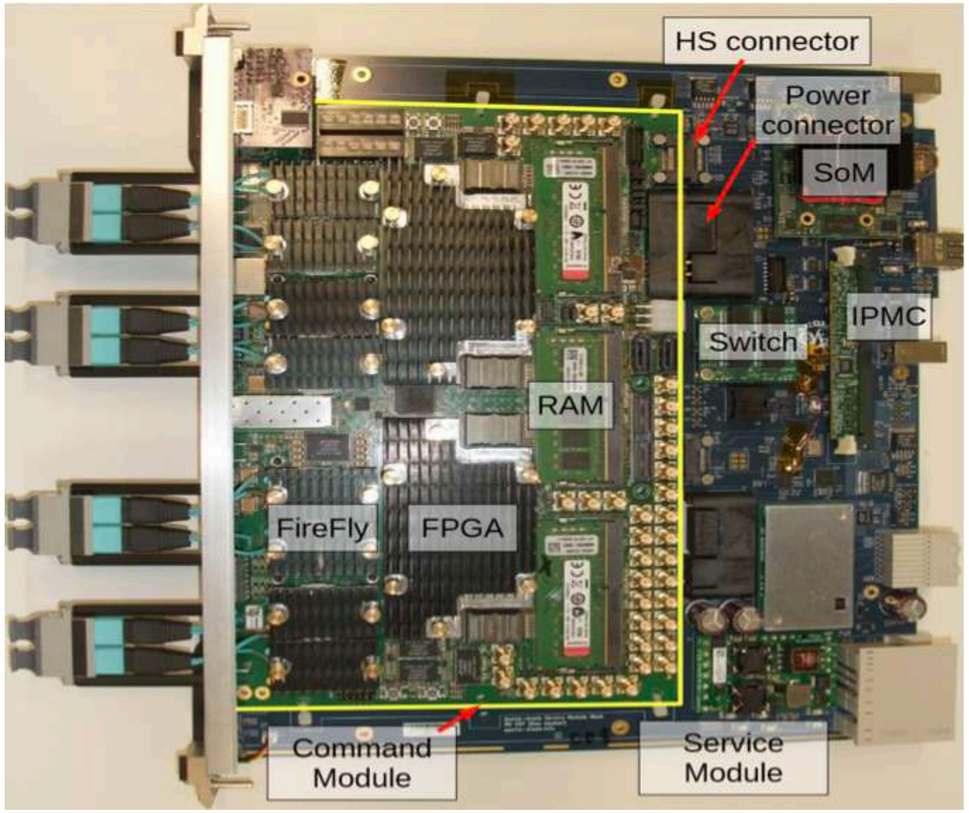


End-cap

The MDT Trigger Processor (MDT-TP)

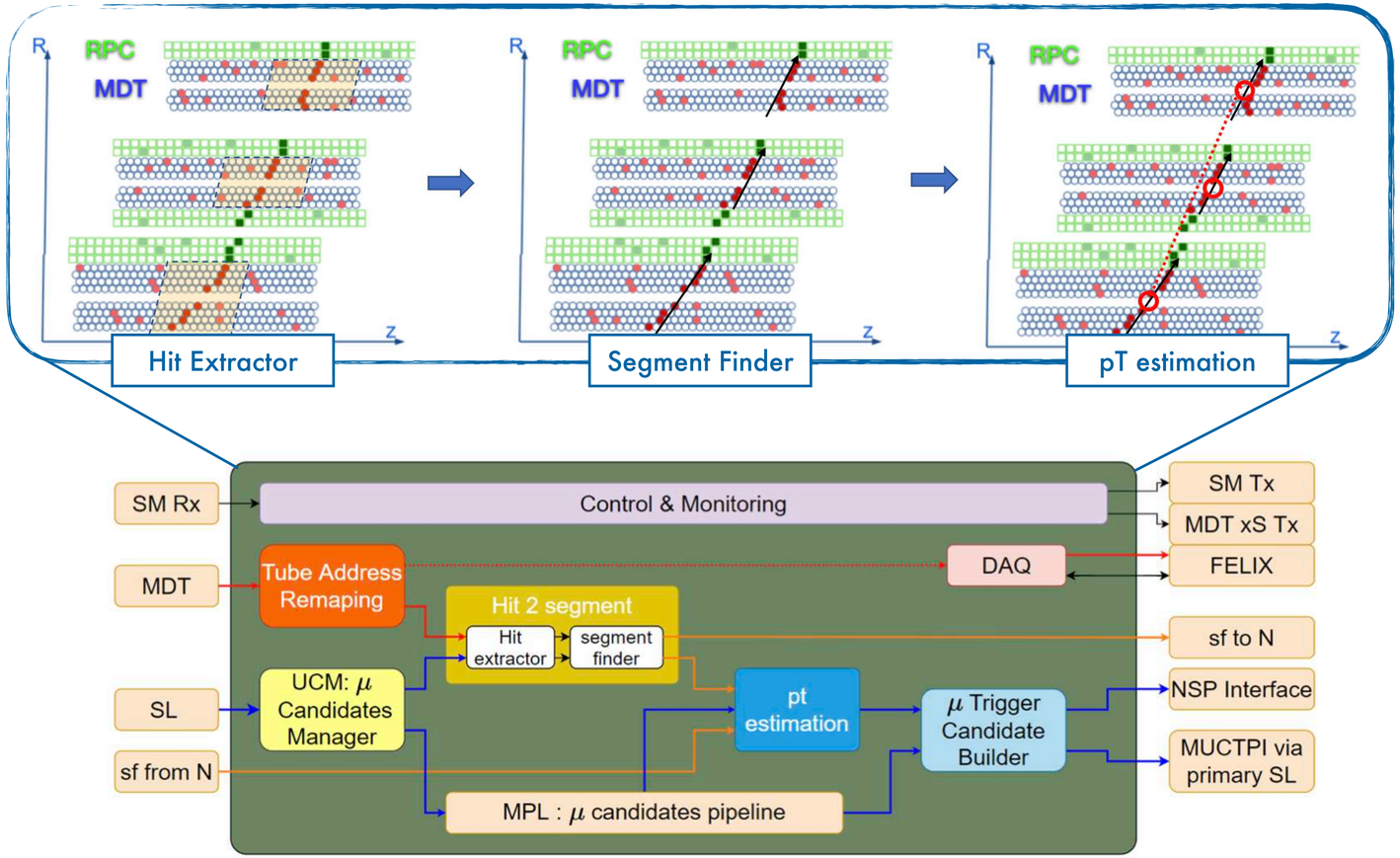
- **Contributed in the definition of the MDT-TP firmware blocks for the trigger decision and the conceptual design of the MDT-TP ATCA blade**
- **Development of algorithms in software, firmware & performance studies**

MDT-TP Hardware Demonstrator



1 MDT-TP Blade/MDT sector (64 in total)

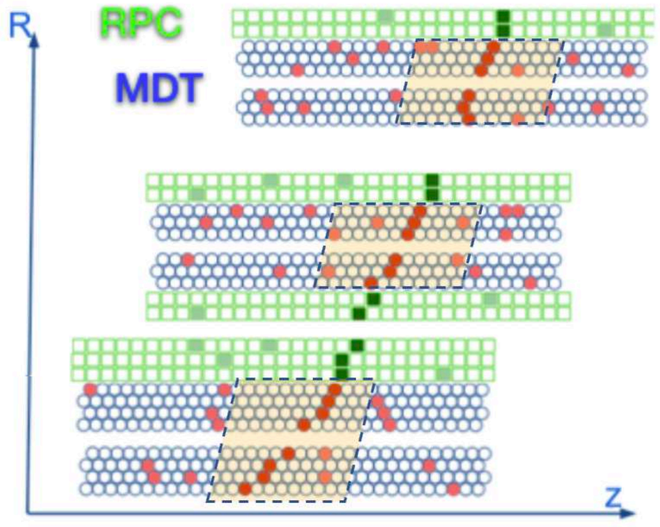
MDT-TP Main Firmware blocks



MDT-TP Trigger Algorithms

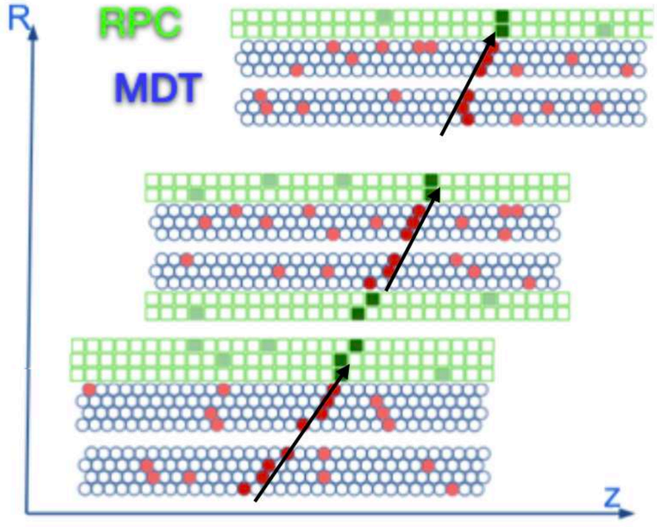
- **Co-developer of the main MDT-TP trigger algorithms simulation in software**
  - Pre-requisite that the algorithms are implemented in detail and fine-tuned before we go into firmware development (performance needs to match requirements)
  - The result of the algorithm simulation is needed as a reference for validating the firmware functionality

Hit Extraction*



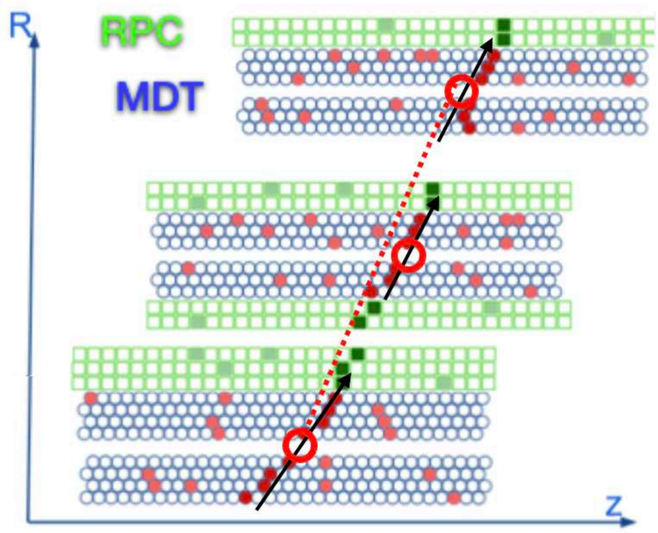
A. Armstrong, K. Ntekas

Segment Finder*



K. Ntekas

pT Calculation*



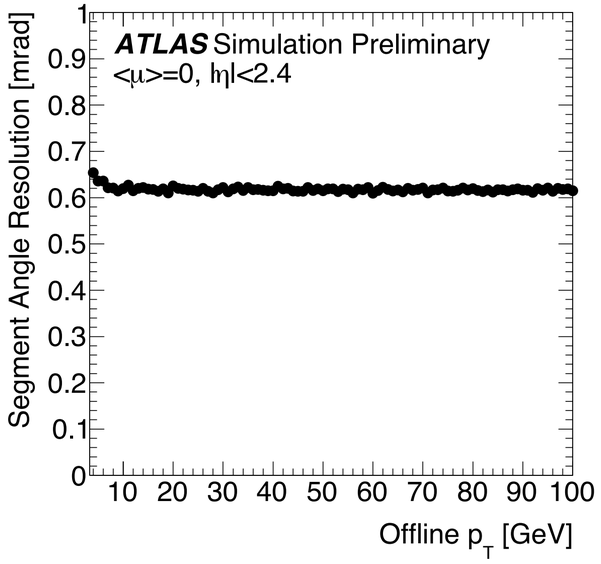
K. Ntekas , A. Soffa., A. Taffard

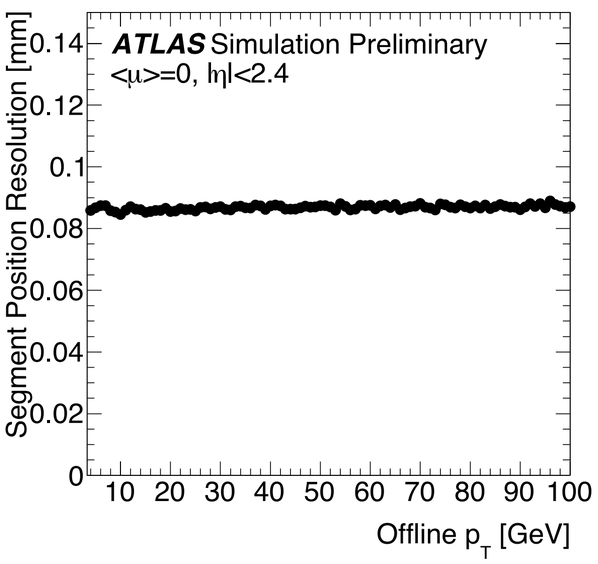
*Algorithm seeded by the Sector Logic (SL) candidate information

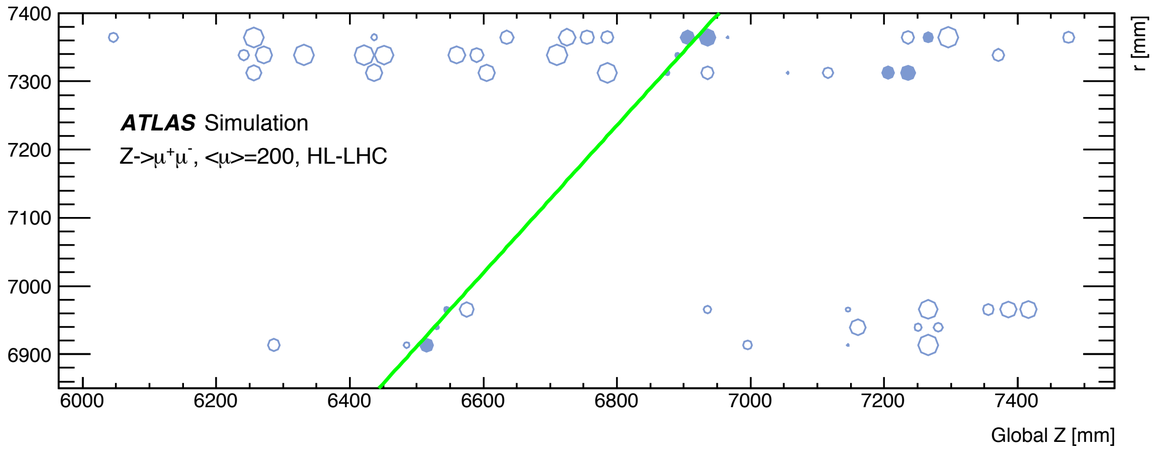
MDT-TP Trigger Algorithms - Legendre Segment Finder (LSF)

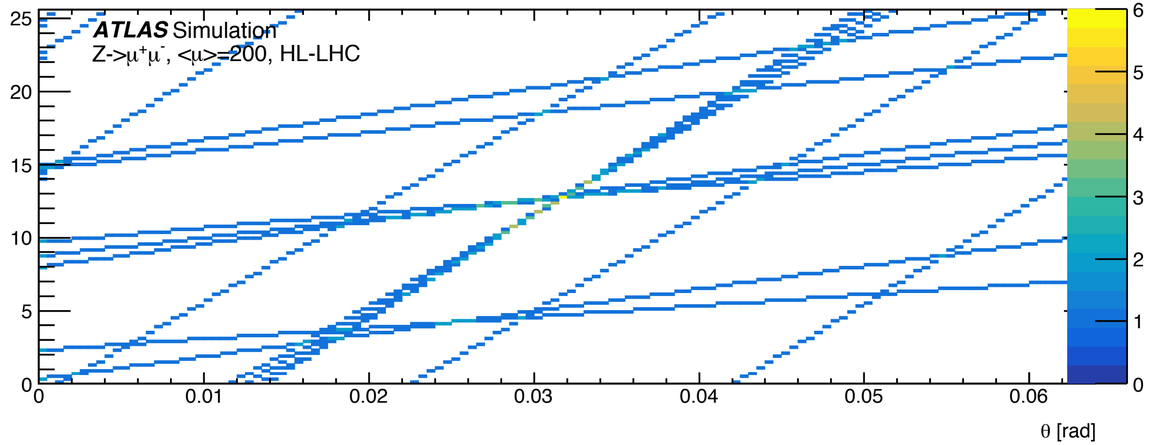
Proceedings Connecting the DOTs 2018

- **Pattern recognition (histogram-based) algorithm for the segment reconstruction in MDTs**
  - Each drift circle in the cartesian space corresponds to 2 lines in the Legendre space
  - Max bin corresponds to the most popular tangent line
- **Very good performance achieved**
  - Trigger seed from SL is used for narrowing down the Legendre space around the expected answer





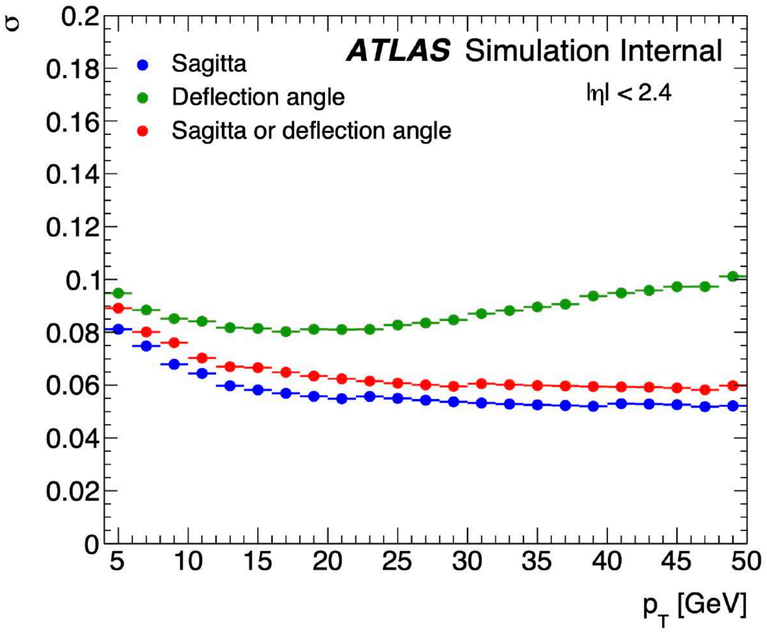


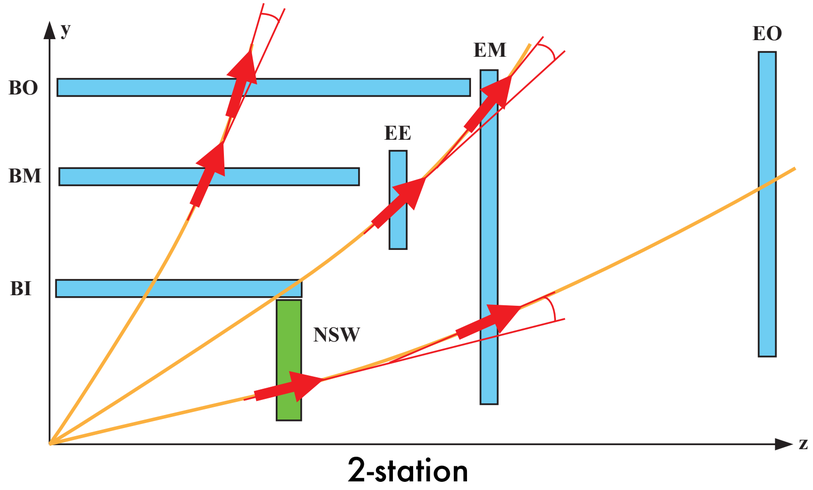


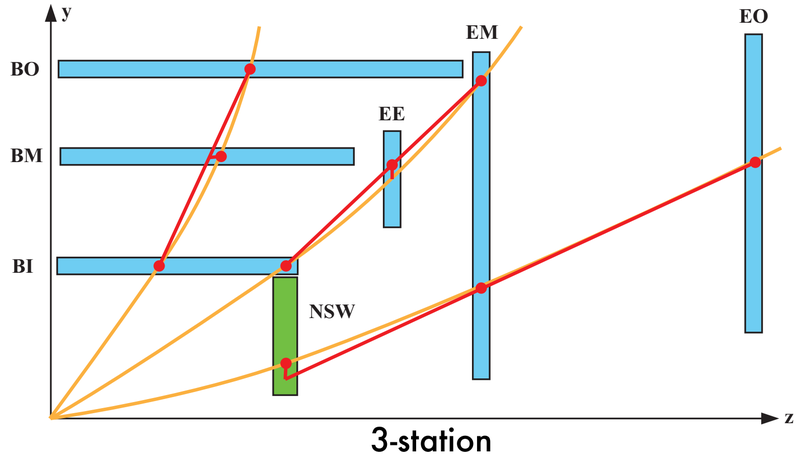
MDT-TP Trigger Algorithms - pT calculation

Proceedings TWEPP 2019

- **Co-developer of new method for fast pT calculation**
  - Measure segment deflection angle (2-station) or sagitta (3-station)
    - Both quantities are correlated with muon pT and B-field
  - Non-uniform B-field and chamber geometry along η and ϕ
    - The pT dependency on the deflection of the muon trajectory can be parametrised with η and ϕ
    - Split the MDT system in ~500 trigger towers (chamber combinations) and extract a different parametrisation per tower
- **Method achieves pT resolution close to the one of the offline reconstruction and can be easily implemented in firmware utilising LUTs**



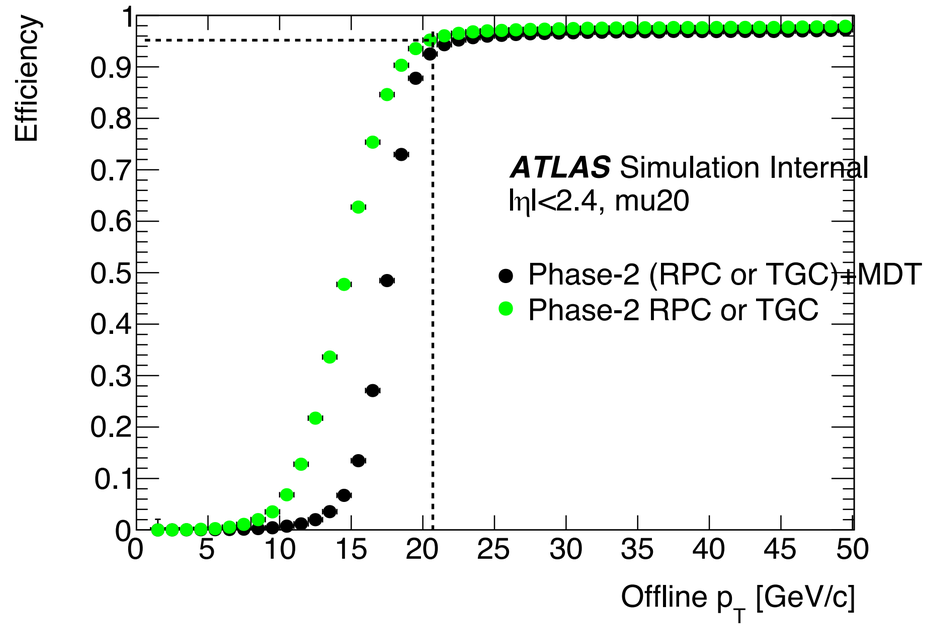


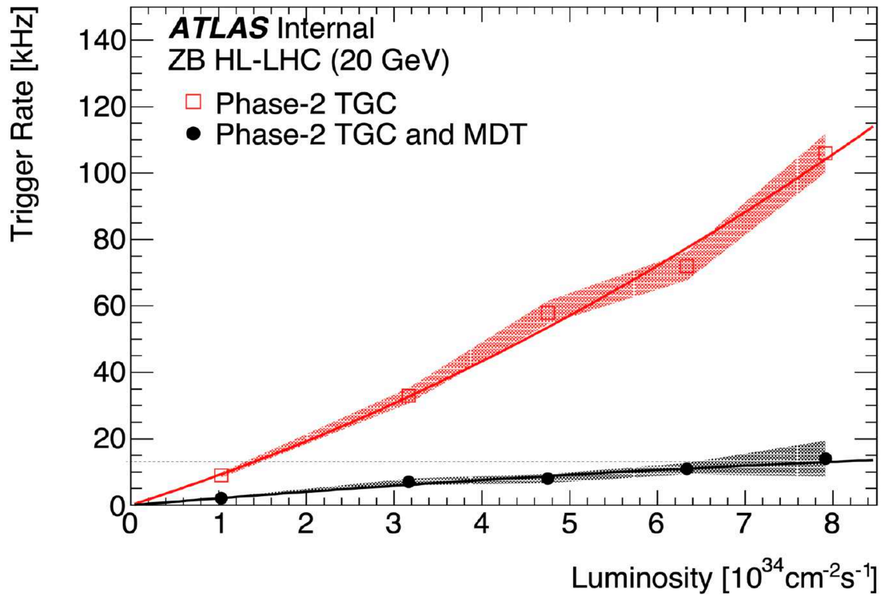


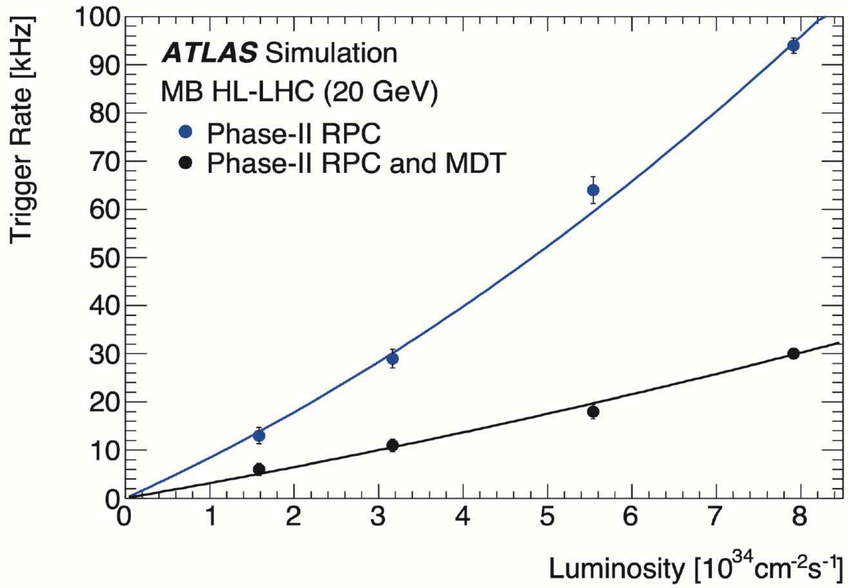
The expected Performance of the Phase-2 L0 Muon Trigger System

ATLAS TDAQ Phase-2 TDR

- **Coordinator of the Phase-2 L0 Muon Trigger simulation framework**
  - Produce custom made n-tuples from ATLAS DATA & MC
  - Simulation of the full Phase-2 L0 Muon trigger chain
- **Performed trigger performance studies for the upgraded L0 Muon Trigger architecture**
  - Proof of concept, included in the ATLAS TDAQ Phase-2 TDR







MDT-TP Firmware development

- **Development of the firmware for the LSF algorithm using the Vitis HLS tool**
  - Latency, resource usage and performance within specs (main firmware deliverable for UCI)
- **Guiding students in the development of the other MDT-TP algorithms in HLS**
  - Get acquainted with the concept of HDL and the differences between software and firmware
  - Understand the effect of bit-precision and replacing calculations with LUTs in the performance of the algorithms (HLS test-bench allows to compare results with offline simulation)

Introduction to Vitis HLS

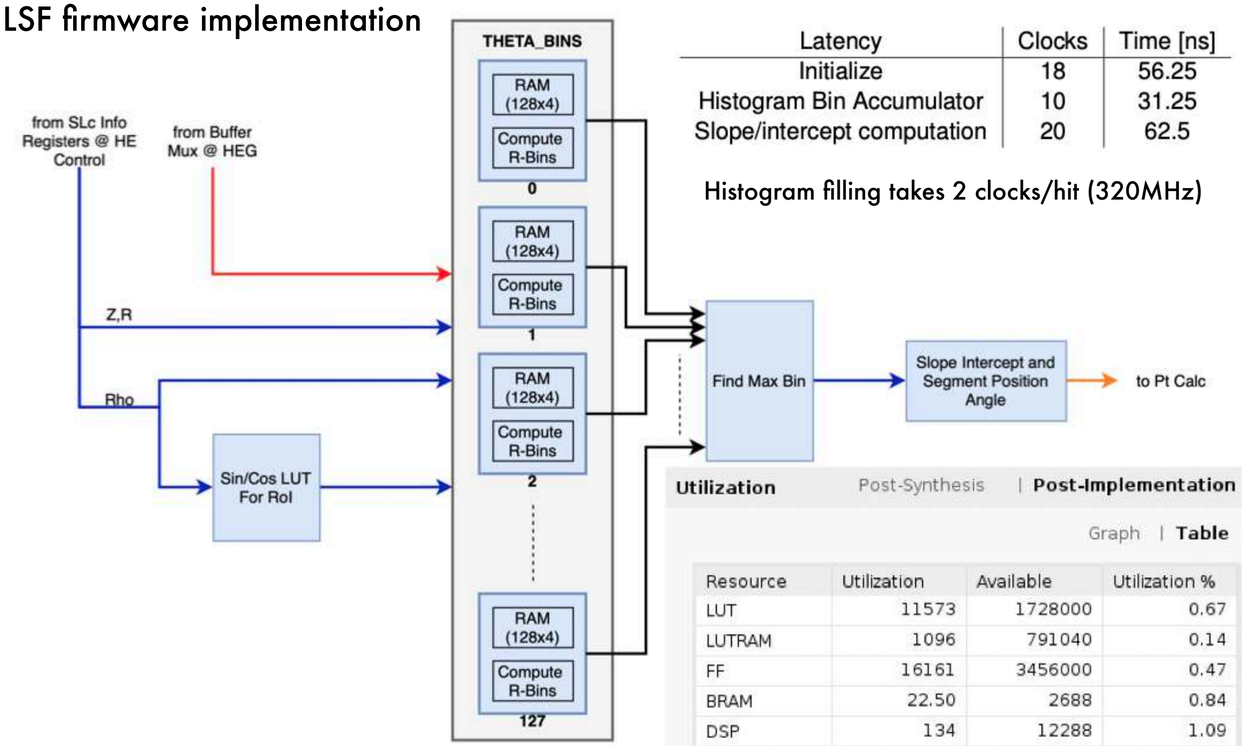
XILINX

Vitis™ HLS is a high-level synthesis tool that allows C, C++, and OpenCL™ functions to become hardwired onto the device logic fabric and RAM/DSP blocks. Vitis HLS implements hardware kernels in the Vitis application acceleration development flow and uses C/C++ code for developing RTL IP for Xilinx® device designs in the Vivado® Design Suite.

Following is the Vitis HLS design flow:

1. Compile, simulate, and debug the C/C++ algorithm.
2. View reports to analyze and optimize the design.
3. Synthesize the C algorithm into an RTL design.
4. Verify the RTL implementation using RTL co-simulation.
5. Package the RTL implementation into a compiled object file (.xo) extension, or export to an RTL IP.

LSF firmware implementation



Latency	Clocks	Time [ns]
Initialize	18	56.25
Histogram Bin Accumulator	10	31.25
Slope/intercept computation	20	62.5

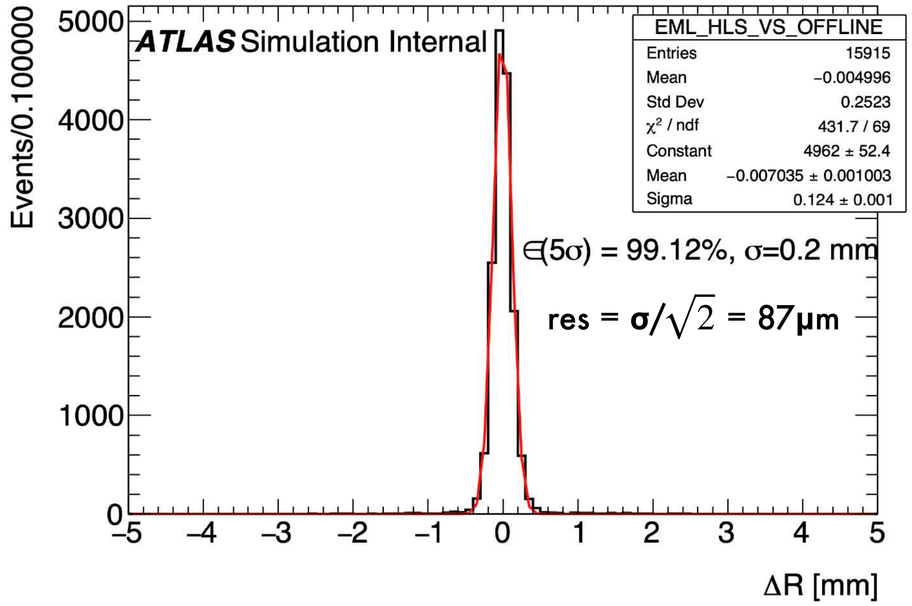
Histogram filling takes 2 clocks/hit (320MHz)

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	11573	1728000	0.67
LUTRAM	1096	791040	0.14
FF	16161	3456000	0.47
BRAM	22.50	2688	0.84
DSP	134	12288	1.09
BUFG	1	1344	0.07

LSF segment position - Firmware vs Offline reconstruction



MDT- TP Firmware integration

- **Integration of all firmware blocks for estimating the total FPGA resource usage**
  - Developer of common data-format package
  - Co-Developer of common test-vector generation using the offline simulation
- **Development of firmware test-benches using <u>cocoTB</u> (compare RTL results vs expected using python)**
  - Co-developer of the cocoTB framework to be used for functional and performance verification of the MDT-TP firmware
  - Developer of the LSF block test-bench

cocotb is a *COroutine* based *COsimulation TestBench* environment for verifying VHDL and SystemVerilog RTL using Python.

With cocotb, VHDL or SystemVerilog are normally only used for the design itself, not the testbench.

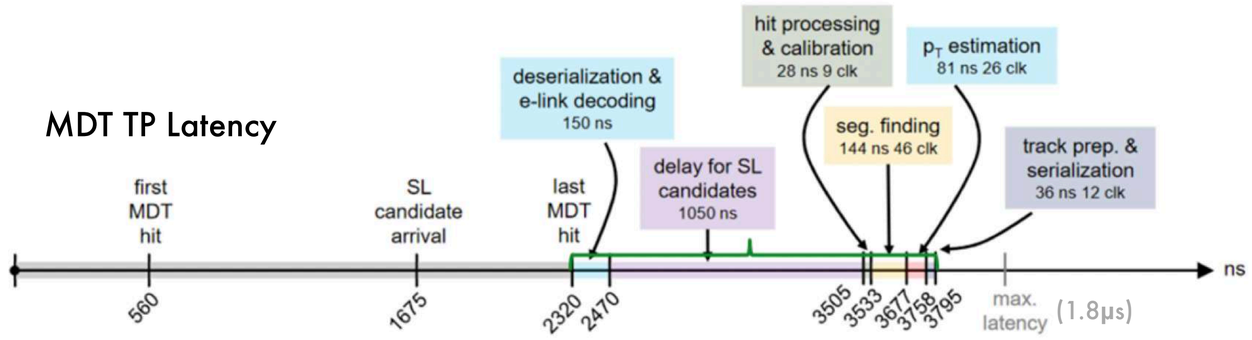
cocotb has built-in support for integrating with continuous integration systems, such as Jenkins, GitLab, etc. through standardized, machine-readable test reporting formats.

cocotb was specifically designed to lower the overhead of creating a test.

How does cocotb work?

A typical cocotb testbench requires no additional RTL code. The Design Under Test (DUT) is instantiated as the toplevel in the simulator without any wrapper code. cocotb drives stimulus onto the inputs to the DUT (or further down the hierarchy) and monitors the outputs directly from Python. Note that cocotb can not instantiate HDL blocks - your DUT must be complete.

MDT TP Latency



MDT TP Firmware Resource Utilisation Breakdown

Module	CLB Luts [10^3]	CLB Registers [10^3]	BRAM Tiles	Ultra RAMs	DSPs
Control Interface	14	16.5	4.5	0	0
HAL	110	211	0	0	0
DAQ	75.6	114.2	864	54	0
3 station H2S (LSF)	332.1	496.6	246	0	1233
MTC Builder	0.1	0.1	0	0	0
Pipeline	2.1	2.7	0	0	0
TAR	0.4	0.5	36	0	0
UCM	177	6.7	0	0	78
PT Estimation (mpt)	1.7	1.7	36	0	24
VU13P	1728.0	3456.0	2688	1280	12288
Total (LSF + MPT)	713.2 (41%)	850.1 (25%)	1186.5 (44%)	54 (4%)	1335 (11%)

Changed to single Ultrascale+ FPGA architecture

Summary

- **Research Experience**
  - ATLAS Muon NSW Upgrade (2010 - ongoing)
  - ATLAS Trigger Phase-2 Upgrade (2016 - ongoing)
  - ATLAS Muon Operations (2012 - 2016, 2020 - ongoing)
- **Experienced with coordination of teams and supervision of students in my past and current projects**
- **Engaged in outreach activities as ATLAS underground guide and with presentations about CERN and ATLAS NSW in different forums**

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Thanks for your attention