Level-1 Trigger (FPGA) + On-Detector Readout (ASIC)

Daniel Diaz
University of California San Diego
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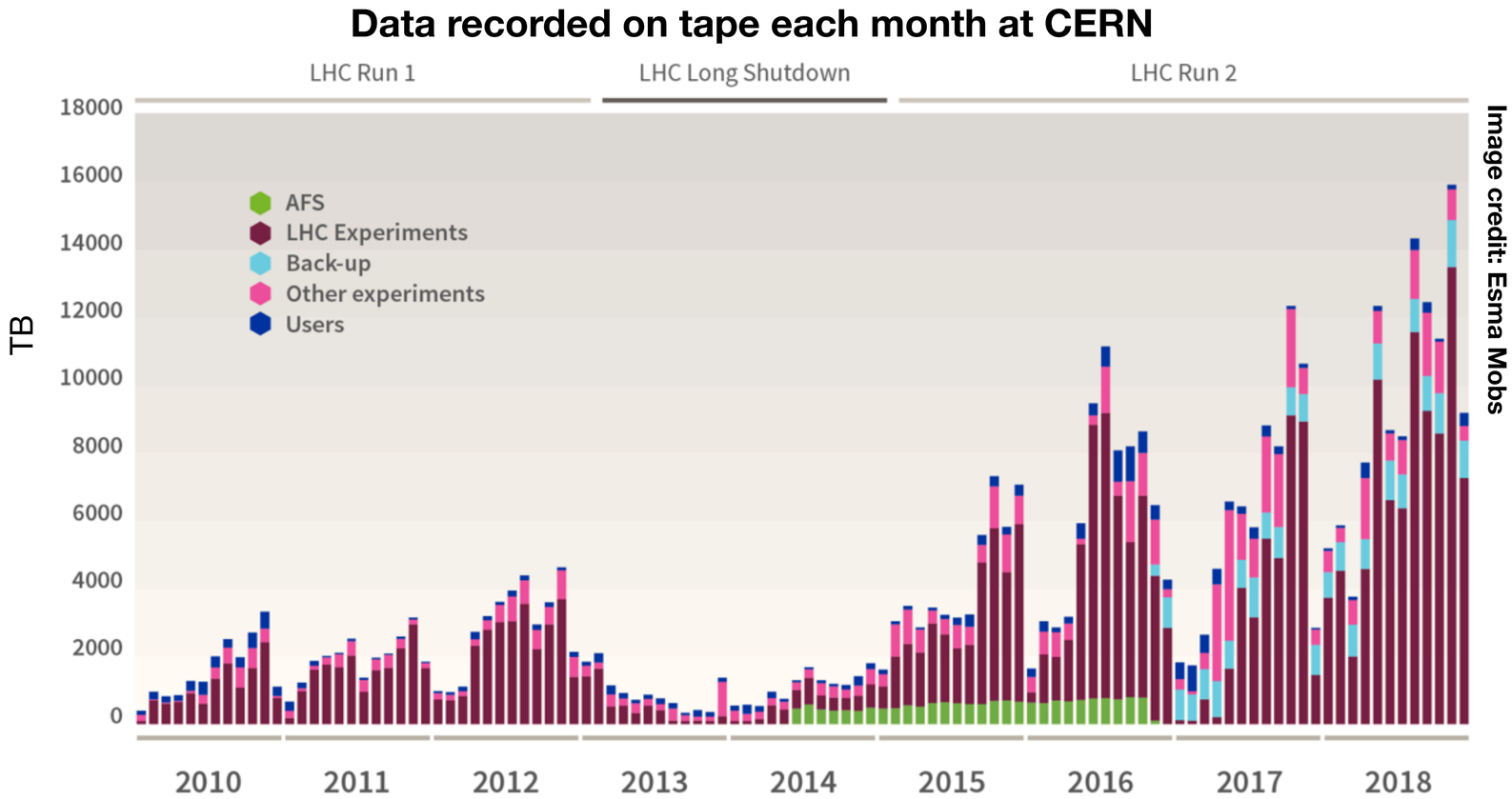
Data Collection @ the LHC

- Bunch crossings at the LHC occur every 25ns.
- LHC provides pp collisions at a rate of ~40 MHz.
- Data rate is increasing.
- Expected input rate ~63TB/s (1/10th the traffic seen by the world wide web)

Sophisticated algorithms and fast hardware are required to keep up!!



Data Taking Complexities

- In addition to data load there are a number of hurdles that make selecting data a complex problem.

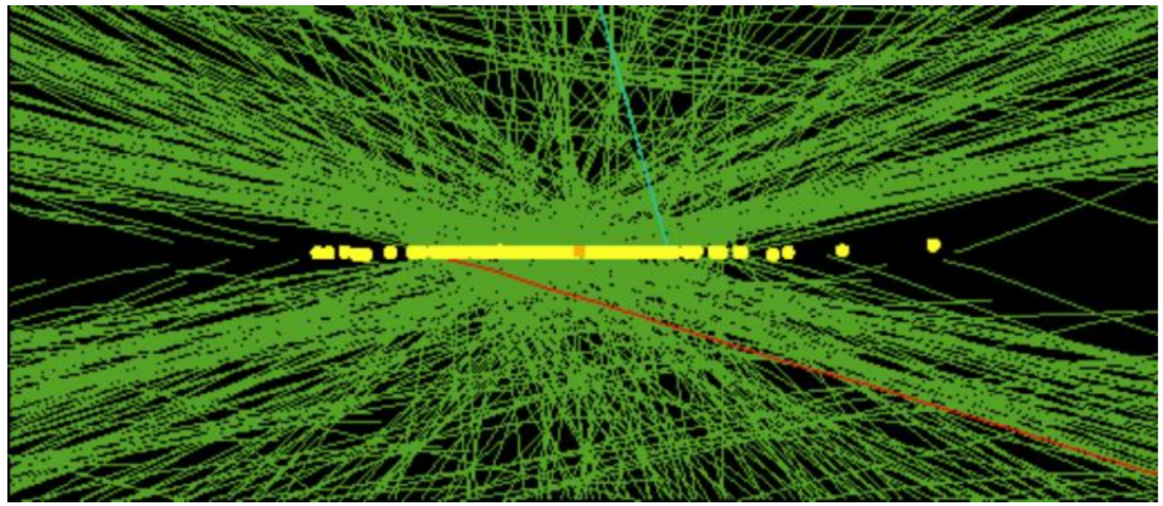
- Pileup

  - When an event of interests contains multiple additional reconstructed vertices.

  - We must decide quickly if the event contains interesting physics amongst the noise.

  - Increasing need for complex often ML-based algorithms to be used earlier in the reconstruction.

High PU event with 78 reconstructed vertices



PU is soon expected to be on the order of 200 vertices!!

Data Reduction @ the LHC (CMS)

- CMS uses a two-tier trigger system to reduce data load.
- Complex algorithms needed to reduce data rate at L1=> FPGAs a suitable choice.

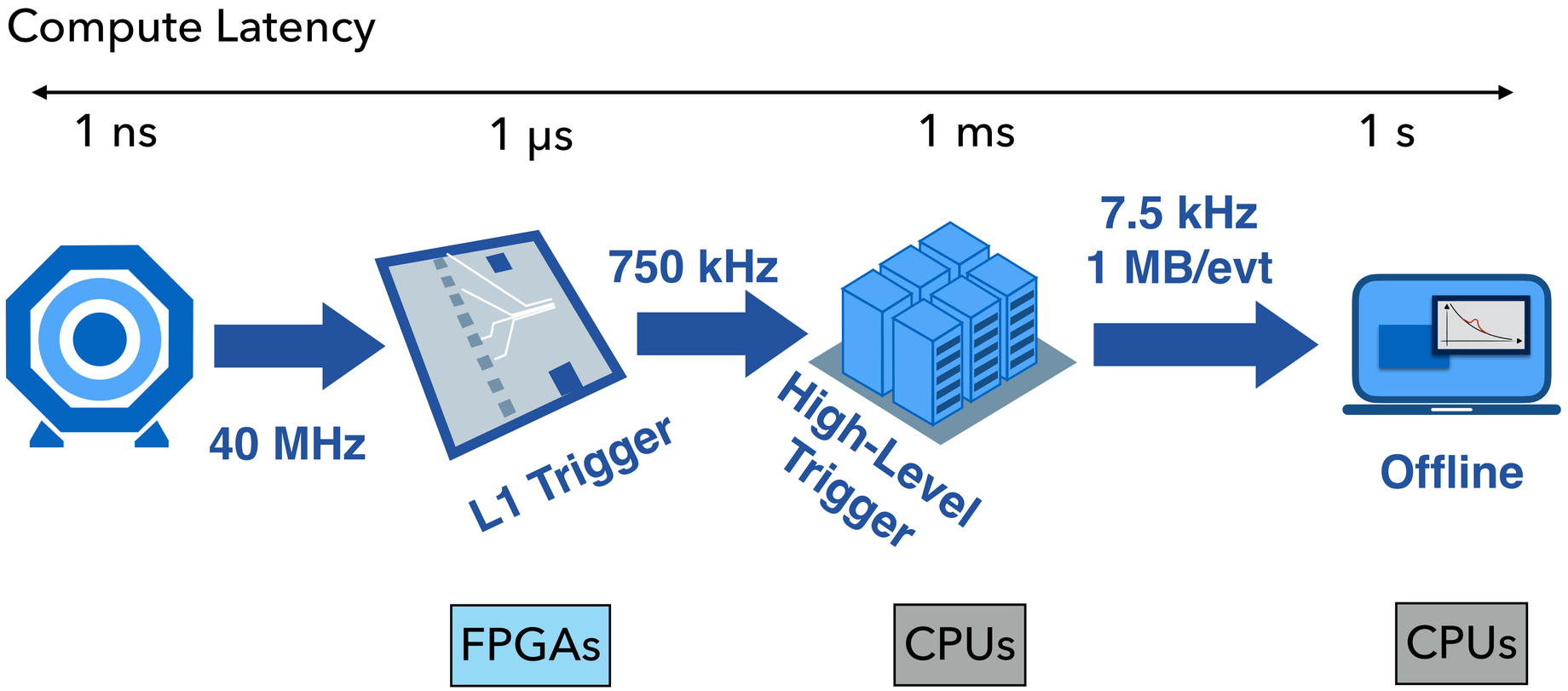
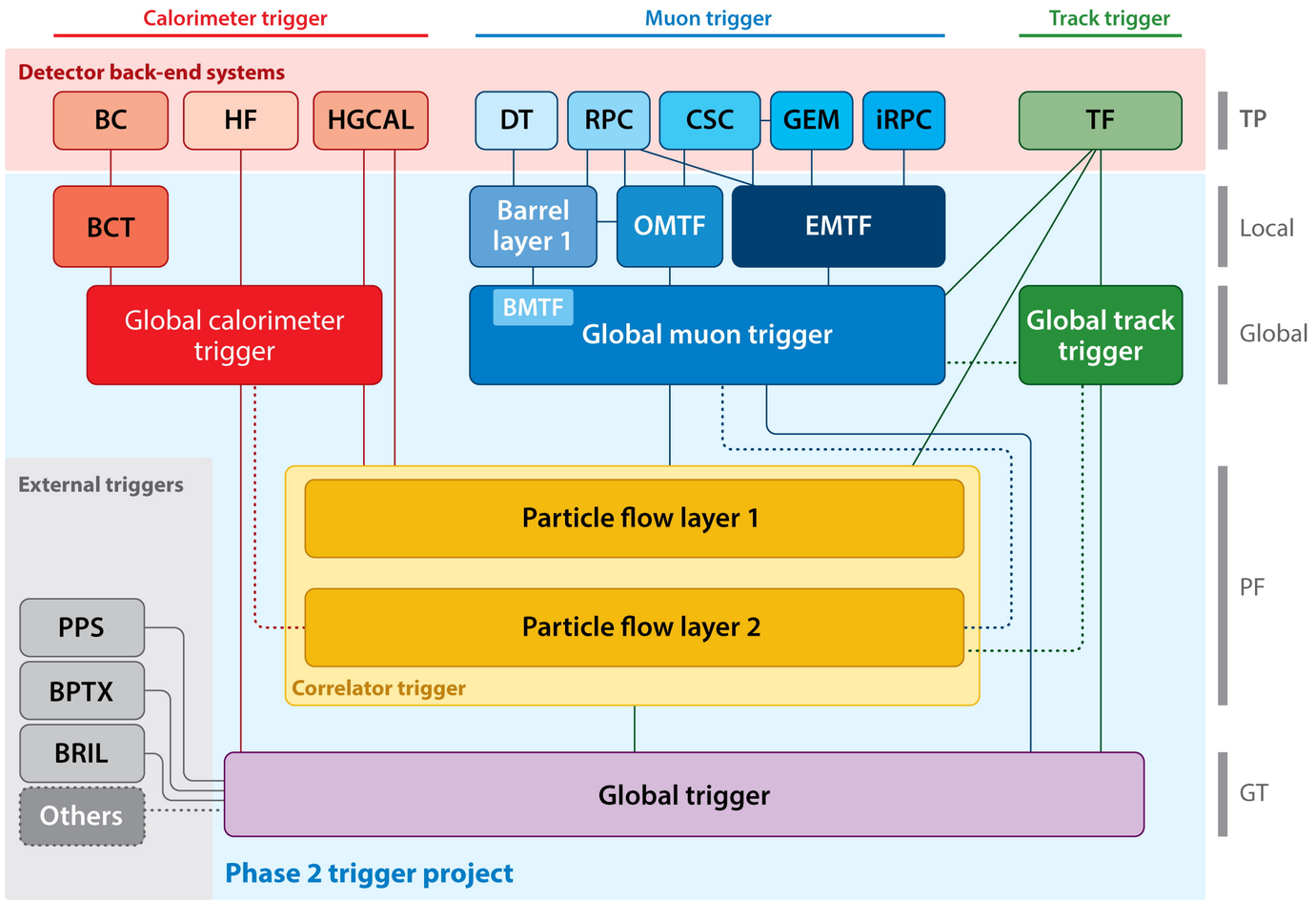


Image credit: Javier Duarte

Implementation

- Latency budget: 12.5μs
- Board allotment: 729 FPGAs
- Individual algorithms typically need to be <1μs.
- Individual algorithms
  - Typically occupy <1 board
  - Typically need to be run on all FPGAs to meet timing requirements.

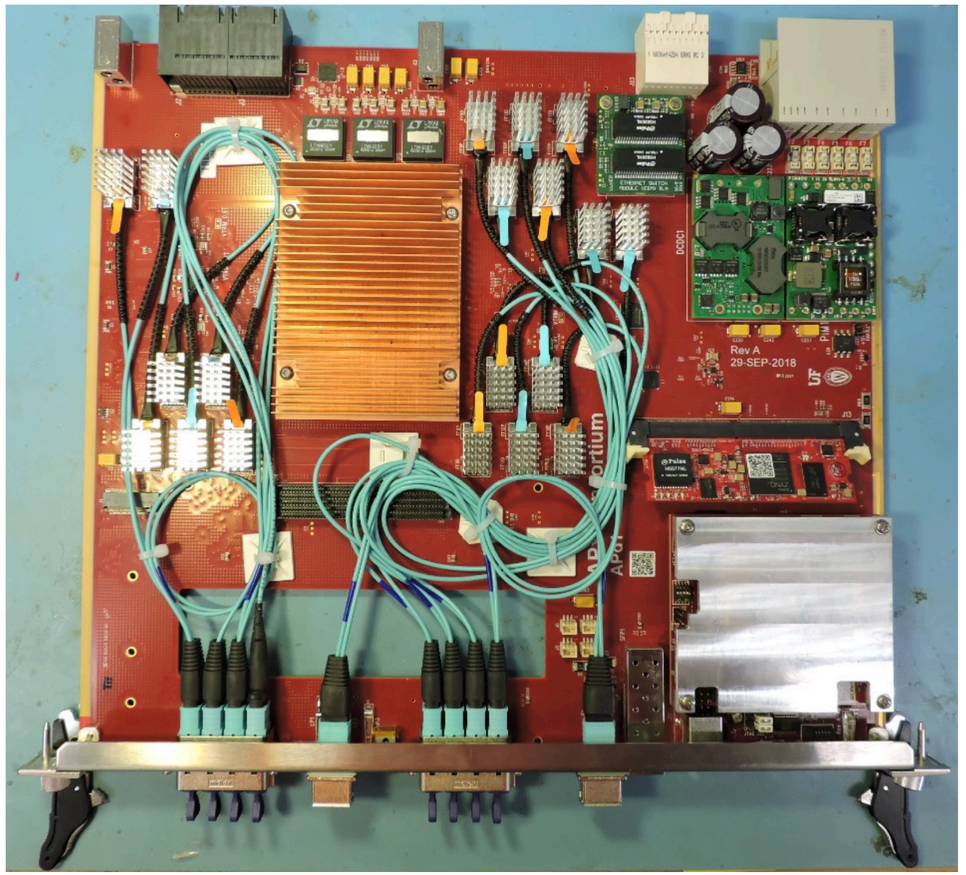


CMS L1 Trigger system overview for the HL-LHC

Ryd A, Skinnari L. 2020.
Annu. Rev. Nucl. Part. Sci. 70:171–95

FPGA Hardware and Programming

- CMS is targeting Xilinx Virtex UltraScale+ devices
  - 3 ATCA board designs in development.
    - Boards designed with firmware shell for hardware communication.
  - O(100) transceivers @ 28 Gb/s available (allows for increased bandwidth from upgraded detector electronics.)
- Devices can be programmed using HLS4ml package, providing the translation of complex algorithms from C/ python to Verilog required for FPGAs



CMS-TDR-021

hls4ml

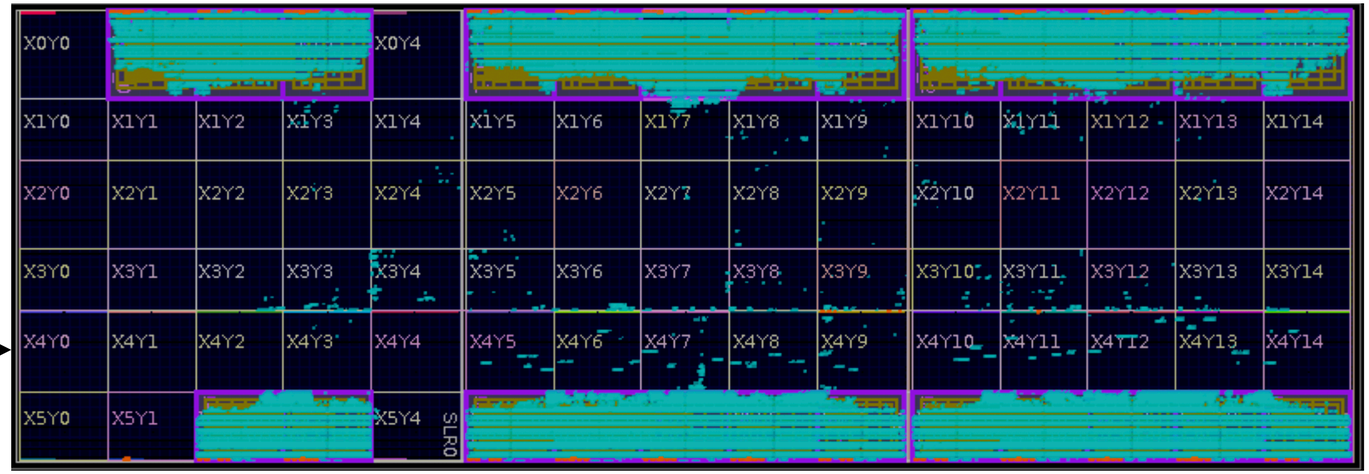
XILINX

Programming

- 3 Primary methods:
  - Custom RTL
  - HLS
  - HLS4ML

- Create an IP to deploy on the board
- IP needs to fit alongside board firmware.

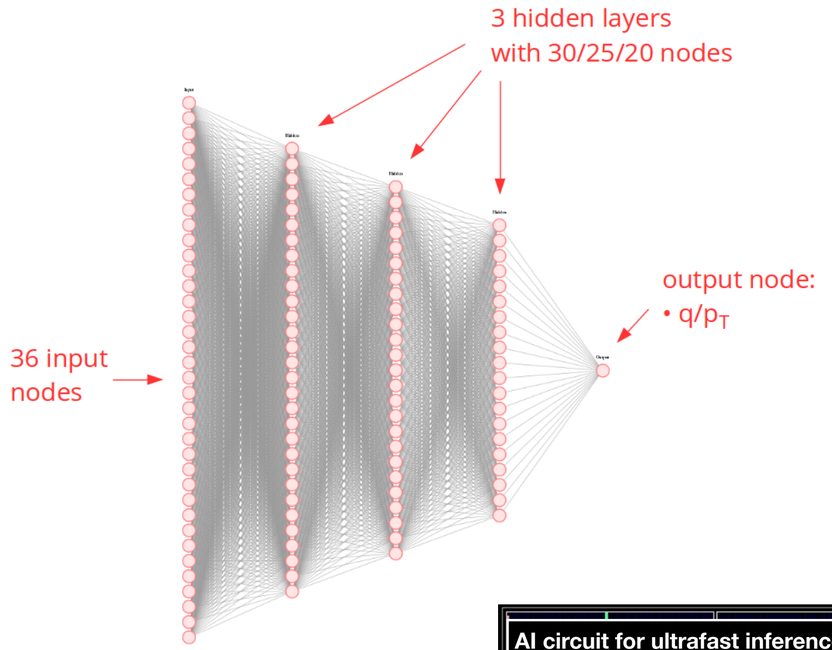
Occupancy of APx firmware in VU9P package

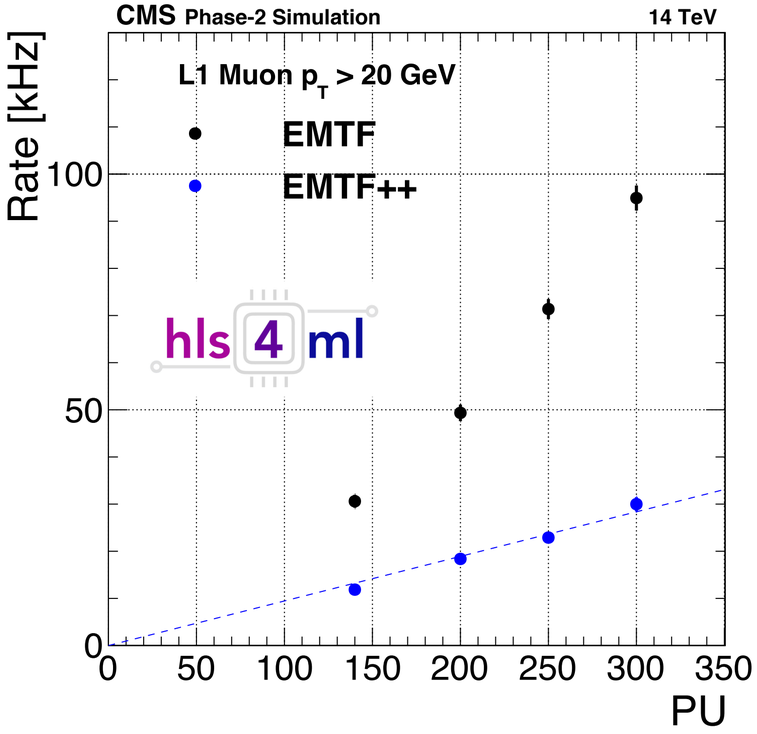


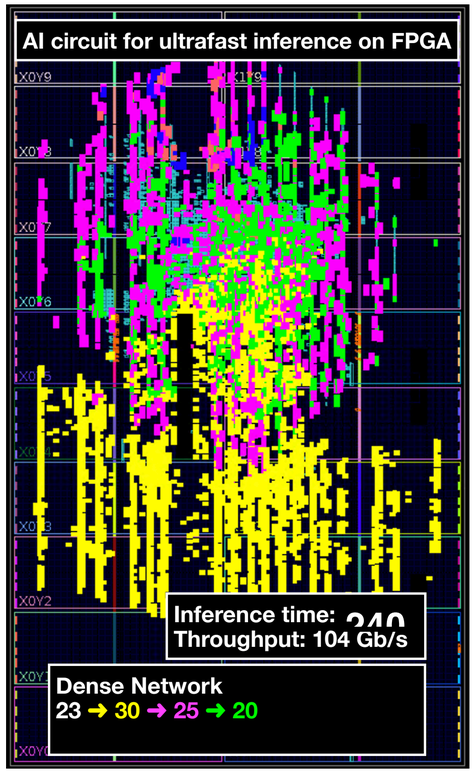
CMS-TDR-021

L1 Applications at CMS

- Endcap muon track finder EMTF++ (NN)
- Tau identification
- b-jet identification
- Auto encoder for anomaly detection
- VBF topology identification



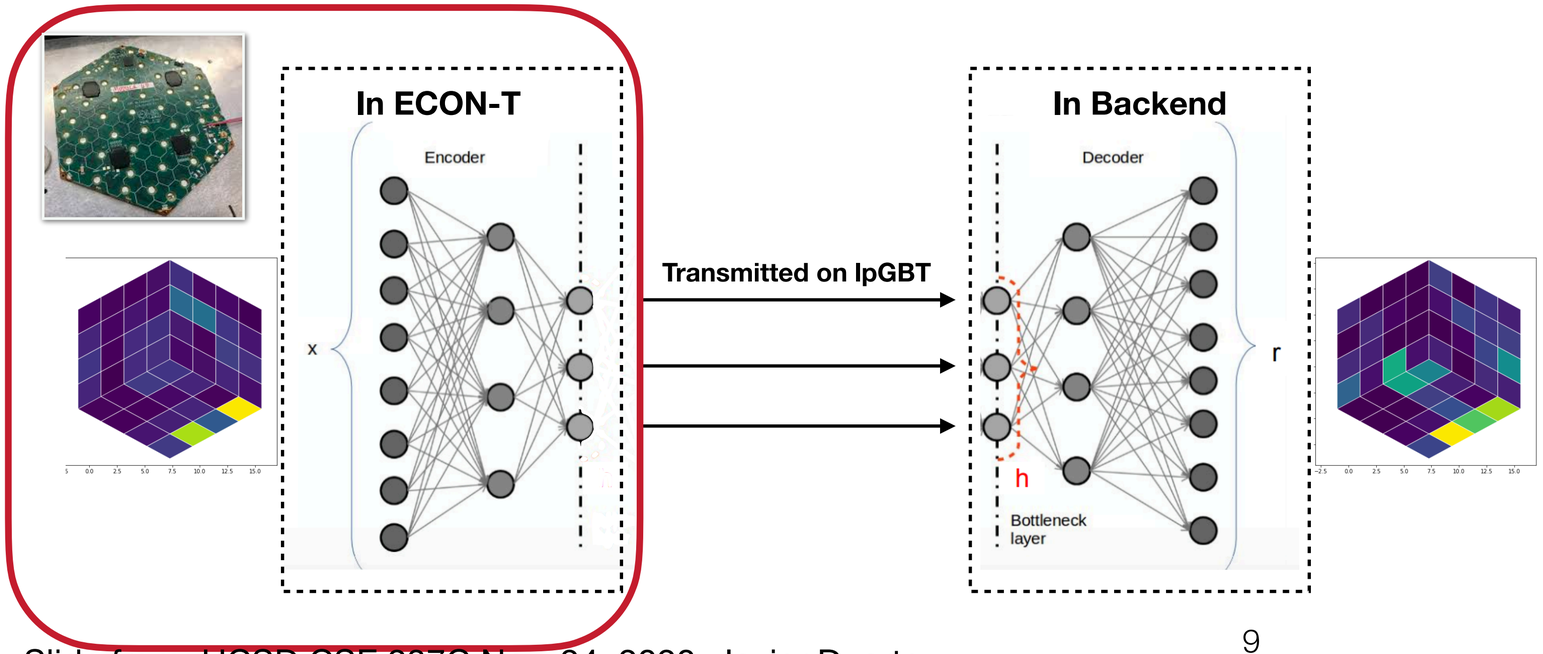




WHAT ABOUT ASICS?

https://indi.to/szYBS

- **Autoencoder** on the detector front-end for **data compression**
  - Application: **CMS HGCal ECON (data concentrator) ASIC**
  - ASIC required due to radiation tolerance and power requirements
- **Fully reconfigurable ASIC** to address: future unknowns including **evolving LHC conditions** (pileup, beam bkgd.), **detector performance** (noise, dead channels), **performance metrics** (resolution, substructure, new physics signatures)

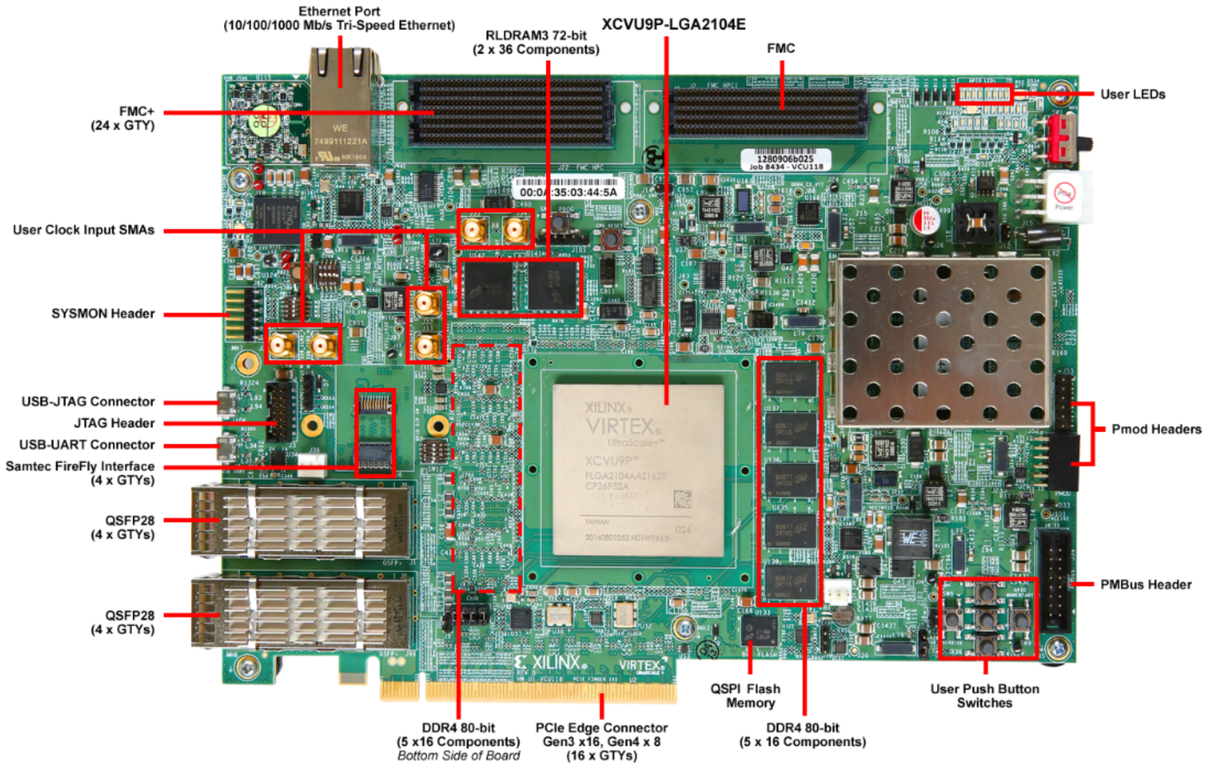
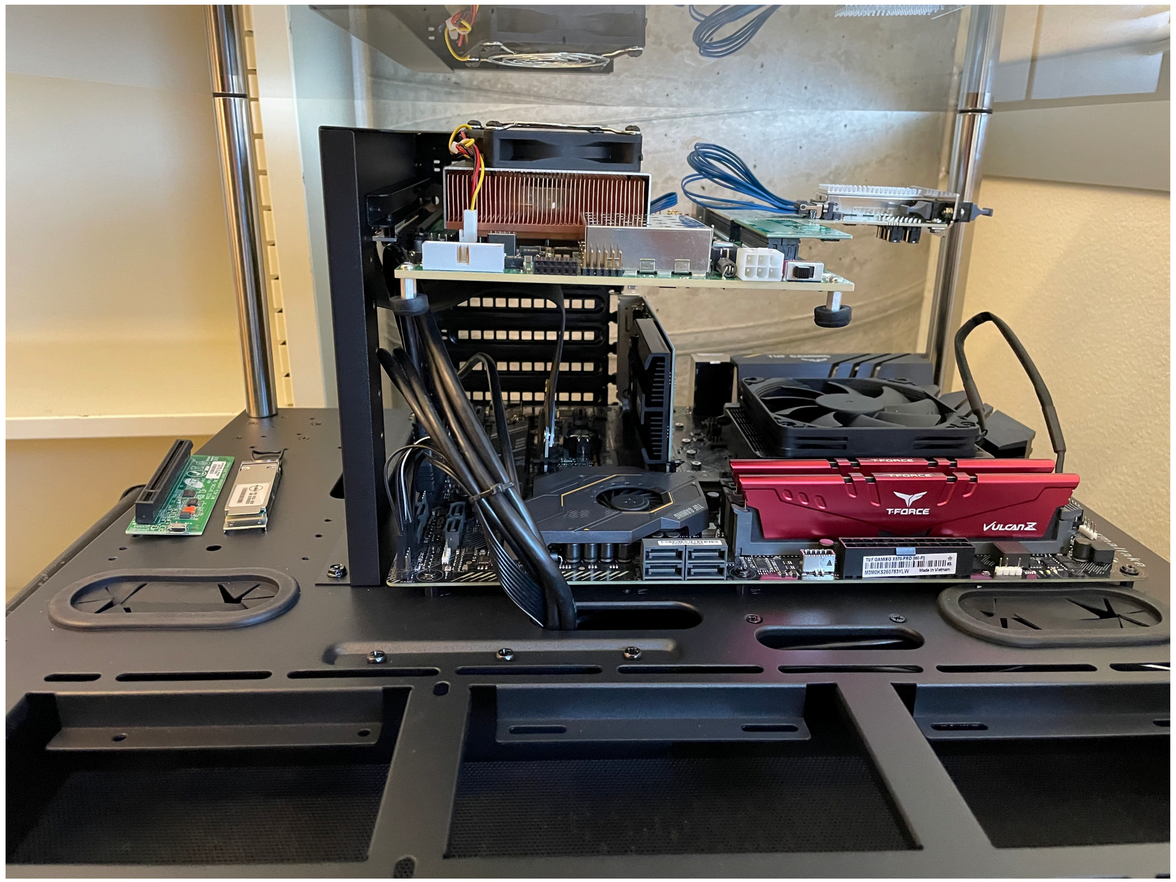


Auto-encoder design: Conv2D + Dense

Performance metrics defined based on energy mover's distance and physics resolutions/rates

QAT very important!

Slide from: UCSD CSE 237C Nov. 24, 2020; Javier Duarte

Test Stand Status UCSD

- Test stand operational at UCSD
- VCU 118 dev kit
- Operating with EMP framework.