Sleep Spindles as a Driver of Low Latency, Low Power ML in HLS4ML & TinyML

Hardware Development: Xiaohan Liu, Aidan Yokuda, Scott Hauck, Shih-Chieh Hsu
Neural Interfaces: Michael Nolan, Leo Scholl, Amy Orsborn
Neural Processing Algorithms: Trung Le, Eli Shlizerman

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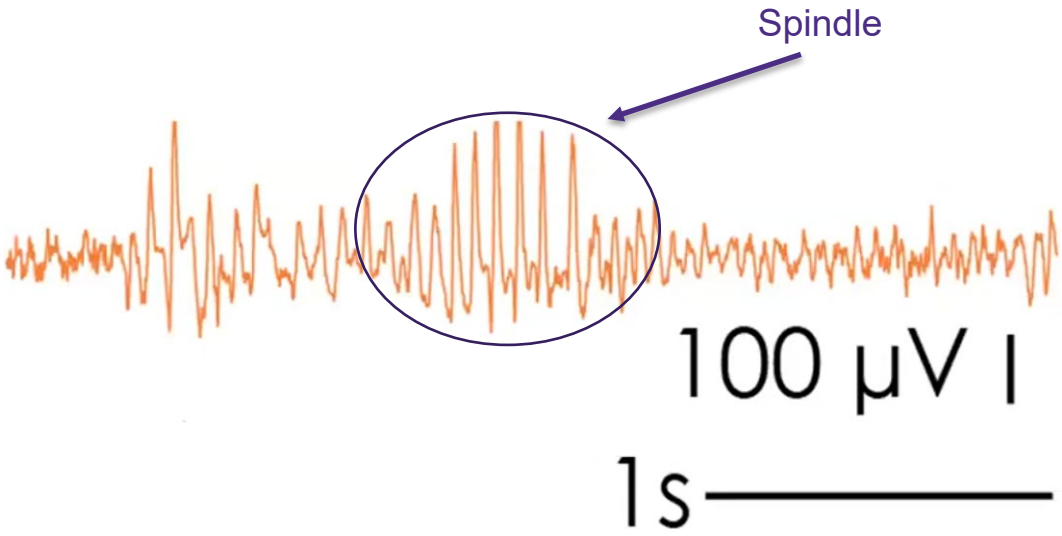
Interesting Neural Data – Sleep Spindles

Local Filed Potential Measurements
(electrical activity of groups of neurons)



Sleep Spindles Definition and Function

- Spindles are oscillation signals that occur during sleep or rest.
- Spindles believed to contribute to learn.

Current Development and Future Goal

- Currently: detect a spindle start and stimulate to disrupt.
- Goal: predict spindle will occur, stimulate to prevent.

Orsborn A, Shlizerman E, Dadarlat M. (2021) "Understanding & Interfacing with the brain: challenges and opportunities"

General Idea & Setup of the System

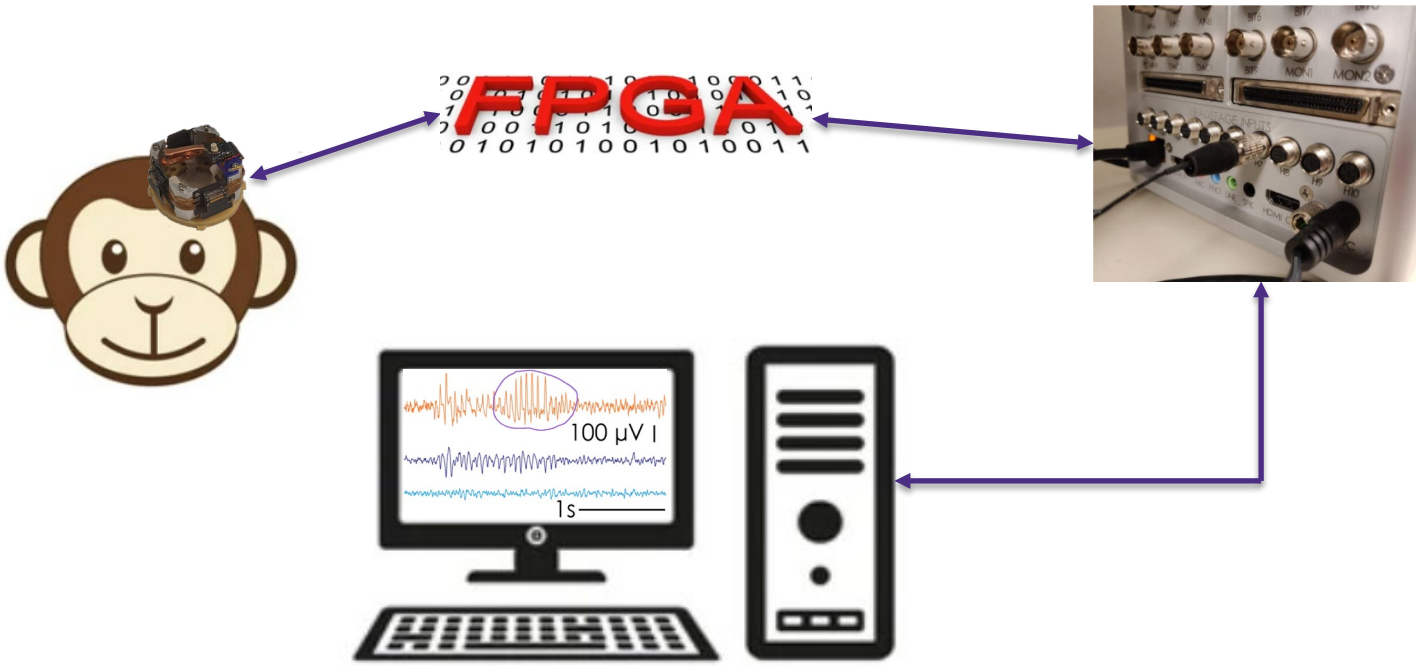
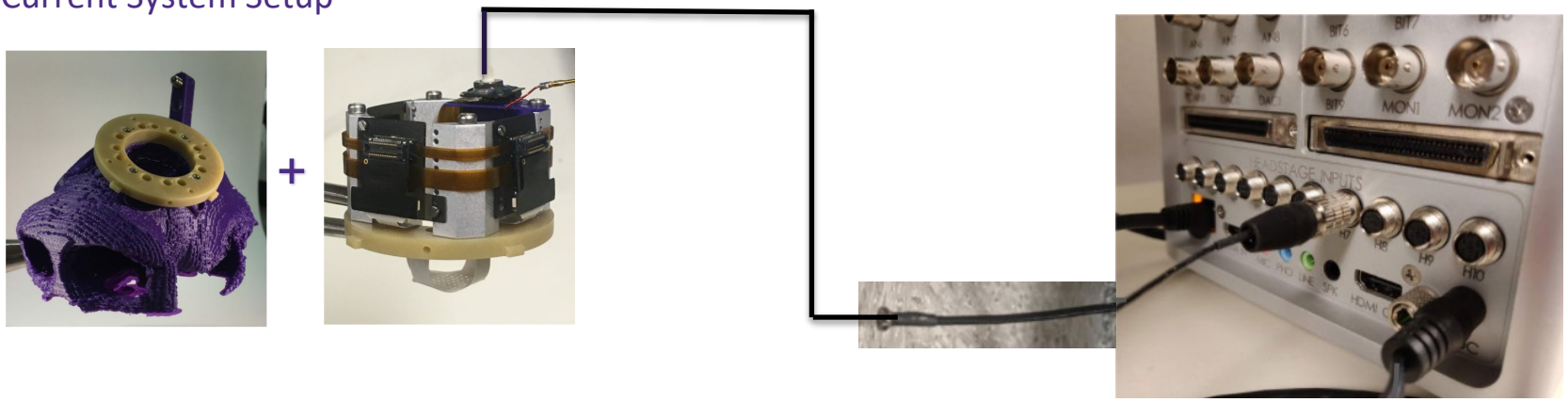


Image resources: Amy Orsborn's Lab, www.shutterstock.com, www.white-matter.com.

Orsborn A, Shlizerman E, Dadarlat M. (2021) "Understanding & Interfacing with the brain: challenges and opportunities"

Current & Future System Setup

Current System Setup



Future System Setup

Goal: Fully implemented FPGA add into the head-mounted device

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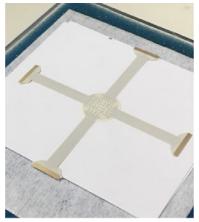
Image resources: Amy Orsborn's Lab, www.shutterstock.com.

Current Head - Mounted Device Setup

1 x Electrocorticography array with 4 ZIF arms



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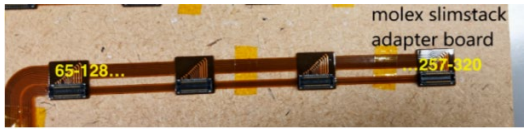
4 x Amplifiers

+

1 x ZIF Adapter board



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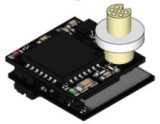
1 x Headstages



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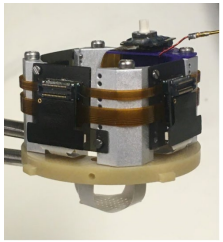
1 x Head-mounted device



HS-640

- **Channels**: 64
- **Weight**: 0.99g
- **Footprint**: 10.4 x 10.9 mm
- **Factory Modules**: mag-tether
- **Bandwidth**: 0.1Hz ~10kHz
- **Noise Floor**: 2.0 uV RMS (grounded inputs, full bandwidth)
- **Sampling**: 14 bit ADC, 25 kSps
- **Data Cable**: 6 wire ultra-fine gigabit cable (1.0 ~ 1.5mm, O.D, optional Kevlar sheath)

Image resources: Amy Orsborn's Lab, www.white-matter.com.

Related Researchers

Hardware Development Team

- Prof. Scott Hauck: Professor in UW ECE.
- Prof. Shih-Chieh Hsu: Associate Professor in UW Physics.
- Xiaohan Liu: MS student, HLS4ML for sleep spindle detection, FPGA board development.
- Aidan Yokuda: Undergrad, TinyML for ultra low power FPGA development.

Neural Interface Team

- Prof. Amy Orsborn: Assistant Professor in UW ECE & BioE.
- Leo Scholl: Postdoc, Neural mechanism analysis.
- Michael Nolan: PhD student, Neural data reconstruction with autoencoder-decoder.

Neural Processing Algorithms Team

- Prof. Eli Shlizerman: Assistant Professor in UW ECE & Applied Math.
- Trung Le: PhD student, Data alignment for autoencoder-decoder.

Project Timeline

Year 1: Investigate White Matter system, develop compatible FPGA system; load autoencoder algorithm into HLS4ML/TinyML flow.

Year 2: Demonstrate sample ML on 1st generation tethered power FPGA board. Obtain initial algorithm for sleep spindle detection.

Year 3: Push 2nd year sleep spindle detection algorithm into HLS4ML and load onto FPGA; Continue pushing algorithm developments into HLS4ML/TinyML.

Year 4: Use sleep spindle as a benchmark to test performance and revise any algorithm/hardware setup as needed.

Year 5: Complete fully battery powered deployment of final sleep spindle algorithm on testbed.

Thank you for listening!

Questions?