# ECAL-2 Free Running DAQ

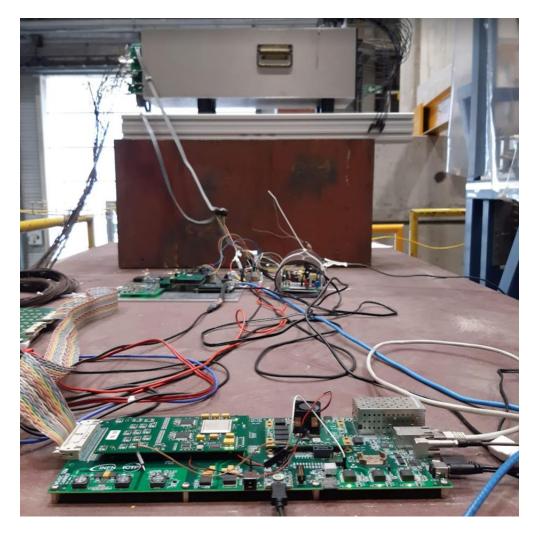
Global architecture, digital design, embedded programming, and data analysis

B. Valinoti, M.L. Crespo, A. Cicuttin, R. Molina, I. Morales, L. Garcia, S. Levorato,...

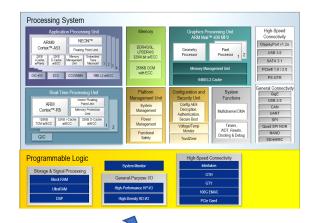


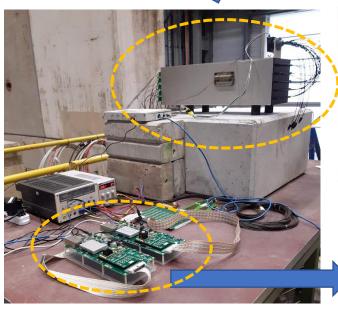


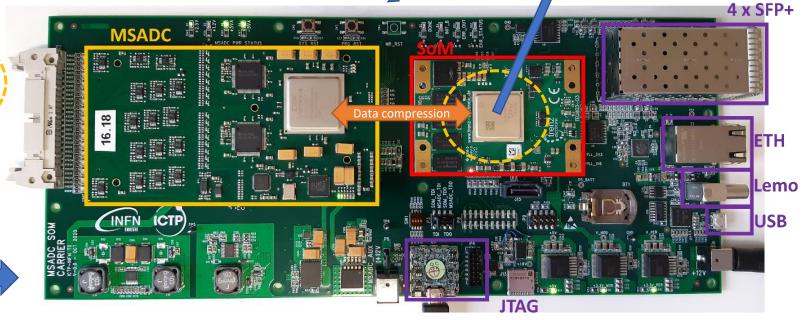




## **ECAL-2 MSADC SoM Carrier**







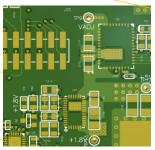




#### MSADC SoM Carrier V1\_1 (small redesign)



- Production 20 units
- Approx. for mid Dec'22
- Issues to find some components
- Redesign of power system 1.8V and Vaux, approx. 2-3 days





- Xilinx Zyng UltraScale+ XCZU9EG-1FFVC900E
- 2520 DSP block
- 32.1 Mb BRAM (embedded)
- 4GB DDR4 SDRAM (external)
- No stock, probable delivery date: Middle 2023

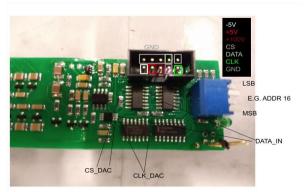


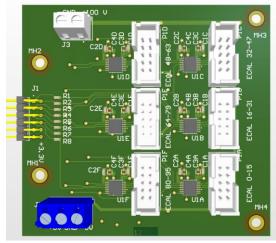
#### Control and distribution of the HV to polarize the ECAL2 PMTs.

ECALHV PCB prototype module was designed to handle the control and distribution of the HV to polarize the ECAL2 PMTs.

- Each module can control 96 Channels.
- Prototype implemented on a Zedboard Zynq xc7z020 and can handle 4 modules.













Current version is controlled using command line prompt script running on Python.

• Currently we are experiment with Quasar OPC running in the ARM microprocessor.



```
mlabadm@hp6g4-mlab-5: ~/my_gits/infn_pamp/SDK/udma_pamp/src
 File Edit View Search Terminal Help
Board communication
_____
close_server connect disconnect log udma x_change_cb
Comblock Read
_____
x_read_fifo x_read_mem x_read_ram x_read_reg
Comblock Write
x_ecal_ramp_all x_ecal_set_all x_write_fifo x_write_ram
x_ecal_ramp_ch x_ecal_set_ch x_write_mem x_write_reg
pAmp Control
========
adc500_cfg HVadj_set
                        imon read pas set
                                            vadj set
hv_pwrdwn HVadj_set_ramp pAmp_init set_dec_n vmon_read
Uncategorized
alias exit history py
                        run_pyscript set
                                           shortcuts
edit help macro quit run_script
                                     shell
```





#### **Network hardware**

#### Order already placed, some components arrived to CERN









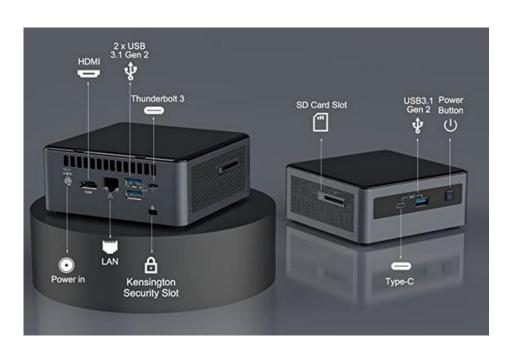


- 1 x FHD MTP®-24 Cassette, 24 Fibers OM4 Multimode, Type AF, MTP® to 24 x LC Duplex (Aqua), 0.35dB max
- 1 x FHD MTP®-24 Cassette, 24 Fibers OM4 Multimode, Type A, MTP® to 12 x LC Duplex (Aqua), 0.35dB max
- 10 x Cisco SFP-10G-SR Compatible 10GBASE-SR SFP+ 850nm 300m DOM Duplex LC MMF Optical Transceiver Module
- 10 x 20m (66ft) LC UPC to LC UPC Duplex OM4 Multimode PVC (OFNR) 2.0mm Fiber Optic Patch Cable
- 10 x 3m (10ft) LC UPC to LC UPC Duplex OM4
   Multimode PVC (OFNR) 2.0mm Fiber Optic Patch
   Cable





### PC – two units for interface, control and programming



#### NUC-Slim 8th Gen/8GB/240SS -- 514 euro

- Core™ i5, 8GB RAM, 240GB SSD
- Front 2 x USB 3.1 Gen2, Rear 2 x USB 3.1 Gen2
- 1000 Mbps Ethernet port
- 1 x HDMI
- CERN provided: not clear when available --> EDH Dec 2022

Buy	SCEM Code	Unit	Unit Price	Stock	Expected Delivery	Direct Delivery	DESIGNATION - DESCRIPTION	Data sheet - URL
( j	80.01.01.025.4	PC	718.0	0 i	14.12.2022	>=5 <b>i</b>	HP Elite 800 G9 Desktop Mini, i5, 16GB RAM. 512GB SSD, GbE RJ45 Port, 120W Power Adapter	<u>Lire la fiche</u> <u>technique</u>
Ê	80.01.01.026.3	PC	551.0 i	0 i	10.02.2023	>=5 <b>i</b>	HP-EliteDesk 800 G8 Tower i5/8GB/256 SSD	Read technical sheet
	80.01.01.029.0	PC	514.0	0 i	02.12.2022	>=5 <b>i</b>	NUC-Slim 8th Gen/8GB/240SS	Read technical sheet
							COEMA and an attended declare UD 000 OC Ministration and letter to the second of the s	





#### **100V Power source – W Ethernet interface**

#### **Thurlby Thandar Instruments PLH-P 250**

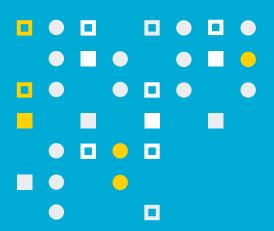




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#### SUMMARY

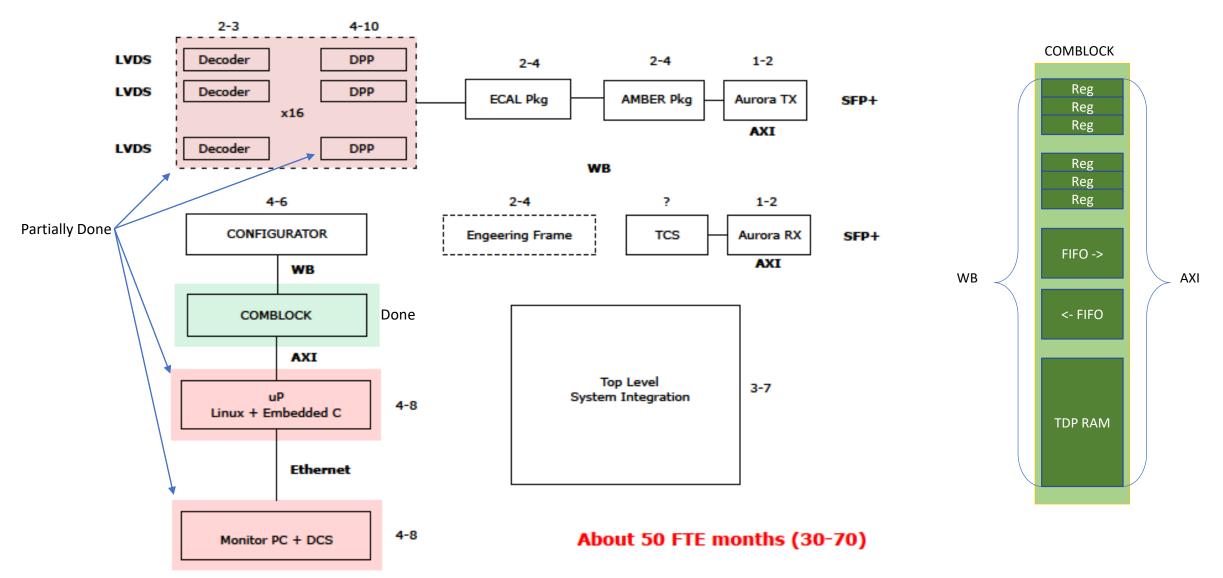
# Hardware Status



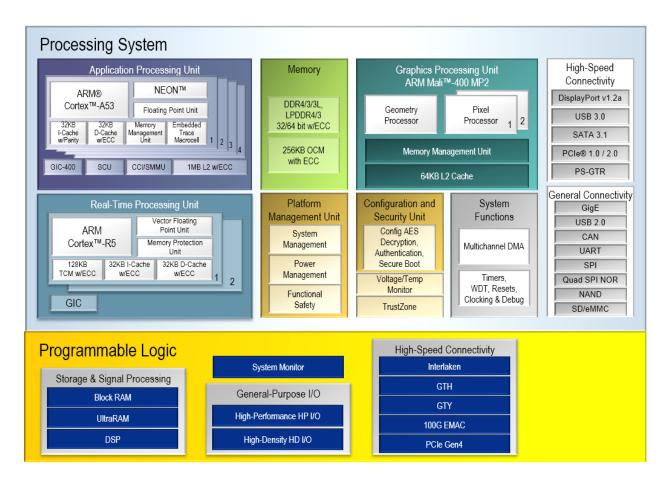
- Carriers production
  - 3 units V0\_0 (Oct-Dec 2020)
  - 3 units V1\_0 (July-Dec 2021)
  - 20 Carrier V1\_1: Requesting quotation these days
- System on Modules (Xilinx Zynq Ultrascale+)
  - 5 acquired and using
  - 20 expected by Middle 2023 (about 52 weeks from order)
- MSADC cards: from current ECAL2 front-end electronics
- HV Control board: Fully implemented and working.
   Production of new control boards batch
- PC for interface, control and programming: Two to be ordered
- Network hardware: Order already placed, some components arrived to CERN

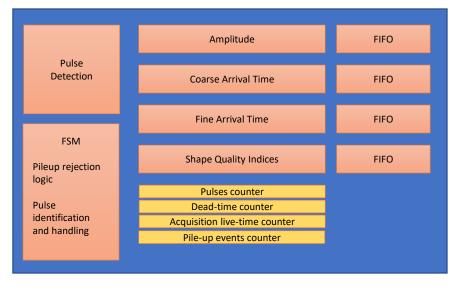
#### Firmware Development

Global Design Architecture Main functional blocks and their estimated development times (range in FTE months)



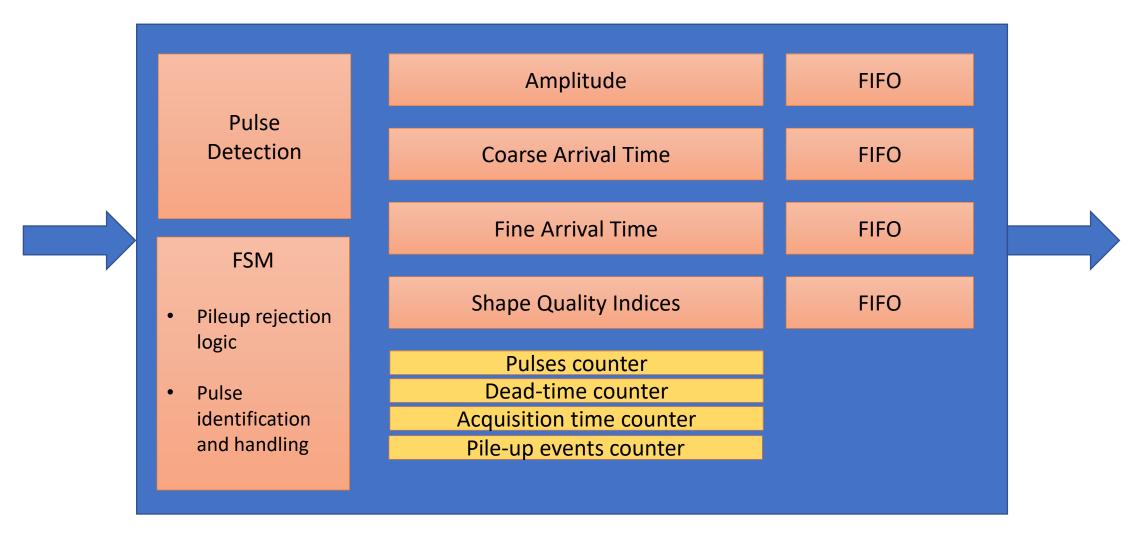
### Firmware Development: The Digital Pulse Processor (DPP)



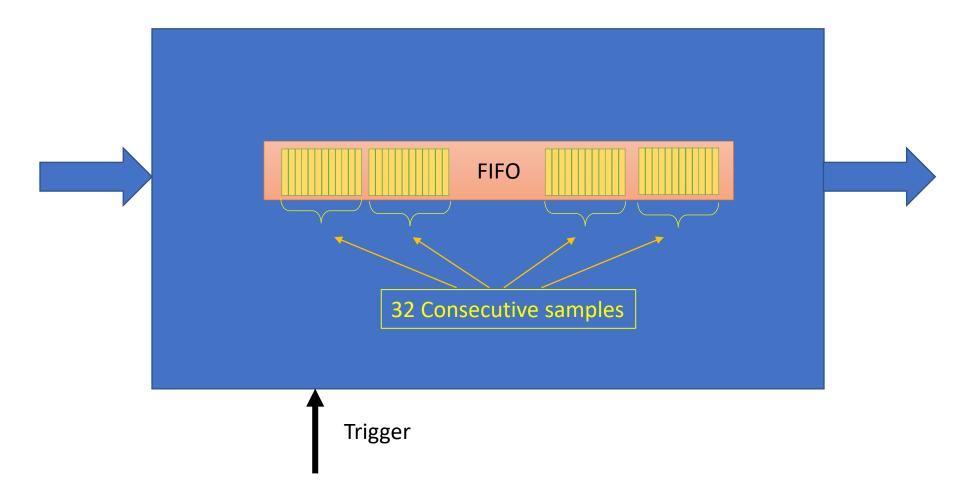




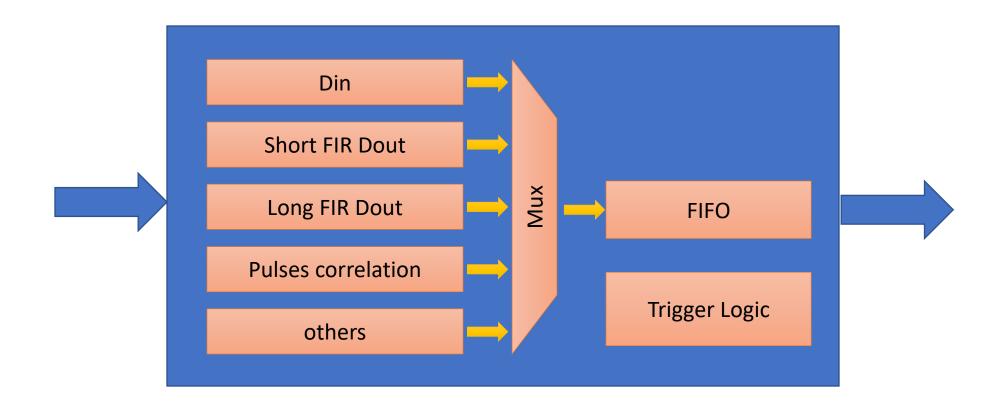
#### DPP: Possible features extraction in free running working mode



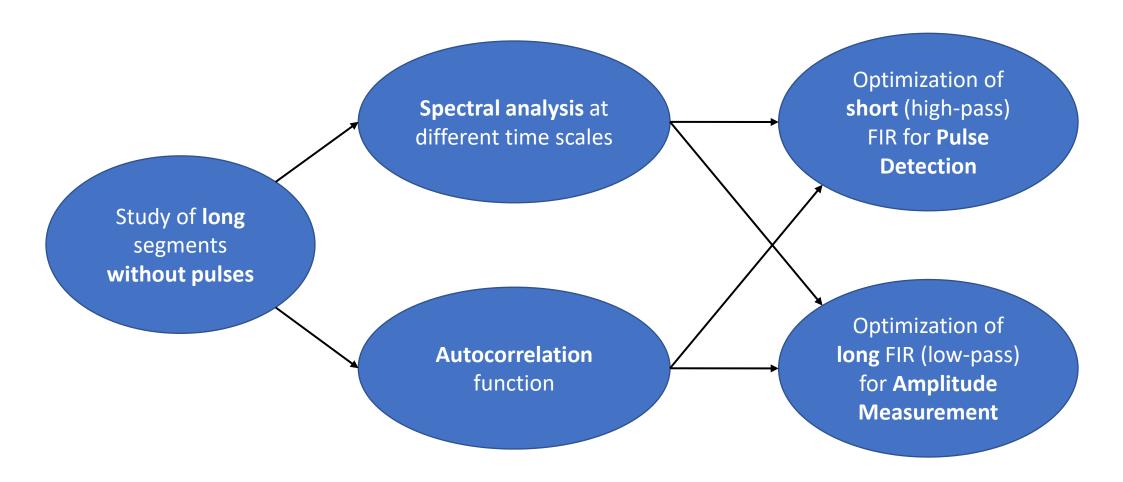
# DPP: Legacy (present) working mode



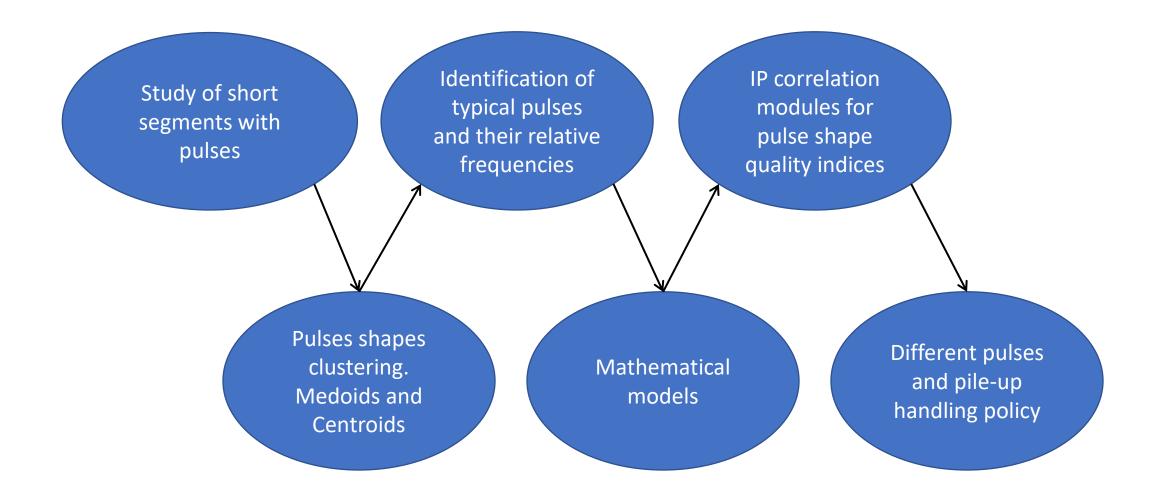
## DPP: Digital oscilloscope (debugging) working mode



## ECAL-2 Data Analysis I: Noise study



### ECAL-2 Data Analysis II: Signals study



# ECAL-2 Data Analysis III: New research lines



Machine Learning and ECAL2

Romina Molina

Trieste - Italy 1.04.2022

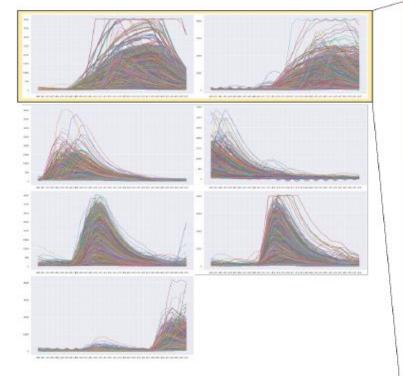


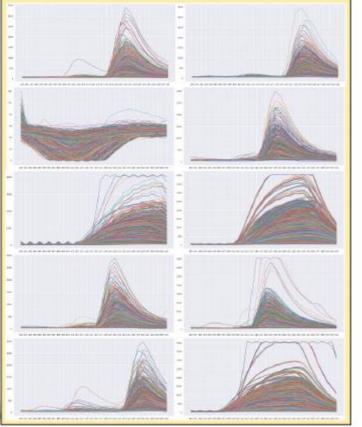




### **Centroid-based clustering**

#### Offline algorithmic pulse classification







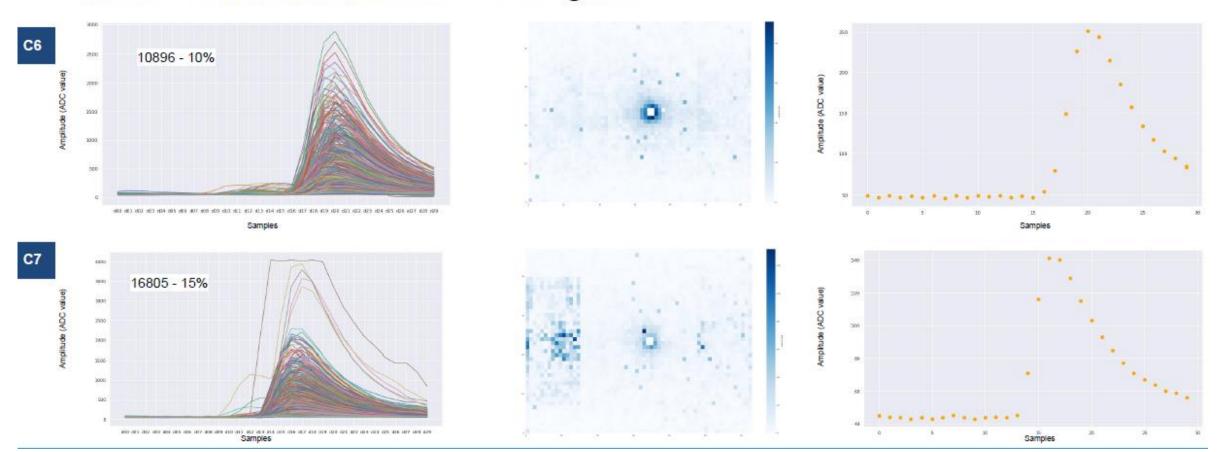




### **Centroid-based clustering**

#### Results - Second Iteration with 135129 signals

Possible debugging/diagnostic based on pulse shapes



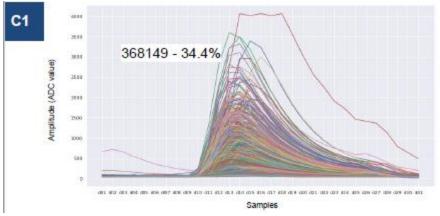


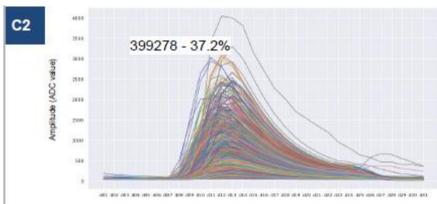


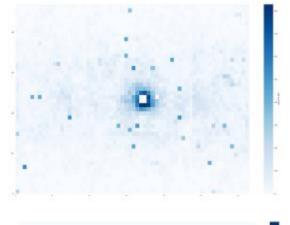


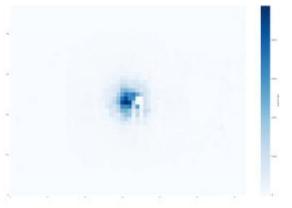
### **Centroid-based clustering**

#### Results - First Iteration with 1072747 signals









# Possible pulse shape based particle discrimination?

