



# A novel fast-timing readout chain for LHCb RICH LS3 enhancements and prototype beam tests

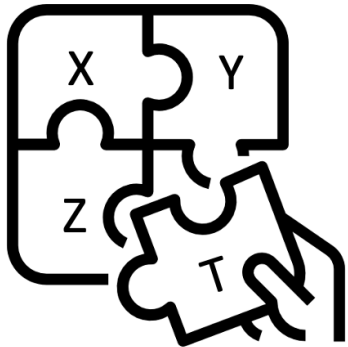
Floris Keizer on behalf of the LHCb RICH collaboration



11<sup>th</sup> International workshop on Ring Imaging Cherenkov Detectors,  
RICH 2022, 12–16 September, Edinburgh

# A time-resolved RICH detector

Promptly emitted Cherenkov photons + focusing mirror geometry  
= For each track the signal arrives ~ simultaneously



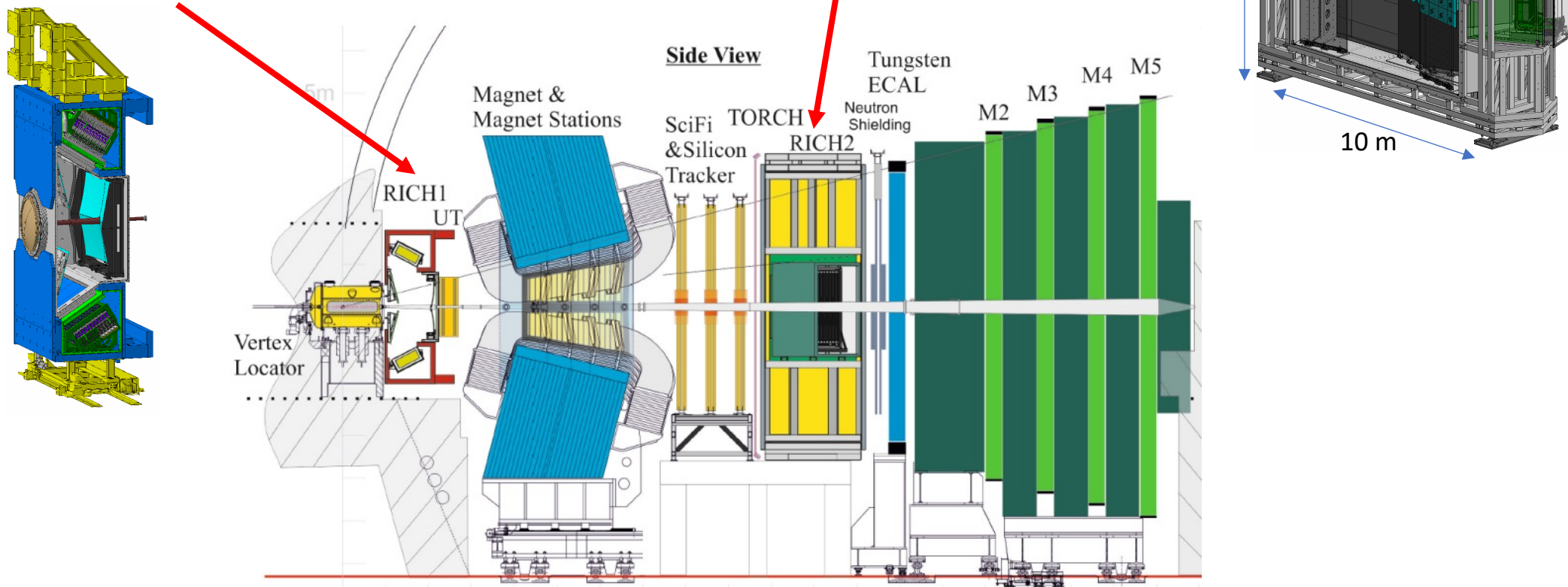
In this presentation, aim to address:

- **How** to make use of this feature to improve the PID.
- **Which** readout technologies and functionality to install during LHC Long Shutdown 3.
- **Prototype** developments and the ongoing test beam campaign.

# The LHCb detector layout

**RICH 1** ( $C_4F_{10}$ ) for charged hadron ID from 3 GeV/c (veto mode) to 65 GeV/c.

**RICH 2** ( $CF_4$ ) covering 15 to 100 GeV/c.



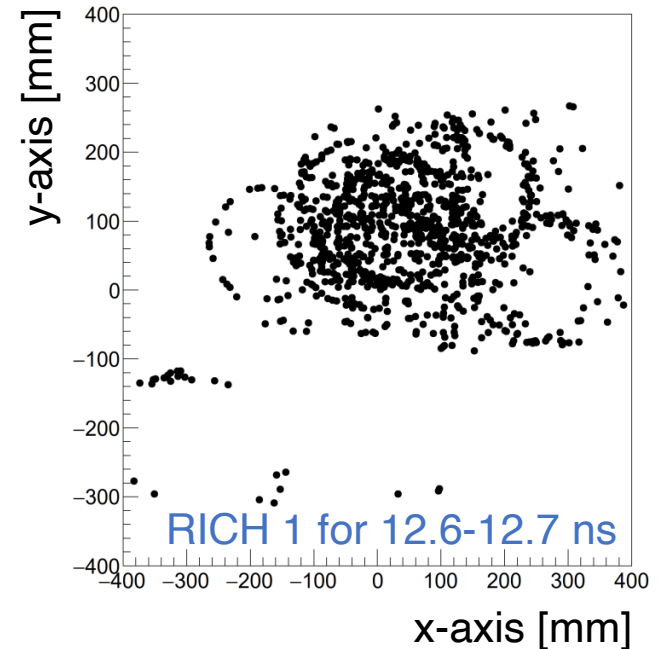
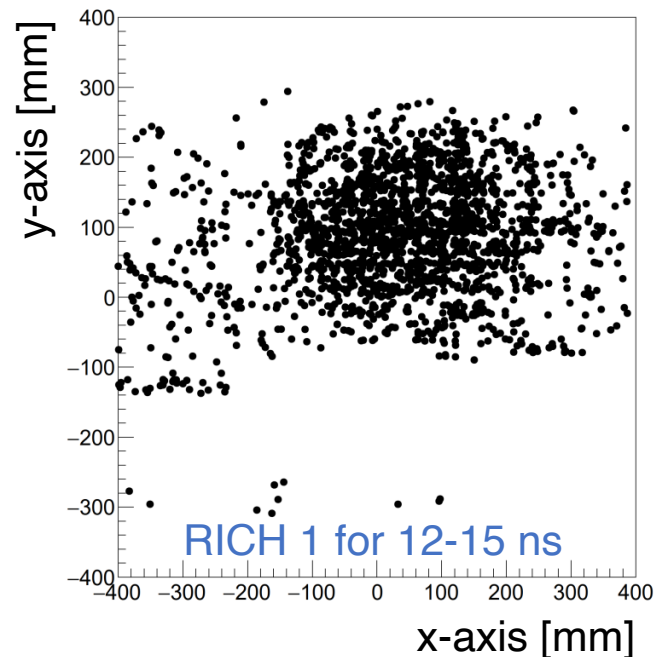
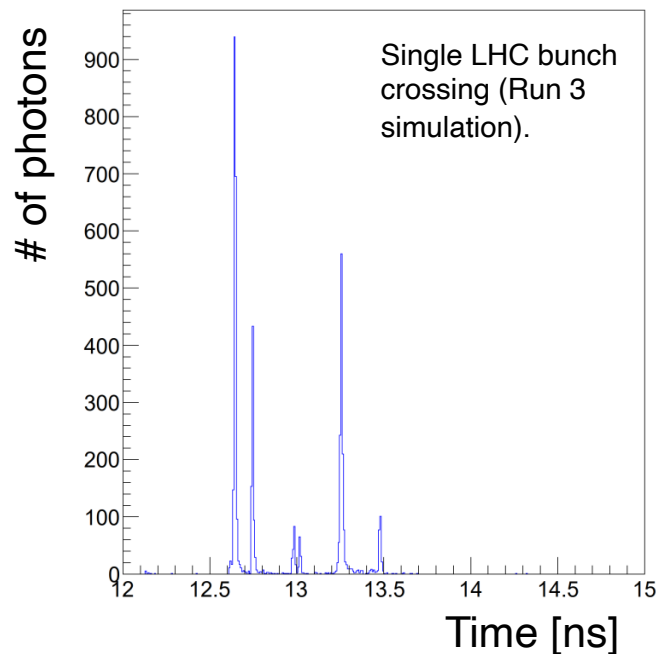
At these **relatively high momenta**, the particle time-of-flight differences are negligible. Instead, time information improves PID through (combinatoric) background reduction.

# Hit map for a single LHC bunch crossing (Run 3 simulation)

Simulating the Run 3 detector with an 'ideal' photon detector with zero time jitter shows distinct peaks originating from different Primary Vertices (PVs).

- In practice, the photon detector time **resolution blurs** the image in time.
- The RICH reconstruction maximum-likelihood approach works with **tracks and single hits**.

To reduce background and improve PID, need to accurately predict **when** the photons from a given track ought to arrive.



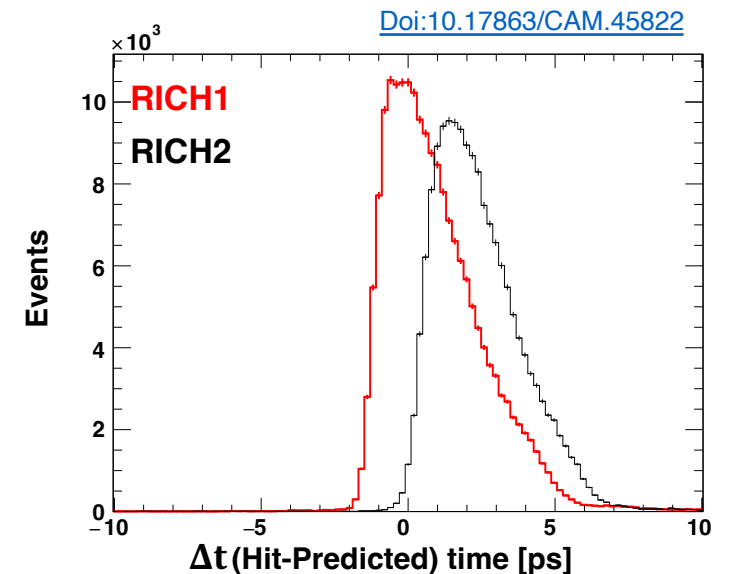
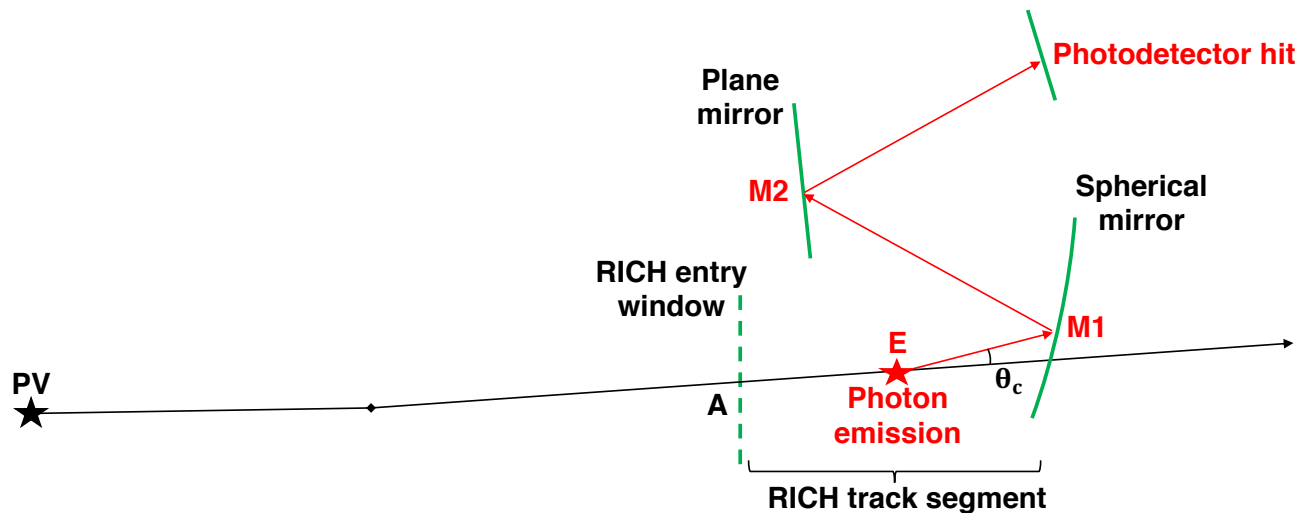
# RICH photon hit times are predictable to within 10 ps

The reconstruction algorithm **already finds the track and photon paths**.  
Combined with the **PV t-zero**, the photon hit time can be predicted.

$$t_{\text{predicted}} = t_{\text{pv}} + t_{\text{track ToF}} + t_{\text{photon ToF}} (+\text{RICH2 correction for curved tracks})$$

Considering all contributions, obtain a **prediction of better than 10 ps**.

- Faster detectors are better, as in practice the photon detector resolution will limit the performance.

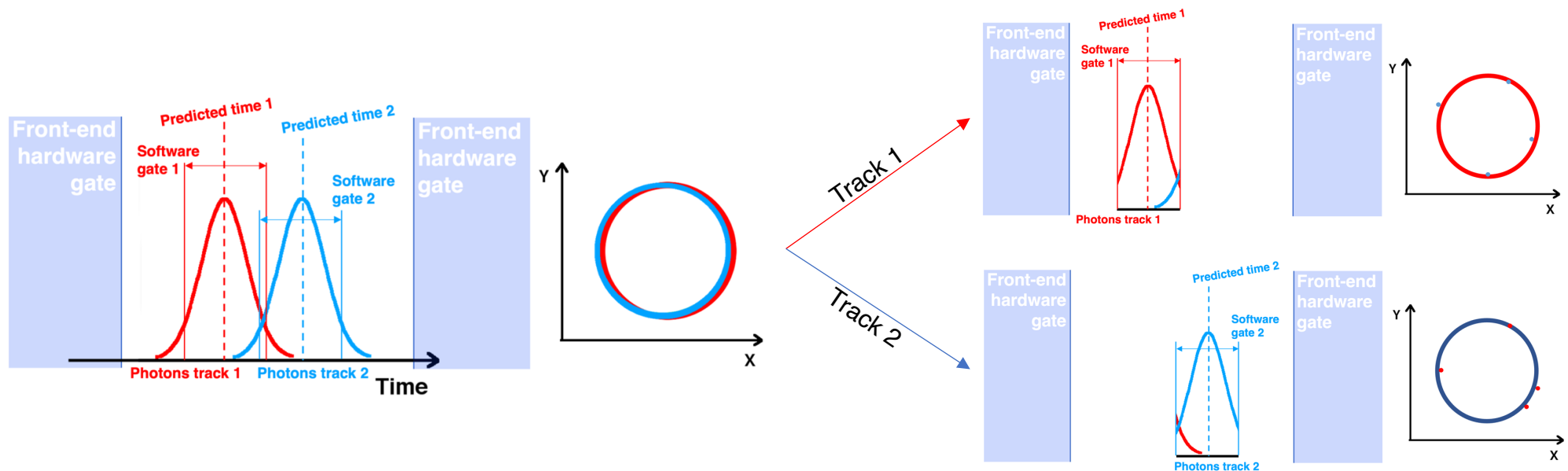


# How to use time information: shutter and timestamp

1. At the front-end ASIC, apply a **nanosecond-scale “shutter time” to save bandwidth.**  
Width includes time-walk, PV spread, photodetector jitter and ‘track + photon’ path-length variations.
2. Within the shutter, give all hits a **picosecond-scale timestamp to improve PID.**  
Can be used to apply a software time gate during the event reconstruction.

Width of the software gate :

- Must be large enough to accept sensor spread and small enough to reduce combinatoric background.
- $\pm 2\sigma_{\text{sensor}}$  was found optimal.
- **Oversampling** in the readout electronics helps to tune the width of the gate.



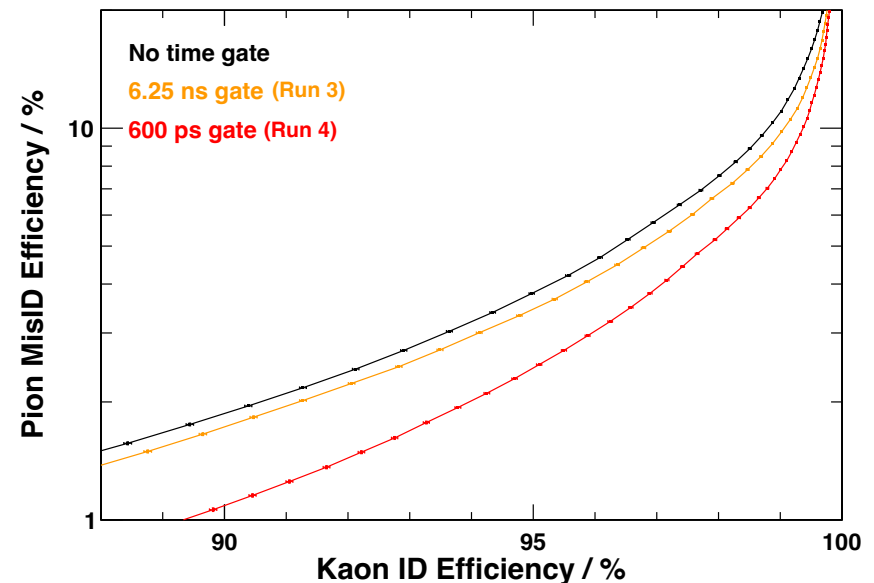
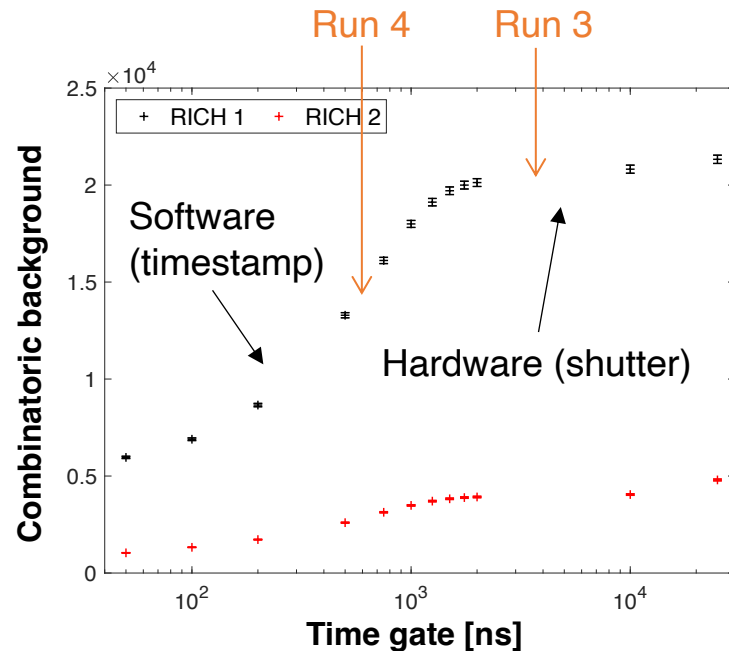
# Time gate in reconstruction software

For the Run 4 MAPMTs with  $\sigma_{\text{sensor}} \sim 150$  ps, the optimal software time gate is  $\pm 2\sigma \sim 600$  ps.

- FastRICH ASIC with  $\sim 25$  ps bins can be coupled to new sensors with improved time resolution for Upgrade II.

Significant improvement in PID performance with time gate (PV time from MC).

- MAPMT noise (dark counts, SIN) not included; purely photon backgrounds.
- Subsequent effect on selected physics channels was demonstrated in note [LHCb-PUB-2021-009](#) with up to 70% background reduction.



# RICH estimate of Primary Vertex (PV) t-zero during Run 4

The PV “t-zero” is a key parameter for the predicted RICH detector hit time.

- Using LS3 electronics enhancements, RICH can standalone estimate the PV t-zero.
- New measurement for the RICH detector and LHCb.

Variation of the expression on slide 4.

$$\langle t_0 \rangle_{PV} = \sum_{\text{true phot} \leftrightarrow \text{PV relations}} [t_{\text{hit}} - t_{\text{track ToF}} - t_{\text{photon ToF}}]$$

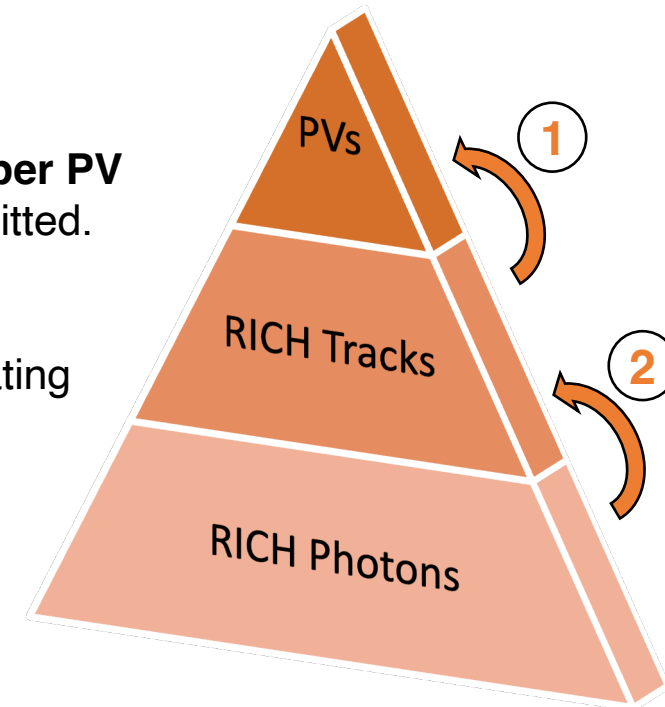


**Main challenge is to correctly associate photons to their PV.**

- **Oversampling** in electronics of the **multitude (hundreds) of photons per PV** allows the relatively large MAPMT transit-time spread ( $\sigma \sim 150$  ps) to be fitted.
- Stage 1: Using LHCb tracking container for PV reconstruction.
- Stage 2: Cuts (first studies) or iterative (alternative, but more CPU) approach inside the RICH algorithms to reduce combinatorics in associating photons to tracks.

**First (preliminary) studies** showed a resolution better than 100 ps at least for a subset of PVs in the full LHCb simulation.

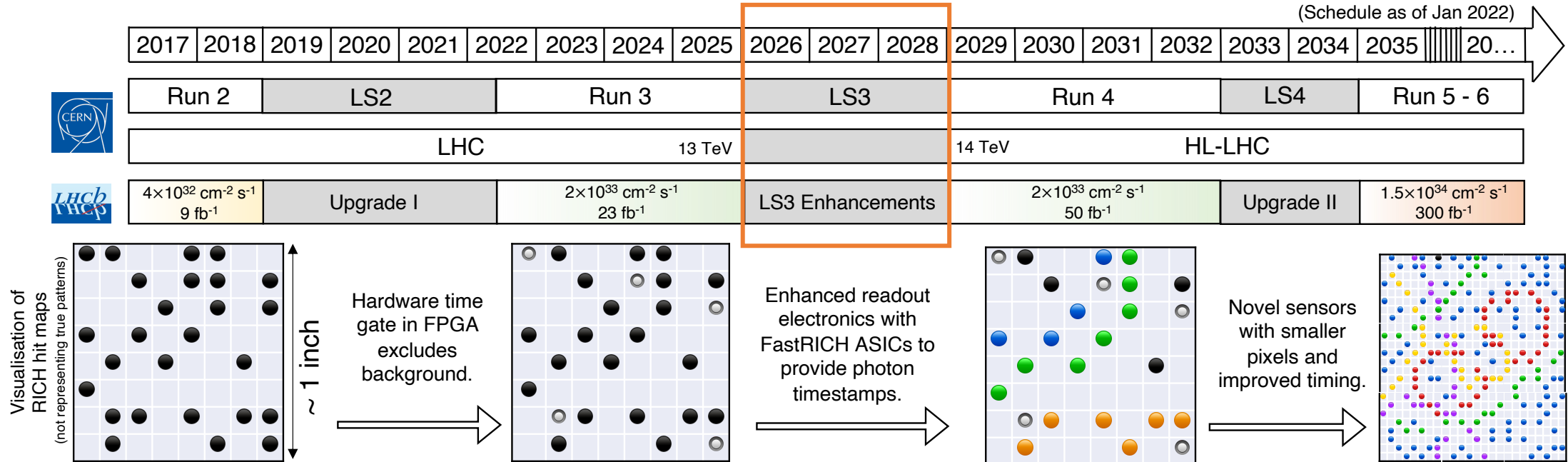
- Further software R&D foreseen.





# Evolution of the RICH photon detector

Relatively long period of LS3 central to the RICH evolution.



- LS3 / Run 4 : focus on **FastRICH** readout electronics with fast timing and wide input dynamic range.
- LS4 / Run 5 : focus on **sensor technology**. Fast-timing is essential for the luminosity challenge after Upgrade II. [[Talk](#) by Stephen Wotton]

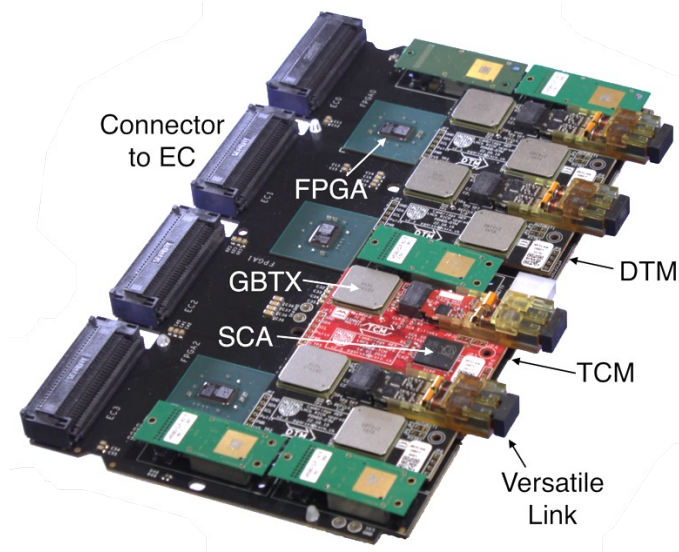
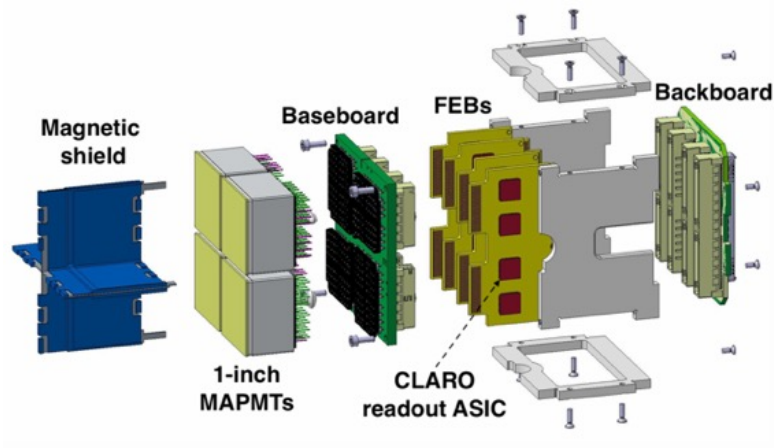
# Run 3 photon detector and hardware shutter time

Run 3 MAPMTs are read out by CLARO ASICs to shape and discriminate signals.

- Digital board with FPGAs samples the digital signals at 320 MHz (3.125 ns), formats the data and transmits the data using GBTX ASICs.
- Allows **hardware shutter** to be implemented. Still only 1 bit/hit output: no timestamp. The shutter is limited to 3-6 ns by CLARO time-walk.

Approach limited by **radiation hardness of the FPGA** and by **clocking / logic resources**.

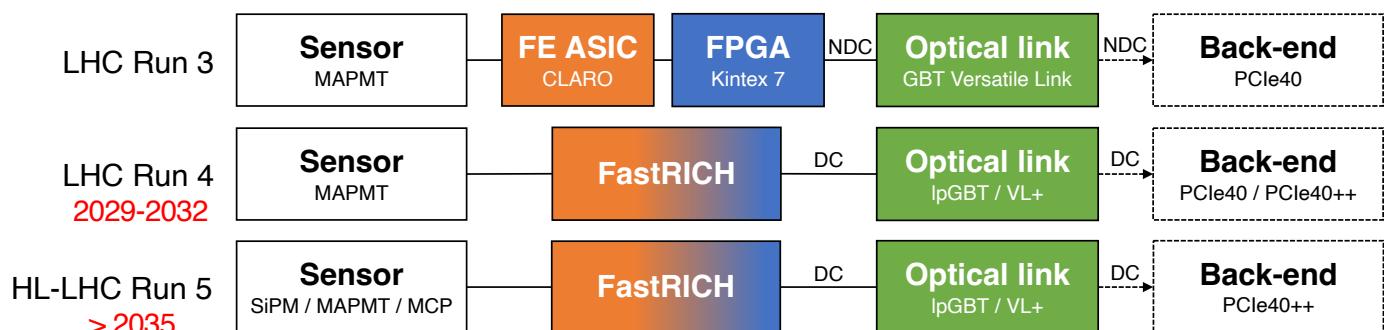
- FPGA firmware designed to use only 1-2% of logic resources to reduce radiation upsets.
- **ASIC solution** required for future upgrade operation.



# Readout chain for LS3 and LS4

The LHCb RICH LS3 enhancements aim to equip the detector with new front-end readout electronics including the **FastRICH ASIC** capable of timestamping photon detector hits with  $\sim 25$  ps time bins.

- ✓ Improve **PID performance during Run 4**.
- ✓ Introduce technologies for high-luminosity operation **ahead of Upgrade II**.
- ✓ Gather valuable experience with novel fast-timing and data compression techniques.



LS3 enhancements:

- Introduce FastRICH with 25 ps bins.
- Change to Data Compressed (DC) format.
- Introduce lpGBT/VL+.
- Small expansion at the back-end.

	Sensor	ASIC timewalk	FE time gate	TDC time bin
LHC Run 3	150 ps	< 4 ns	6.25 ns	None
LHC Run 4	150 ps	CFD correction	2 ns	25 ps
HL-LHC Run 5	$\sim 50$ ps	CFD correction	2 ns	25 ps

# LS3 hardware changes

Intend to modify **only** the FE electronics whilst maintaining all other services and components (cooling and power, mechanics, optics and sensors).

Remove:

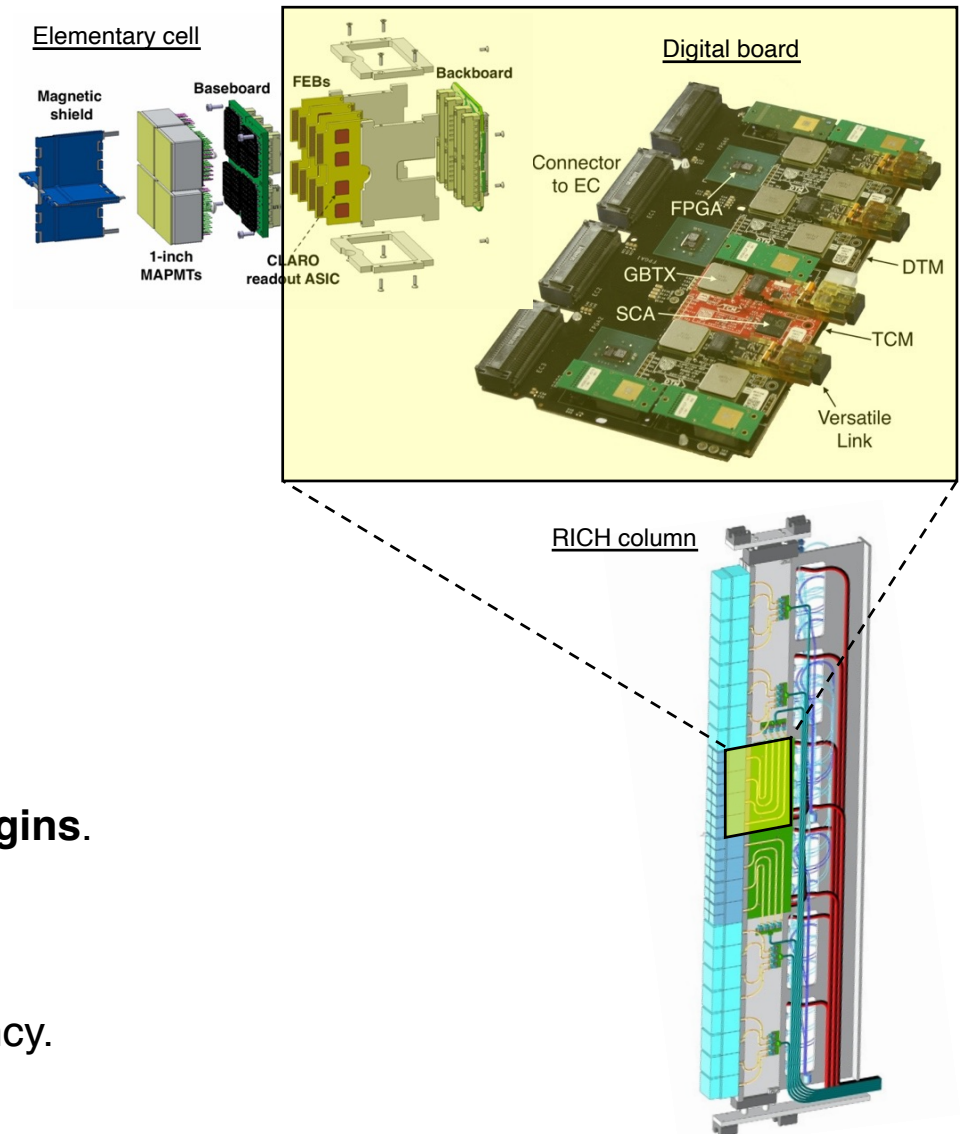
- FEBs with **CLAROs**.
- PDMDB motherboards with **FPGAs**.
- (R&D study) Perhaps **GBTX/VTRX plugins**.

Install:

- New boards with **FastRICH**.
- New electronics **levelling plate** to cold bar.
- (R&D study) Additional or all new **IpGBT/VTRX+ plugins**.
- Additional **PCIe40++** cards for back-end processing.

Adjust:

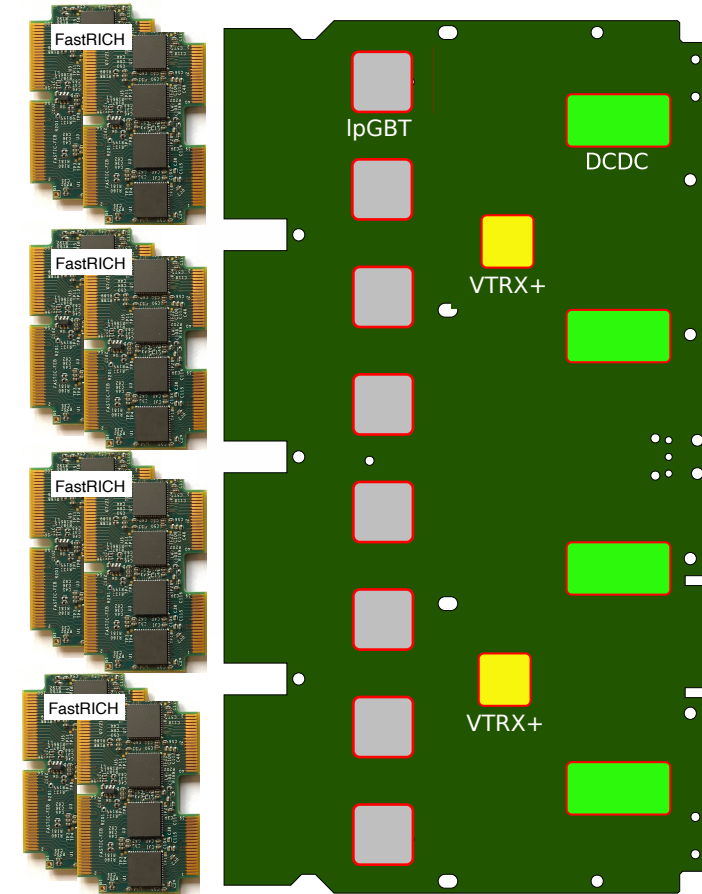
- Fibre distribution to account for non-uniform occupancy.



# Front-end electronics specifications

Specifications are tailored to ensure backwards-compatibility with the Run 3 mechanics whilst equipping the detector for Upgrade II.

- Time resolution: TDC with  $\sim 25$  ps time bins.
- Power consumption: less than 6 mW per channel (analog + digital).
- Radiation hardness: ASIC solution for  $\sim 10^{13}$   $n_{eq}/cm^2$  and  $\sim 5$  kGy.
- Number of channels: 16.
- Dynamic range: 5  $\mu$ A to few mA for coupling to MAPMT or SiPM.
- LHCb compatibility: direct compatibility with IpGBT / VTRX+ chipset.
- Bandwidth: aim for  $\sim 12$  bits per hit or less.
- Readout rate: 40 MHz (LHC).



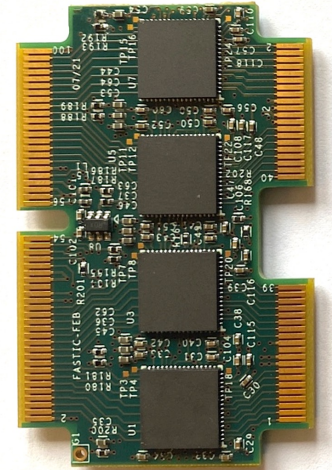
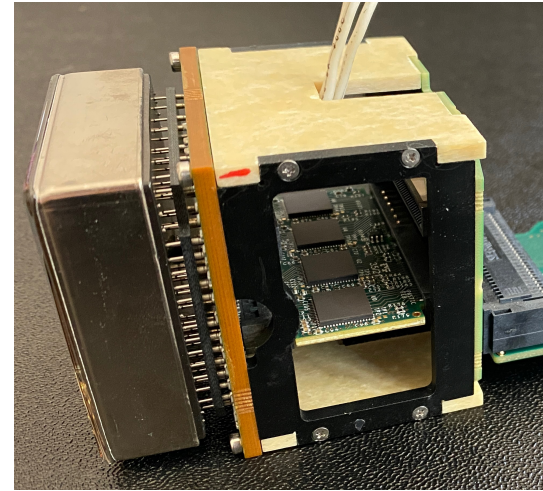
Note: Sketch for illustrative purposes. The numbers and placement of components will be subject to R&D and optimisation.

# FastIC and FastRICH ASICs

[[Poster](#) by Rafael Ballabriga et al].

The Fast Integrated Circuit (**FastIC**) is an ASIC designed in 65 nm CMOS technology by the University of Barcelona (ICCUB) and CERN-EP-ESE.

- 8-channel chip with **wide input dynamic range** (5  $\mu$ A to 25 mA) for pos/neg signal polarities.
- **'Analog' ASIC** with fast discriminator ( $\sim 30$  ps jitter).
- **Not** designed to be specifically **radiation hard**.



RICH elementary cell with FastIC ASICs.

Next-generation **FastRICH** is based on the FastIC and **specific requirements of the RICH detector**.

- 16-channel chip with **analog and digital** signal processing.
- **Hardware shutter time** (configurable) to limit the timestamp range to  $\sim 1$  to 2 ns.
- **Constant-fraction discrimination** (CFD).
- **Zero-suppressed** output over configurable number of output links to IpGBT.
- TDC with  $\sim 25$  ps time bins and 40 MHz readout rate.
- Radiation hard by design ( $\sim 10^{13}$   $n_{eq}/cm^2$  and  $\sim 5$  kGy).
- Compatibility with IpGBT and the architecture of the Run 4 and Run 5 DAQ.

FastRICH design is ongoing (CERN-ICCUB) with the analog parts far advanced.

# LS3 bandwidth considerations

The excellent FastRICH data-compression techniques of CFD, hardware shutter and zero-suppression achieve **7 bits time plus 4 bits channel ID per hit.**

## Run 3: no data-compression (NDC) at FE.

- ~ 200k channels and 40 MHz rate gives ~ **8 Tb/s.**
- DC at back-end, but sufficient margin in available PCIe40 readout boards.

## Run 4: DC techniques at FE.

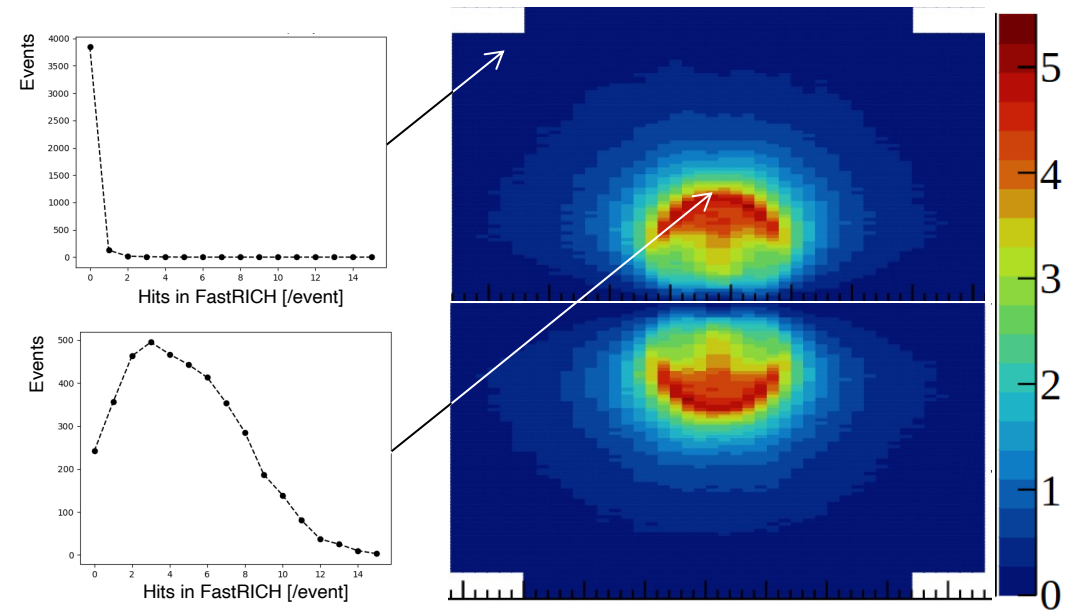
- Average occupancy of 5.5%, 11 bits per hit and 30 MHz gives ~ **3.5 Tb/s.**

More than a **factor 2 lower** than the Run 3 bandwidth and factor 3 than the Run 3 optical fibre limit (~ **12 Tb/s**).

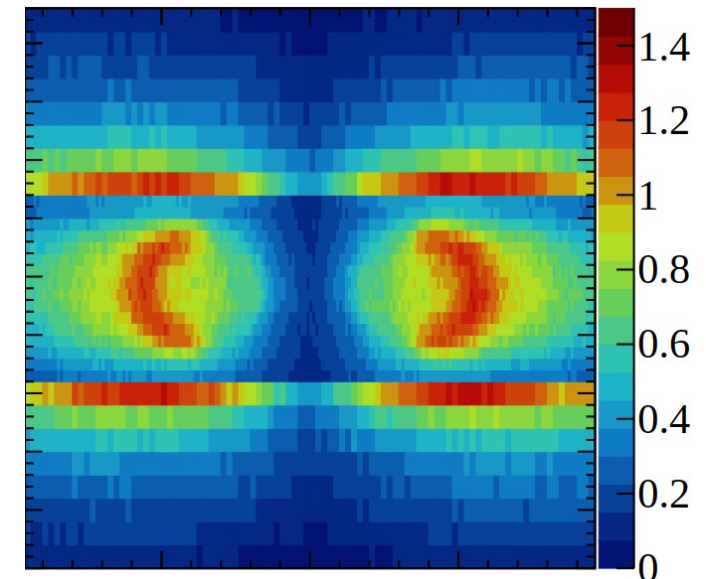
- Margin available for (a) fluctuations / “busy events”, (b) bunch count synchronisation / header data and (c) **challenging FastRICH-to-optical link mapping for non-uniform occupancies.**

Detailed simulation studies are ongoing.

Run 4 average number of hits per FastRICH per event, **RICH 1**



Run 4 average number of hits per FastRICH per event, **RICH 2**



# Power consumption of the readout electronics

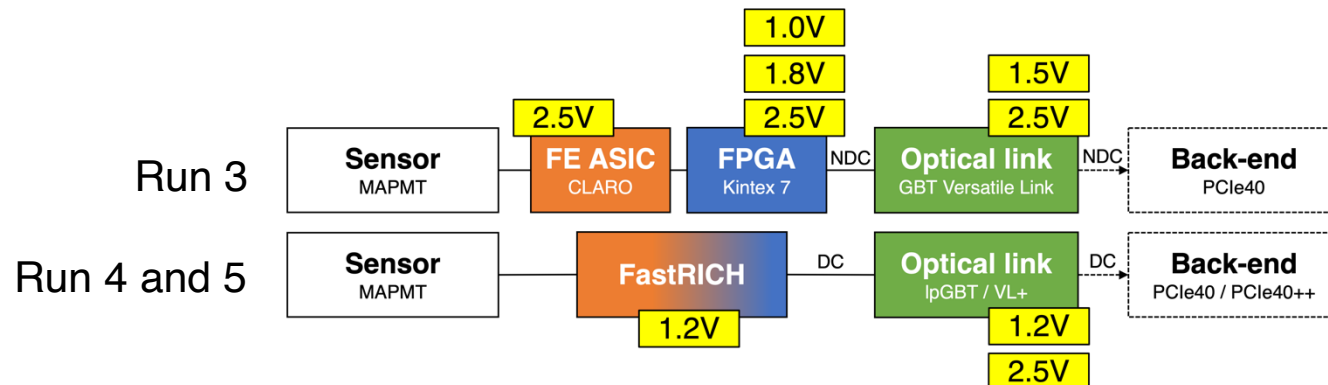
Removal of the Run 3 **FPGAs saves ~ 8.6 mW/ch** (and CLARO ~ 1 mW/ch).

- Additionally, 50% margin was built into the Run 3 electronics power consumption for irradiation damage during Run 3 and Run 4 combined. The LS3 enhancements set the **TID for Run 4 back to zero**.

With ~ 6 mW/ch target consumption for the FastRICH, the **overall column power consumption goes down**.

- The Run 3 FPGAs are closely coupled to the cold bar, and **R&D** is ongoing to evaluate adjustments to the boards layout to **improve the thermal coupling** between the cold bar and the FastRICH ASICs.

New electronic readout simplifies the number of required power levels:





# Optical plugins (IpGBT and VTRX+)\*

The FastRICH will be closely-compatible with the IpGBT.

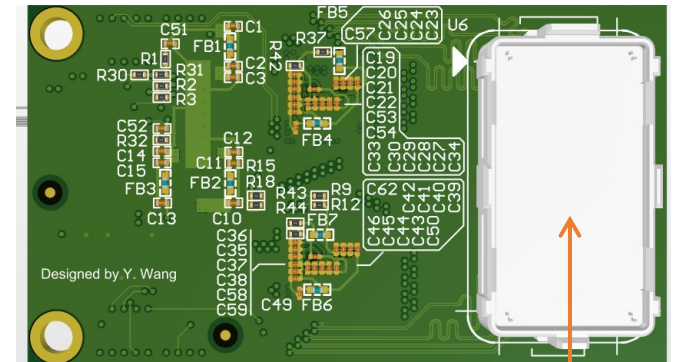
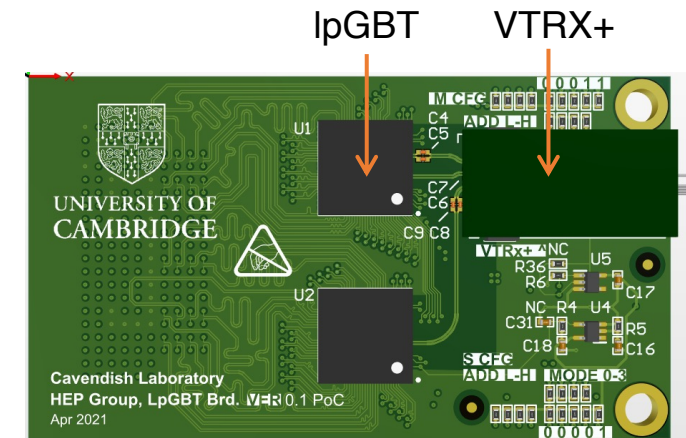
- Digital outputs of the FastRICH **couple** directly to the IpGBT eLinks.
- **Configurable** number of FastRICH output links in FastRICH to account for different occupancy regions.
- **I2C** for configuration.
- 160 MHz **clock lines** from the IpGBT distributed across the FE.

Plugin driven by:

- (a) Flexibility on motherboard for bandwidth optimisation.
- (b) Modularity.
- (c) PCB requirements for the IpGBT (with small BGA pitch).

Alternative for highest-occupancy region:

Optical link components directly integrated onto the motherboard in order to achieve the required density.



Connector to motherboard

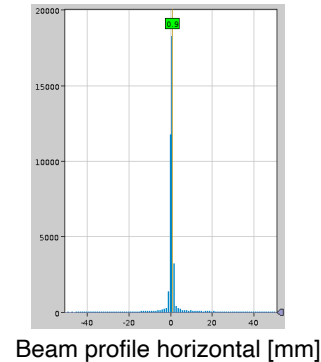
\* Next-generation CERN 10 Gbps optical link chipset

# SPS test beam studies of a prototype opto-electronics chain

Studies of a prototype opto-electronic chain with  $\mathcal{O}(100 \text{ ps})$  timing for LS3 / LS4.

➤ 'Proof-of-principle' demonstration to detect 4D Cherenkov rings / arcs.

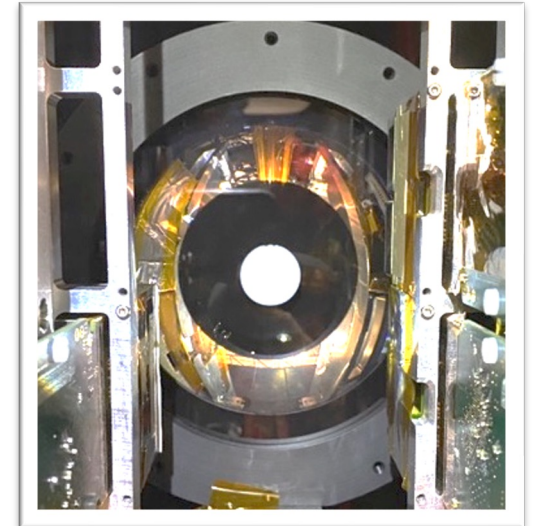
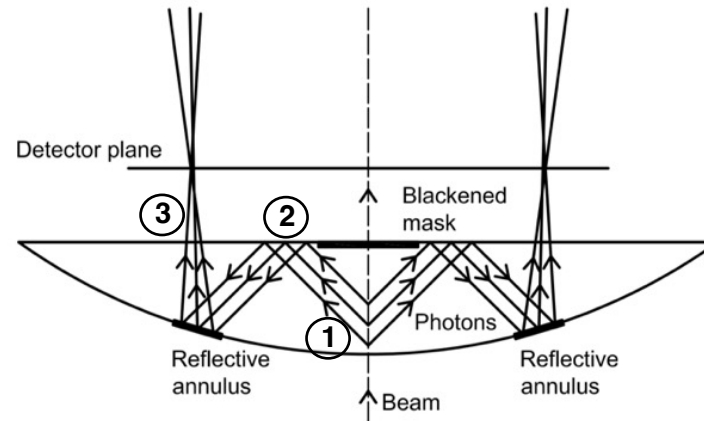
- CERN SPS test beam facility.
- 180 GeV/c pions and protons.
- Pencil beam with  $\sigma < 5 \text{ mm}$ .
- Few hundred kHz average particle rate.
- RICH MCP-PMT for track time reference.
- TimePix4 telescope for tracking information.
- Oct 2021, July 2022 and (upcoming) Oct 2022.



Parallel setup in this beam for aerogel studies [[Poster](#) by A. Lozar et al].

Coated borosilicate **lens** in the beam to:

1. generate the Cherenkov photons,
2. reflect them and
3. focus the Cherenkov ring onto the detector plane.



[DOI:10.1088/1748-0221/12/01/P01012](https://doi.org/10.1088/1748-0221/12/01/P01012)

# The prototype fast-timing readout chain

Digital board for the testbeam, containing a Kintex7  
**FPGA with 34-channel TDC** with 150 ps time bins

➤ [[Poster](#) by Lucian Cojocariu et al].

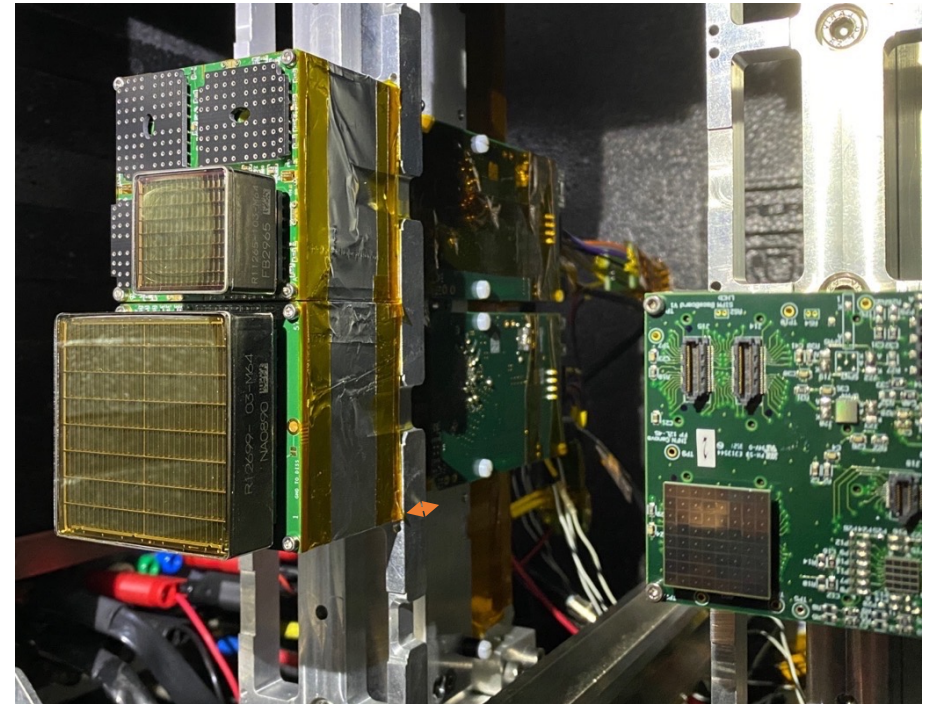
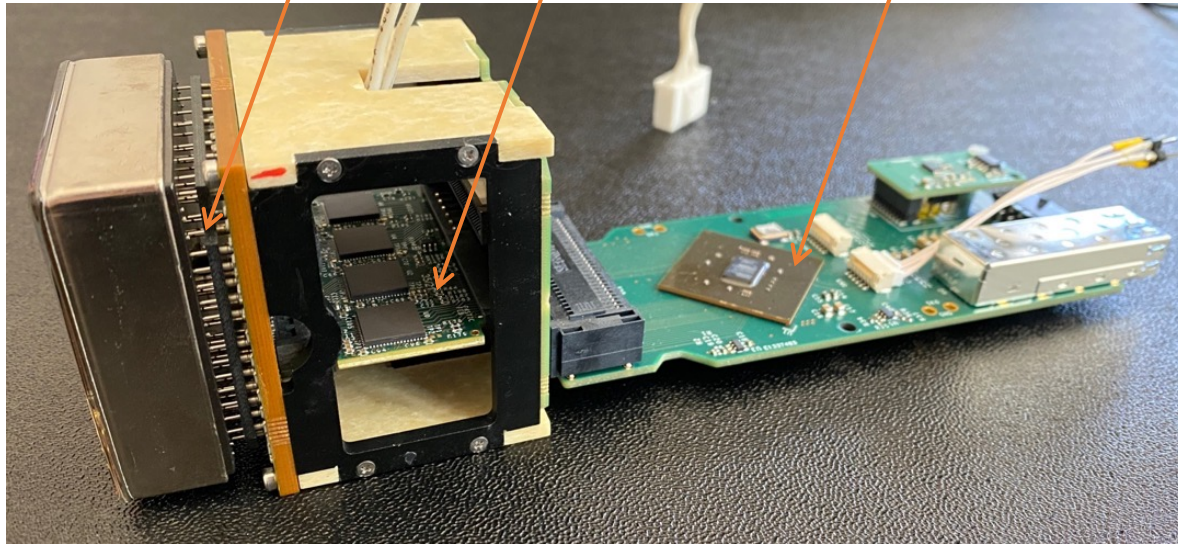
FEBs with **FastIC** ASICs.

➤ Output of fast-timing channel:  
ToA + **non-linear ToT**.

**MAPMT / SiPM** baseboard.

➤ [[Talk](#) by Roberta Cardinale]

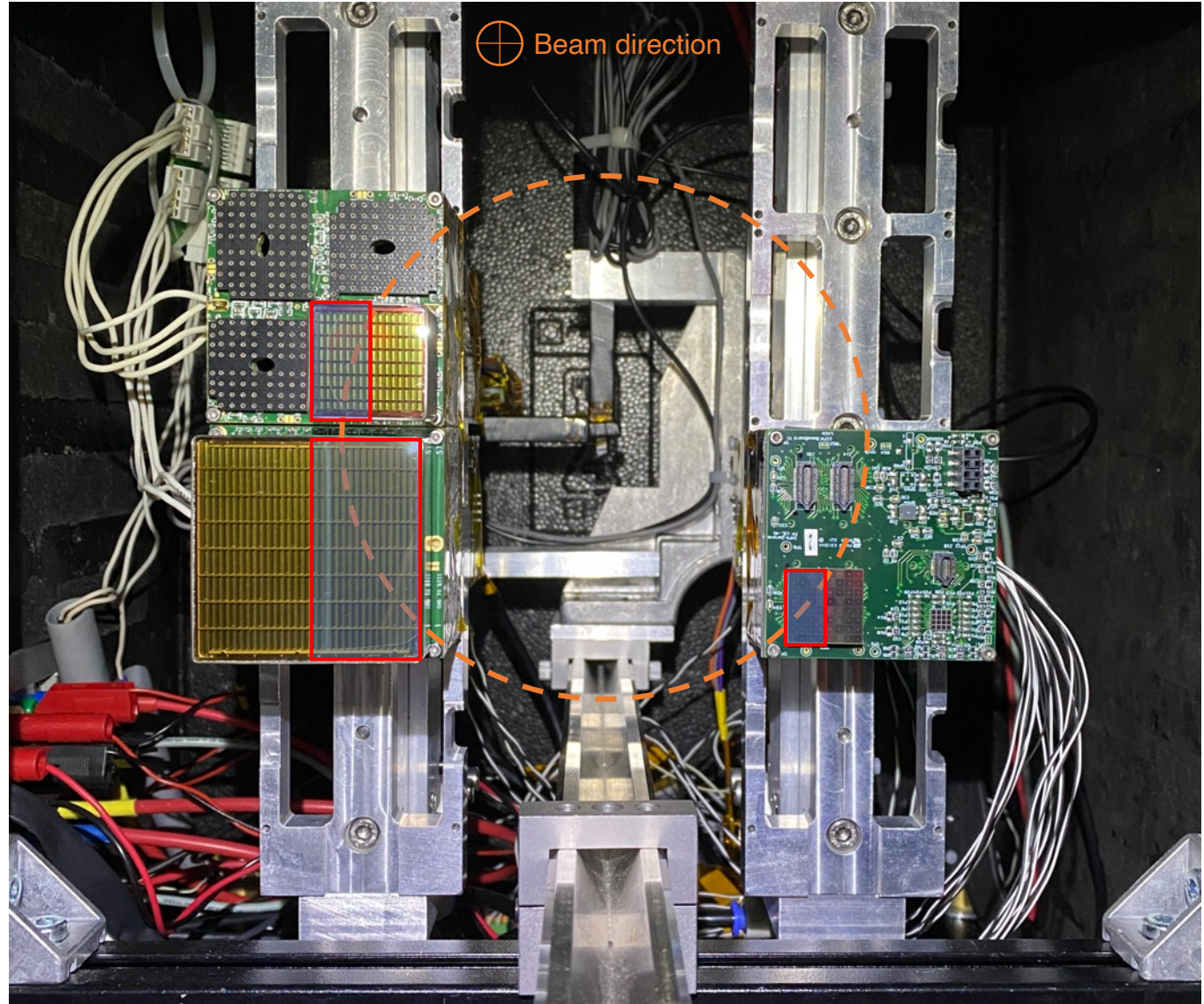
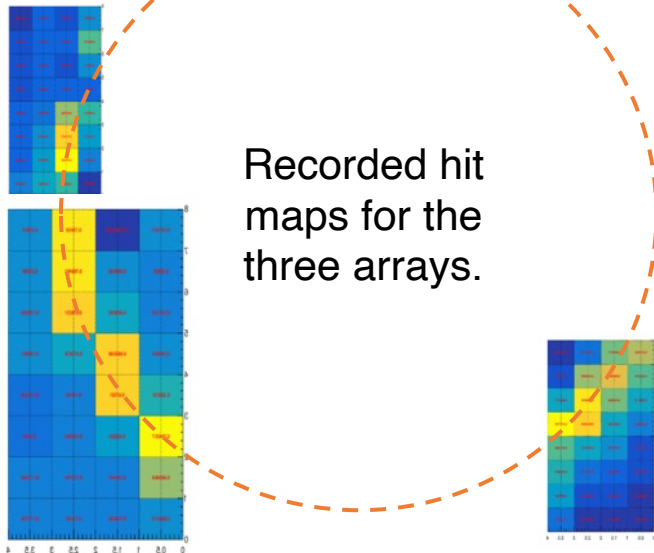
FastICs **coupled to MAPMTs**  
(1 and 2-inch devices, Run 4)  
and an **SiPM array** (Run 5 candidate).



# Readout using 3 FEBs with 16 FastICs



FastIC FEBs for partial readout of sensor area.



# Ongoing analyses and first results

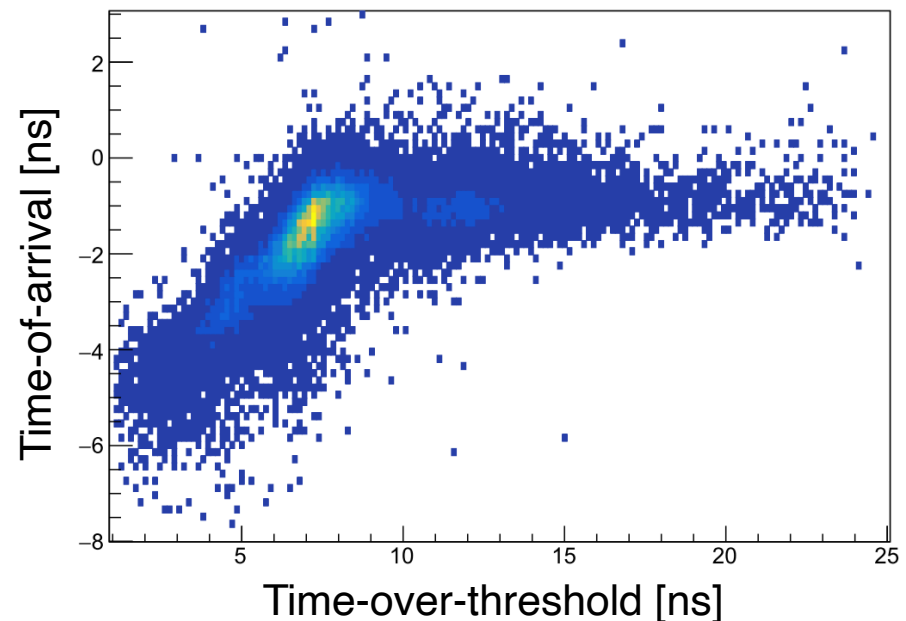
Extraction of the time resolution requires detailed analysis of the data, including:

- Correction for **time walk** effect.
- **Calibration** of the TDC-in-FPGA.
- Understanding of FastIC **working points** and photon **occupancy**.
- Study of **systematic errors** including track time reference and chromatic dispersion.

Aim to achieve the single-photon resolution of  $\sim 150$  ps limited by the MAPMT transit time spread.

Analyses are ongoing with prospect of more data-taking in October 2022 followed by testbeam paper.

- Plot shows example of measured time walk for a typical pixel.



# Conclusion

**Fast-timing information** is foreseen to be added to the LHCb RICH system **during LS3** (3 year long).

- Improve the **PID during Run 4**.
- Gain important experience (hardware / software) with **technologies and techniques for Upgrade II**.

**The proposed new readout chain will:**

- Introduce the **FastRICH**, which includes specific LHCb RICH upgrade requirements.
- Affect only a small part of the Run 3 detector and require limited resources.

**Key features of the enhancement include:**

- **25 ps time bins** and a wide dynamic range for coupling to MAPMTs or SiPMs.
- **Data compression techniques**: CFD, 2 ns FE gate and zero-suppressed readout.
- **Direct compatibility optical links**: IpGBT / VL+.

**SPS test beam campaign to study prototype readout chains.**

- Successful data-taking in July 2022 with detailed timing analyses ongoing.