The arrival of the Cherenkov photons to the photon detectors of the LHCb RICH system from a particular track can be predicted to within 10 picoseconds. This property can be used to improve pattern recognition and particle identification methods when high detector occupancy results from multiple primary vertices, which are slightly displaced in time. Time-stamping the Cherenkov photons with an accuracy of 100 ps or better improves the signal to noise ratio and allows operation with good particle identification for luminosity in excess of 10^34 cm^-2 s^-1.

The FastRIC is a readout chip that is being designed in the framework of the upgrade of the LHCb RICH detector to be installed during the LHC Long Shutdown 3 (2023-2028) to read out multi-anode PMTs, while allowing compatibility with a detector R&D programme for operation in Run 5 for which SiPMs are candidates. The Application Specific Integrated Circuit (ASIC) is a derivative of the FastIC ASIC designed in a collaboration between the Microelectronics section at CERN and University of Barcelona.

The FastIC chip provides a radiation hard, low power and compact system for the LHCb RICH detector for interfacing with the detector on one side and on the other with lpGBT/optical links. Emphasis is placed at reducing the amount of data generated by (1) using a Zero Suppressed Readout, (2) implementing a programmable "2ns shutter signal" to filter events from background or reflections and (3) implementing a Constant Fraction Discriminator (CFD) in the analog front-end in order to avoid recording the signal Time over Threshold (ToA) to correct for time walk. Also a configurable number of output links (1/2/4) can be programmed to adapt the ASIC to the occupancy of the different regions of the experiment.

The purpose of this contribution is to present a detailed description of the FastIC chip architecture and characterization and the FastRICH architecture and main design choices.

**ASIC SPECIFICATIONS**

- **Technology**: 65 nm CMOS
- **Size**: 56.7 mm²
- **Channel type / Connection**: Linear input / Single ended
- **Channel output**: Negative (PMT, MCP-PMT, SiPM sensor input)
- **Input Signal Amplitude**: 80 mV rms / 50 V pk-pk
- **Input Signal attenuation**: Configurable per channel (1, 1/2, 1/4, 1/8)
- **Input current range / number of pads**: 40 mV rms / 80 pads
- **Package / connector**: QFN56 / BGA (23 pins)
- **Trigger input / channel**: Target => (Single channel)
- **Power consumption (digital)**: Currently under study
- **Power consumption (analog)**: 40 mV rms for 50 mV input pulse, 140 mV rms for pulses above 100 mV
- **Energy resolution** (9% FWHM for the 160 keV peak): 1022 ps
- **Energy resolution** (9% FWHM for the 511 keV peak): 3114 ps
- **Energy resolution** (9% FWHM for the 122 keV peak): 896 ps
- **Detectors**: PMT, MCP, SiPM
- **Output driver**: 8 channels of 8 channels

**FastIC Block Diagram in Single Ended**

- **Input Stage**: From remaining channels
- **Resistive Stage**: Input Stage
- **Common DAC**: Resistive Stage
- **Single Ended Input**: Common DAC
- **Input Stage**: Resistive Stage
- **Common DAC**: Resistive Stage
- **Single Ended Input**: Common DAC
- **Output Stage**: Common DAC

**FastIC Time Waveforms**

- **FastIC provides a measurement of time-to-amplitude per channel in two consecutive pulses**
- **Time is encoded in the rising edge of the first pulse**
- **Energy is encoded in the width of the second pulse (Time above Threshold ToA)**
- The readout is based on an iType/1 architecture

**FastIC Evaluation System**

- **Full system**
- **FastIC generic board**
- **Custom sensor board**
- **FPGA board**

**Proposed system**

- **1211 GEN**
- **TPC**
- **SiPM**
- **Anode readout**
- **Energy resolution**
- **Data rate**
- **Pinout**

**FASTRICH BLOCK DIAGRAM**

- **Input Stage**: From remaining channels
- **Resistive Stage**: Input Stage
- **Common DAC**: Resistive Stage
- **Single Ended Input**: Common DAC
- **Input Stage**: Resistive Stage
- **Common DAC**: Resistive Stage
- **Single Ended Input**: Common DAC
- **Output Stage**: Common DAC

**FastIC Measurements**

- **Linearity error below 3% over the whole dynamic range**
- **Single Photon Time Resolution (SPTR)**

**FastIC Measurements**

- **Energy resolution 9% FWHM for the 511keV peak**
- **Energy resolution 9% FWHM for the 122keV peak**
- **Energy resolution 9% FWHM for the 160keV peak**

**FastRICH Chip for the Upgrade of the LHCb RICH Detector**