From the FastIC ASIC to FastRICH, A Readout Chip for the Upgrade of the LHCb RICH Detector

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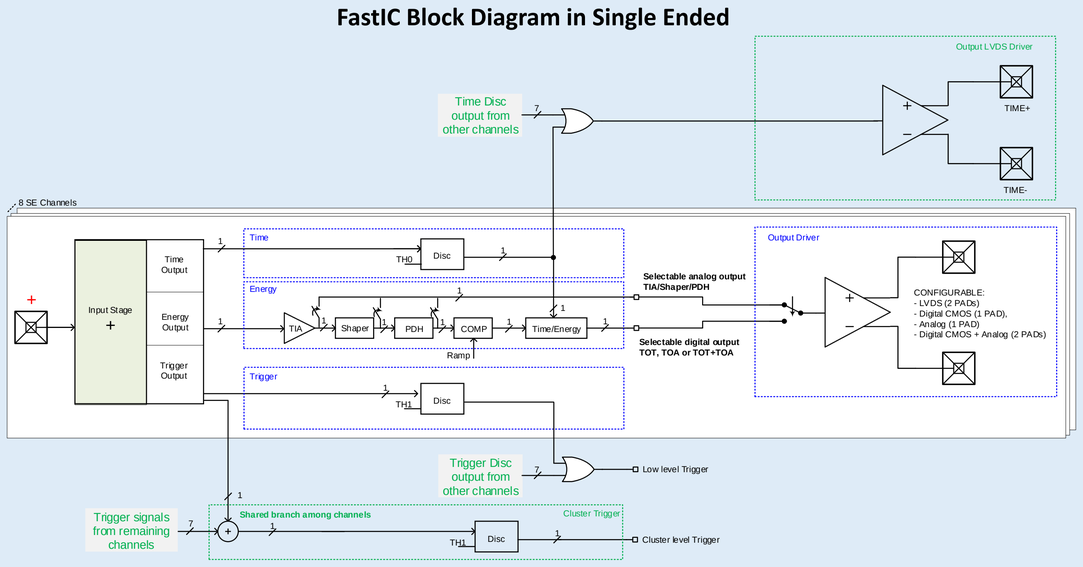
The arrival of the Cherenkov photons to the photon detectors of the LHCb RICH system from a particular track can be predicted to within 10 picoseconds. This property can be used to improve pattern recognition and particle identification performance when high detector occupancy results from multiple primary vertices, which are slightly displaced in time. Time-stamping the Cherenkov photons with an accuracy of 100 ps or better improves the signal to noise ratio and allows operation with good particle identification for luminosity in excess of 10^{34} $cm^{-2}s^{-1}$.

The FastRICH is a readout chip that is being designed in the framework of the upgrade of the LHCb RICH detector to be installed during the LHC Long Shutdown 3 (2026-2028) to read out multi-anode PMTs, while allowing compatibility with a detector R&D programme for operation in Run 5 for which SiPMs are candidates. The Application Specific Integrated Circuit (ASIC) is a derivative of the FastIC ASIC designed in a collaboration between the Microelectronics section at CERN and University of Barcelona.

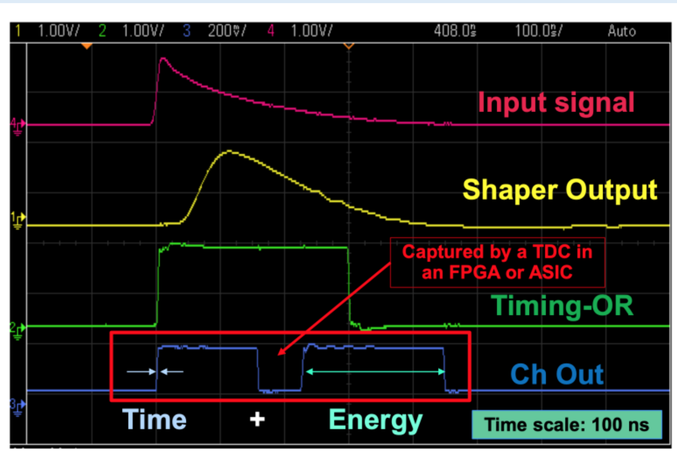
The FastRICH chip provides a **radiation hard** (TID and SEE), **low power** and **compact** system for the LHCb RICH detector for interfacing with the detector on one side and on the other with lpGBT/optical links. Emphasis is placed at reducing the amount of data generated by (1) using a **Zero Suppressed Readout**, (2) implementing a **programmable ~2ns shutter signal** to filter events from background or reflections and (3) implementing a **Constant Fraction Discriminator (CFD)** in the analog front-end in order to avoid recording the signal Time over Threshold (ToT) to correct for time walk. Also a **configurable number of output links** (1/2/4) can be programmed to adapt the ASIC to the occupancy of the different regions of the experiment.

The purpose of this contribution is to present a detailed description of the FastIC chip architecture and characterization and the FastRICH architecture and main design choices.

FastIC Block Diagram in Single Ended



FastIC Time Waveforms

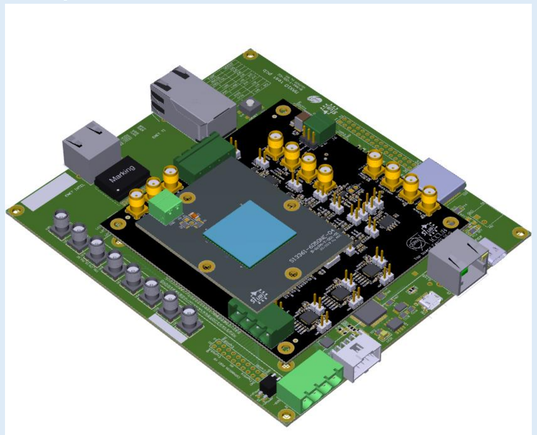


- FastIC provides a measurement of time and energy per channel in two consecutive pulses
- Time is encoded in the rising edge of the first pulse
- Energy is encoded on the width of the second pulse (Time over Threshold ToT). The readout is based on HRFlexToT architecture*

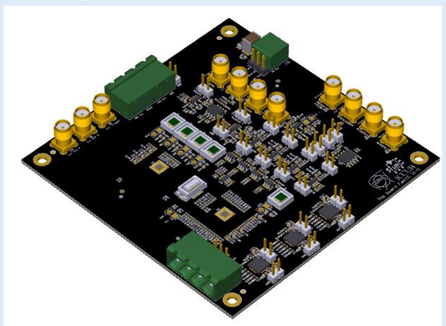
*D. Sanchez, S. Gomez, et. al. "HRFlexToT: A High Dynamic Range ASIC for Time-of-Flight Positron Emission Tomography" 2021, IEEE TRPMS, https://doi.org/10.1109/TRPMS.2021.3066426

FastIC Evaluation System

Full system

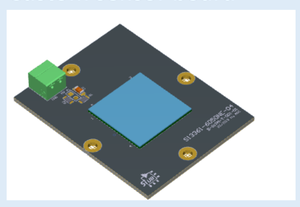


FastIC generic board



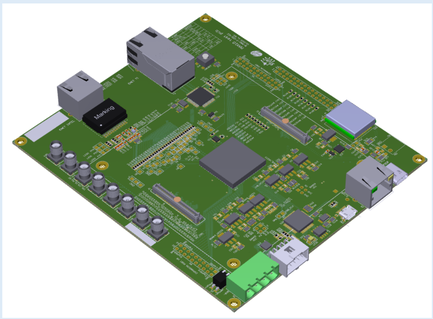
- 2 FastICs on QFN64 (16 channels)
- Reference SiPM sensors included
- The board can be used stand alone

Custom sensor board



- Interface board to other sensors (PMT, MCP-PMT, SiPM sensor array)
- HV must be provided to the external connector

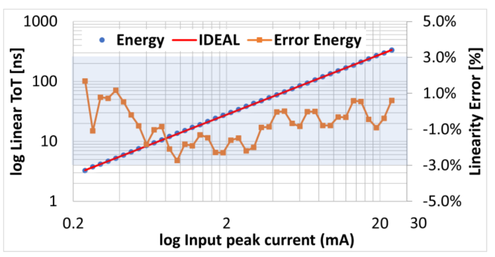
FPGA board



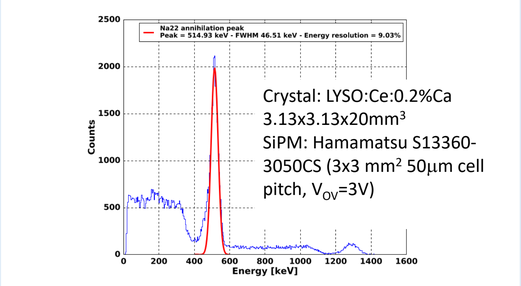
- FPGA board for slow control, acquisition and additional biasing.
- Multichannel TDC is implemented in the FPGA (45ps time bin)

FastIC Measurements

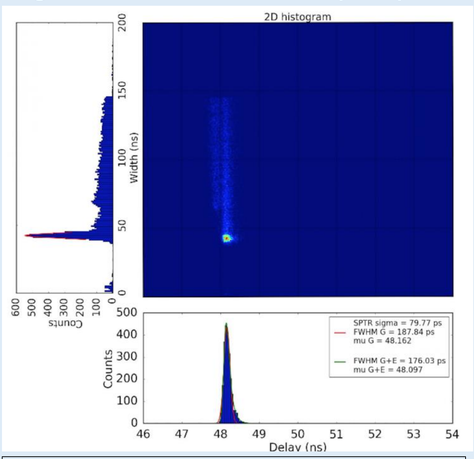
Linearity error below 3% over the whole dynamic range



Energy resolution 9% FWHM for the 22Na 511keV peak

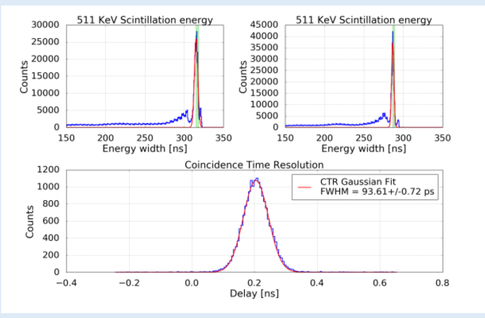


Single Photon Time Resolution (SPTR)



Hamamatsu S13360-3050CS (3x3 mm² 50µm cell pitch, V_{OV}=11V)
SPTR= 176 ± 5 ps FWHM

511keV Photon Coincidence Time Resolution (CTR)



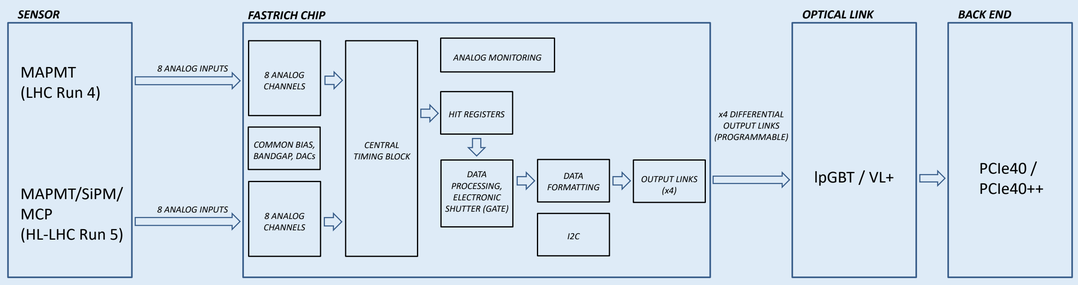
Crystal: LSO:Ce:0.2%Ca 2x2x3 mm², LY=39.2 ph/keV, τ_d=~32ns

SiPM: Hamamatsu S13360-3050CS (3x3 mm² 50µm cell pitch, V_{OV}=8V)

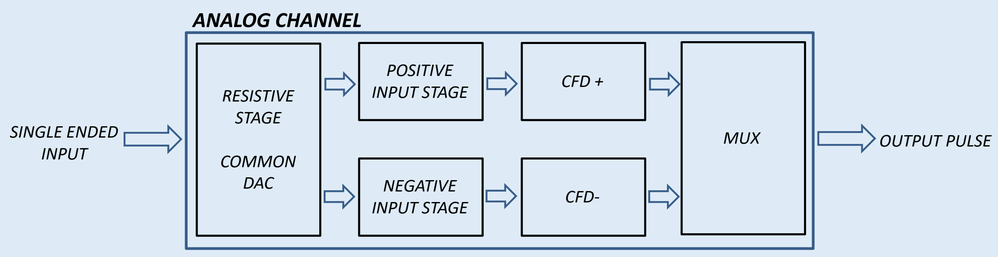
CTR= 93 ± 3 ps FWHM

FASTRICH BLOCK DIAGRAM

Proposed system



Detail of the FastRICH analog channel



ASIC SPECIFICATIONS

Parameter	FastRICH
Technology	65 nm CMOS
Number of channels	16
Channel type / Connection	Linear layout / Single ended
Polarity	Negative (PMT, MCP, SiPM Cathode readout) and Positive (SiPM Anode readout) Front end optimized for small input capacitance detectors (PMT, MCP, ≤1x1mm² SiPMs)
Input Signal attenuation	Configurable per channel (1, 1/2, 1/4, 1/8)
Die dimensions/Number of pads	4x4 mm²/ 80 pads
Package/connection to sensor	QFN64 / BGA (To be studied)
Power consumption Analog	Target ~4mW/channel
Power consumption Digital	Currently under study
Electronics Time Jitter	~40 ps r.m.s. for 50 µA input pulse, <30 ps r.m.s. for pulses above 100 µA
Residual Time Walk	200ps pk-to-pk (after CFD, from 50 µA to 5 mA pulses) (Input PMT pulses are modelled with a Gaussian shape with σ=0.5 ns)
Energy Resolution	Non linear (Energy measurement not required due to single photon regime in experiment) (Possibility of an additional threshold to discriminate multiple photons on amplitude would be an asset for Upgrade 2. increasing the output bandwidth by 1bit/hit) (Feature currently under study)
Dynamic Range	5 µA to 5 mA (The timing performance is achieved for pulses >50 uA) Noise <2 µA r.m.s. (Typical PMT signal: Gaussian shape with σ=0.5 ns and 300 µA amplitude)
Front-End Hit Rate	Ability to detect signals on two consecutive beam crossings.
Testing and Calibration	Yes (With internal test charge generation by means of a test capacitance controlled by a digital signal)
Slow Control Interface	I2C with multiple chips on the same I2C bus
Output	Digital differential/lpGBT compatible
Nominal VCO oscillation frequency/Number of VCO stages	1.28GHz/14
Total Bits/event [bits]	7 ToA bits (2 fToA, 5 ufToA) 4 Channel Identification 1 Threshold High Hit (not required for Upgrade 1b) (Feature currently under study) (Data output protocol under study)
Output links data rate	160, 320, 640, 1280 Mbps
Number of Output links	Programmable at chip level to 1, 2 or 4.
Radiation hardness	Yes (TID (>100Mrad) and Triplication)