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From the FastIC ASIC to FastRICH, A Readout Chip for the Upgrade of the LHCb RICH Detector

The arrival of the Cherenkov photons to the photon detectors of the LHCb RICH system from a particular track can be predicted to within 10 picoseconds. This property can be used to improve pattern recognition and particle identification performance when high detector occupancy results from multiple primary vertices, which are slightly displaced in time. Time-stamping the Cherenkov photons with an accuracy of 100 ps or better improves the signal to noise ratio and allows operation with good particle identification for luminosity in excess of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.

The FastRICH is a readout chip that is being designed in the framework of the upgrade of the LHCb RICH detector to be installed during the LHC Long Shutdown 3 (2026-2028) to read out multi-anode PMTs, while allowing compatibility with a detector R&D programme for operation in Run 5 for which SiPMs are candidates. The Application Specific Integrated Circuit (ASIC) is a derivative of the FastIC ASIC designed in a collaboration between the Microelectronics section at CERN and University of Barcelona.

The FastIC is an 8 channel generic detector readout ASIC developed in 65nm CMOS technology that provides an accurate time stamping of the detected particles and a linear energy measurement with a dynamic range from a few microamperes to $\sim 20 \text{ mA}$. The ASIC contains an analog front-end and discrimination circuitry. The power consumption of the full channel is 12 mW with default settings. The ASIC includes an input stage that can be configured to process the signal from positive or negative polarity detectors with intrinsic amplification, like MCPs, PMTs or SiPMs. Measurements were done using FastIC to read out an R5900 Hamamatsu PMT biased at 800V. The measurement, after time walk correction, showed a time jitter of $\sim 340 \text{ ps}$ FWHM, which corresponds to the intrinsic PMT time uncertainty when detecting tens of photons. The result showed that the ASIC itself introduced a negligible contribution to the measured time uncertainty. The SPTR was also measured (including laser, sensor and electronics contribution) using a blue-light laser source and a $3 \times 3 \text{ mm}^2$ SiPM HPK S13360-3050CS to be $176 \pm 3 \text{ ps}$ FWHM at 10.6 V of over-voltage. When the FastIC is connected to the new technology HD-NUV Low Field SiPM from FBK ($3.2 \times 3.12 \text{ mm}^2$, $40 \mu\text{m}$ cell), the SPTR decreased to $151 \pm 3 \text{ ps}$. An extensive campaign of measurements is ongoing to evaluate the chip in the LHCb RICH environment.

The FastRICH chip under development is based on the analog circuitry of FastIC. The 16-channel FastRICH chip is designed to provide a low power, compact and radiation hard readout including the analog front-end, discrimination, Time-To-Digital Conversion and output data zero-suppressed readout compatible with the lpGBT/VTRX+. The chip is designed to deal with 40 MHz hit rates in the single photon regime. In order to optimize the output data bandwidth, a Constant Fraction Discriminator (CFD) is being studied in order to eliminate the need to measure the trailing edge of the signal for time walk correction. The first simulation results including the front-end and CFD circuit show an electronics jitter $< 40 \text{ ps}$ rms for detector signals above $50 \mu\text{A}$, and a residual time walk below 200 ps peak to peak within the input range from $50 \mu\text{A}$ to 2 mA. Also, a hardware shutter programmable in terms of phase with respect to the experiment clock and duration is implemented to reduce the output data bandwidth.

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