A multi-channel TDC-in-FPGA with 150 ps bins for time-resolved readout of Cherenkov photons

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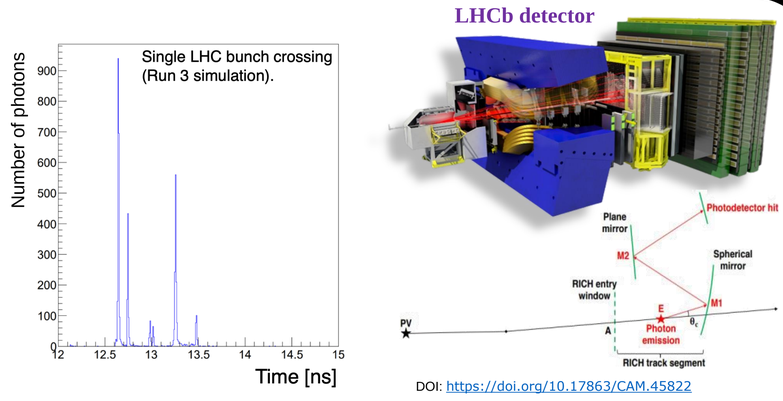
Time-resolved readout in RICH detectors

- The addition of a Cherenkov photon timestamp will provide complementary information to the spatial coordinates to help resolve individual interactions in the high-multiplicity environment of a future LHCb detector [1].
- The excellent intrinsic time resolution of the two LHCb RICH subdetectors allows the time of arrival of all Cherenkov photons from a single particle to be predicted to within ~10 ps.
- We have developed a low-cost, multi-channel TDC in an FPGA having ~150 ps bin width and capable of a photon time-of-arrival (ToA) and time-over-threshold (ToT) capture rate in excess of 50 MHz.
- The TDC was used for measurements in beam tests and in the laboratory to demonstrate the application of time-resolved readout in a compact RICH apparatus.



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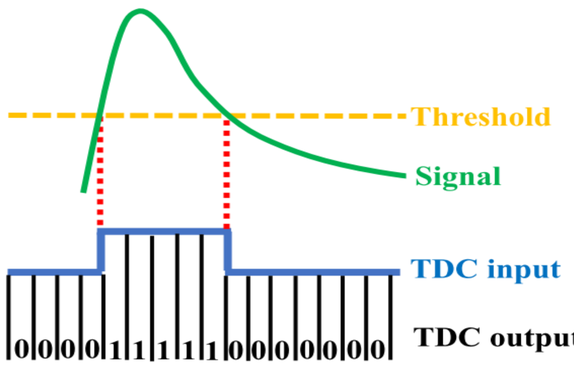
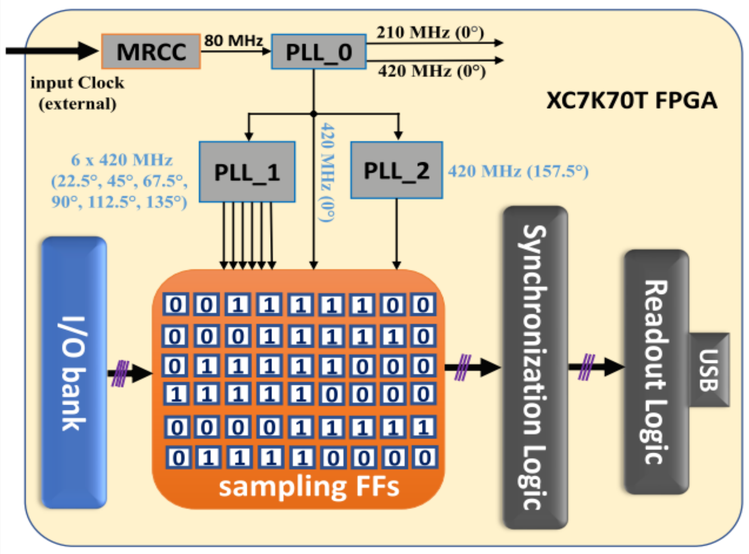
TDC design

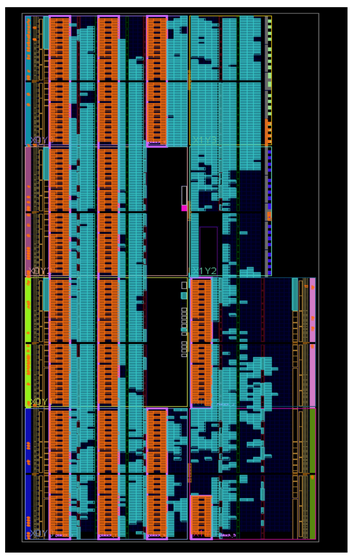
- A multi-phase clock sampling architecture was implemented in a Xilinx Kintex-7 FPGA with the following features:
  - robustness against process, voltage supply and temperature variations (PVT) unlike other FPGA-based TDC architectures;
  - resource-efficient design to accommodate ToA and ToT measurements capability for the same photon signal;
  - replicable and scalable architecture to maximise the number of channels;
  - 34 channels employing 16 phase-shifted copies of a 420 MHz clock (22.5° phase shift), ~150 ps nominal bin size width, and 2 additional channels of which one was used for trigger timestamp;
  - sampling flip-flop logic adopted from [2].



Signal sampling sequence using TDC-in-FPGA core



The simplified architecture of the multi-channel TDC-in-FPGA

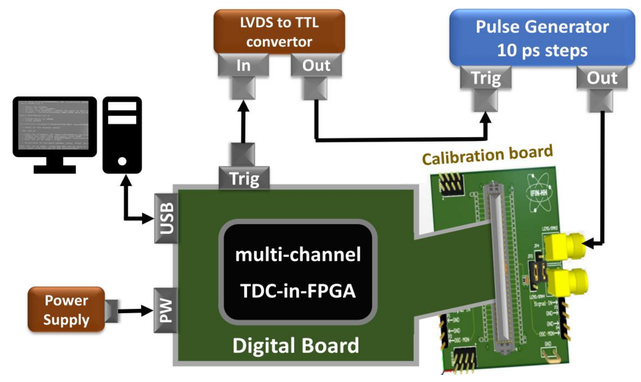


The core logic placement within FPGA, including DAQ

- The FPGA also contains a DAQ system to buffer and output zero-suppressed data via a USB interface in response to an external trigger.
- Design highlights:
  - the input path is divided into branches constrained with the aim of equalising the delay paths from the FPGA I/O pin to all 16 sampling FFs;
  - most of the TDC logic was manually placed to ensure that the sampled data pattern is clocked and synchronised correctly in one clock domain before readout;
  - a dedicated clocking network architecture was developed to accommodate the clock number, frequency and phase requirements.

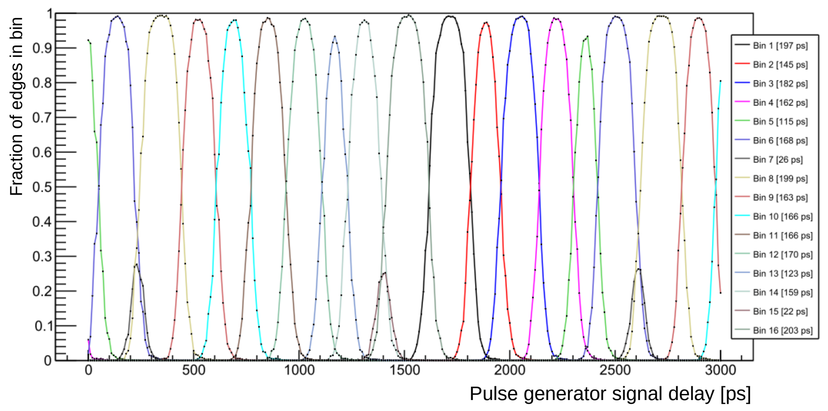
Calibration and measurements

- The TDC resolution is limited by bin-width variations due to propagation delays in the FPGA. These are measured through a calibration process and used to correct the TDC data.
- A pulse generator was used to inject a reference pulse with <25 ps jitter in order to calibrate the TDC core.



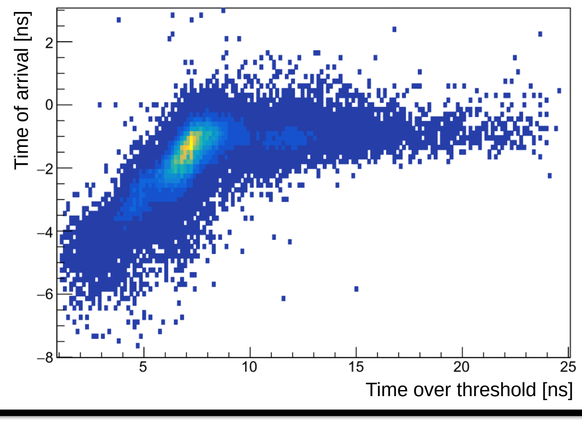
Setup for determining the calibration parameters

- The plot shows, for each TDC bin, the fraction of times when an external reference signal is registered in that bin as the reference pulse is scanned in 10 ps steps across the TDC range.
- The bin widths deduced from this plot, which vary by up to about 180 ps in this implementation, can be taken into account when measuring the photon time of arrival.



Fraction of signals arriving in each bin for different signal delays

- The plot below illustrates the simultaneous ToA and ToT measurement capability of the TDC.
- The detailed timing characteristics of Cherenkov photon signals can be clearly discerned in this uncalibrated data.
- These measurements are typical of the data that we have recorded at the CERN test beam facilities and will allow us to evaluate the timing characteristics of different sensors and read-out electronics that are candidates for the LHCb RICH upgrade.



ToA against ToT measured for Cherenkov photons

Conclusions

- A low-cost 34-channel TDC core was successfully implemented in an FPGA and was used in two test beam campaigns (October 2021 and July 2022) for timing measurements of Cherenkov photons at the SPS test beam facility at CERN.
- The TDC core contained 16 phase-shifted copies of a 420 MHz clock (22.5° phase shift) and ~150 ps nominal bin width.
- The architecture minimises the use of logic resources in order to increase the number of channels with high acquisition rates and low dead-time.
- Calibration of the TDC was performed in 10 ps steps in order to apply an offline correction to recorded Cherenkov photon data.
- For a typical channel, the bin widths were found to vary with a spread of about 180 ps.

Bibliography

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