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A 32-channel TDC Implemented on an FPGA for Photodetector Timing Studies

Simulation studies have shown that future RICH detectors in high occupancy environments will benefit from time-resolved single-photon readout with sub-nanosecond resolution. We present an FPGA TDC (Time to Digital Converter) implementation developed as part of the LHCb RICH upgrade R&D program. The design requirements for a such TDC core are low logic resource utilization, multi-channel readout, high acquisition rate, closely integrated with the DAQ, and less than 300 ps bin size. The TDC core presented here is based on the previous work of Y. Wang et al., which introduced a multi-channel, multi-phase clock sampling architecture implemented in an FPGA. In our design we have simplified the original TDC logic, in order to implement up to 32-channels, minimize the sampling dead-time and allow measurement of both time of arrival (TOA) and time over threshold (TOT) for the same sample using an FPGA having fewer logic resources than the one used in the previous work. The TDC was implemented in a Xilinx Kintex-7 FPGA using 12 phase-shifted copies of a 320 MHz clock for a 261 ps nominal bin size. Even though its architecture is simple, a challenging step was to manually route and place each TDC logic block. This was required to have the same delays on each path that the input signals take to the sampling blocks of the TDC. The TDC capabilities were simulated first and then validated during lab tests by using a precise pulser with 10 ps step. First measurements with particle beams were performed with this 32-channel TDC at the CERN Super Proton Synchrotron (SPS) in October 2021, where it was used to time-tag Cherenkov photons detected with MaPMTs and SiPMs. An improved version of this TDC with 210 ps nominal bin size is currently under development for the planned July 2022 beam tests.

Primary author: PLACINTA, Vlad-Mihai (Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering (IFIN-HH RO))

Co-authors: COJOCARIU, Lucian Nicolae (Horia Hulubei National Institute of Physics and Nuclear Engineering (RO)); FOULDS-HOLT, Daniel (University of Cambridge (GB)); KEIZER, Floris (CERN); WOTTON, Stephen (University of Cambridge (GB)); MACIUC, Florin (Horia Hulubei National Institute of Physics and Nuclear Engineering (RO))

Presenter: COJOCARIU, Lucian Nicolae (Horia Hulubei National Institute of Physics and Nuclear Engineering (RO))

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