ULTRA-LOW NOISE SPADS IN 350 NM CMOS TECHNOLOGY FOR CHERENKOV RADIATION DETECTION IN PARTICLE AND ASTROPHYSICS

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12.–16. Sept. 2022

University of Edinburgh

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OUTLINE

- Introduction

- Pros and Cons: SiPMs for RICH detectors

- CSPAD Technology at Fraunhofer IMS
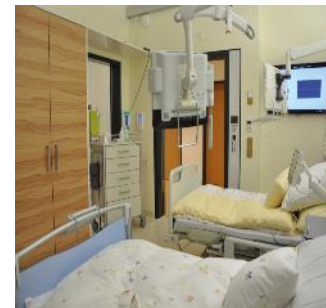
- 3D Integration (Back-SPADs)

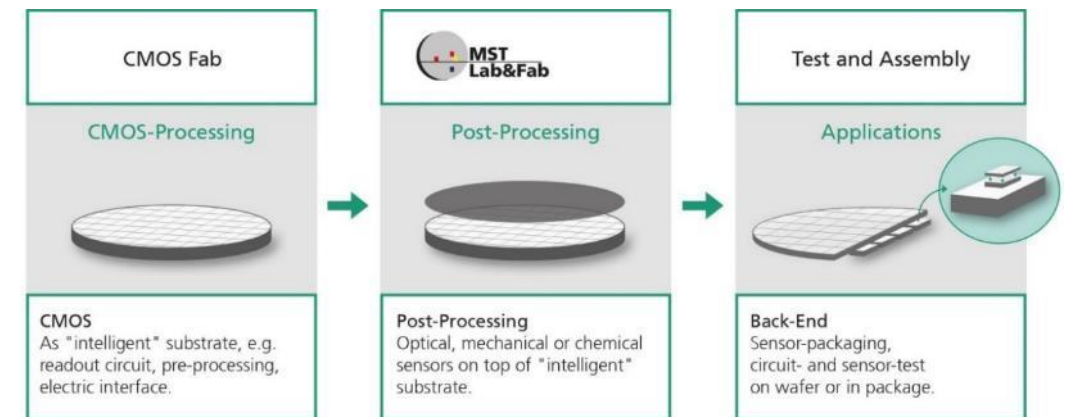- Summary

Sep 12 -16, 2022,
University of Edinburgh

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Introduction
Fraunhofer IMS

- Fraunhofer Institute for Microelectronic Circuits and Systems

- Located in Duisburg, NRW, Germany

- Founded 1984
- > 250 employees

- Infrastructure:
  - In-house 0.35 μm CMOS cleanroom with spezialized processes
  - Microsystem Lab for post-processing
 - Test and assembly capabilities

Introduction
SPAD Operating Principle

- Single-Photon-Avalanche-Diode (SPAD) is an avalanche photo diode which is operated with a voltage higher than the breakdown voltage (= Geiger-Mode)

- Single photons can be detected
  -> Photon Detection efficiency (PDE) = Avalanche Probability (AP) * Quantum Efficiency (QE)

- Fast operation with good time resolution (~100ps FWHM)

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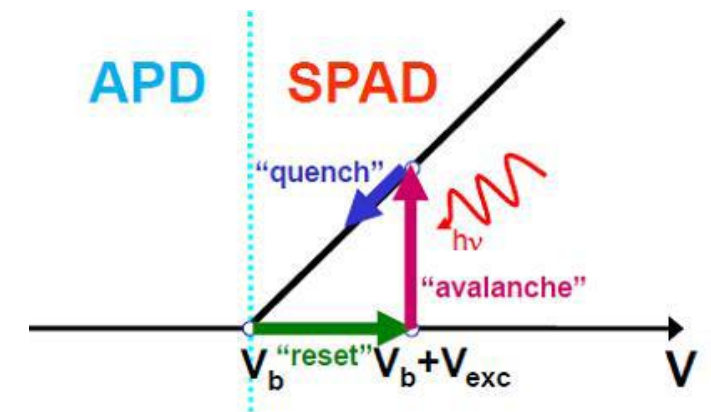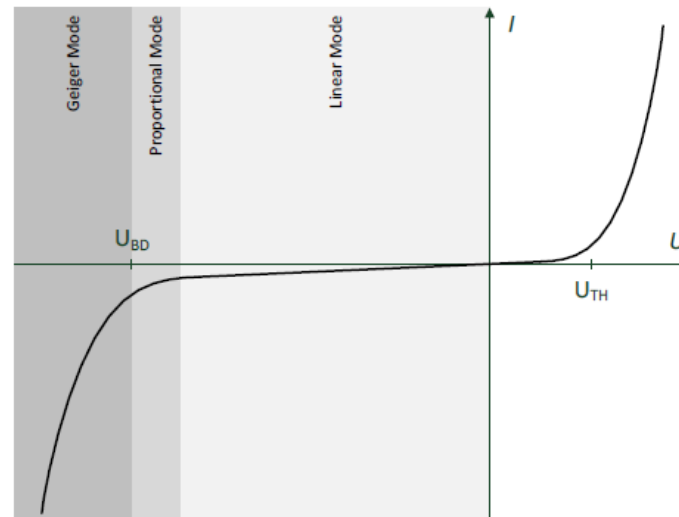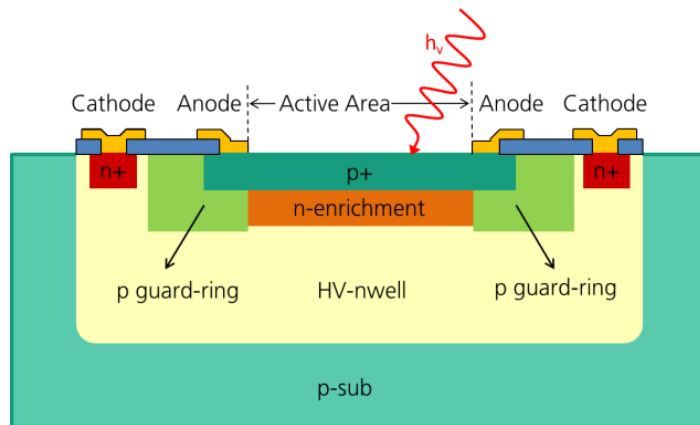
Introduction
Passive Quenching

- simple quenching with resistor, used in SiPM (array of conncected passive quenched SPADs)

- high dead time during Reset due to recharge of diode capacitance with the resistance R_B

Current Pulses

Diode Voltage

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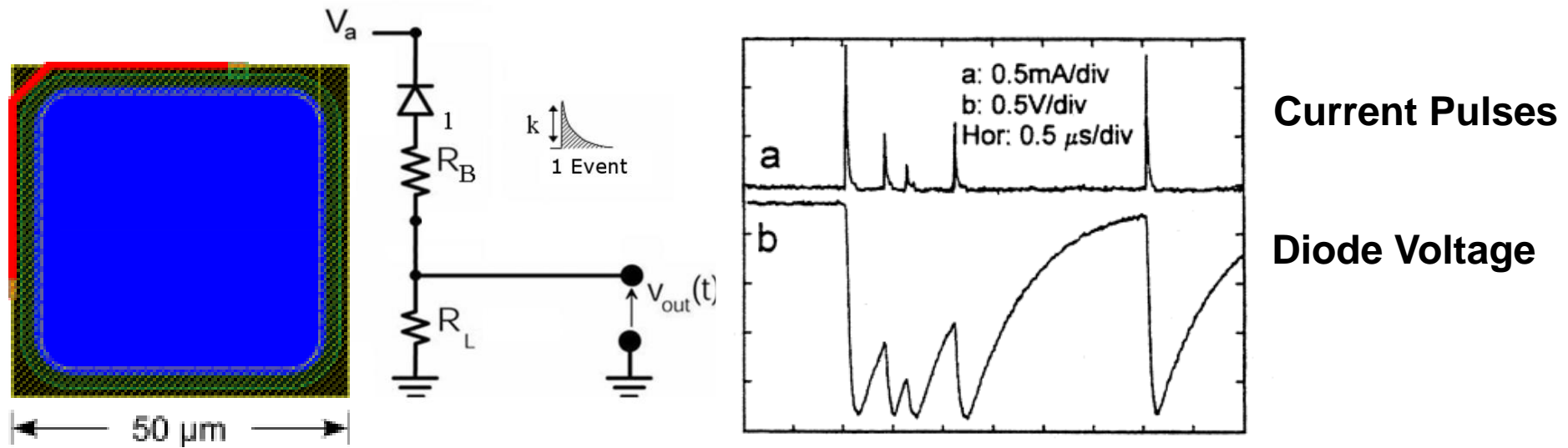
SIPMs for RICH detectors

PROS:

- high photodetection efficiency (PDE)
- operation in the magnetic field
- low supply voltage
- fast response
- flexible granularity
- compact

CONS:

- high dark count rate {~100kHz / mm² at RT)
- Radiation damage
- Cooling

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CSPAD (CMOS integrated SPAD)

Technology

- Avalanche Photodiode (APD) operated in Geiger mode

- Smart frontside illuminated pixels integrated into standard 0.35µm CMOS process (dual gate oxide, 4 metal layers)

Unique Selling Points

- Lowest Dark-Count-Rate

- High uniformity

- Picosecond time resolution

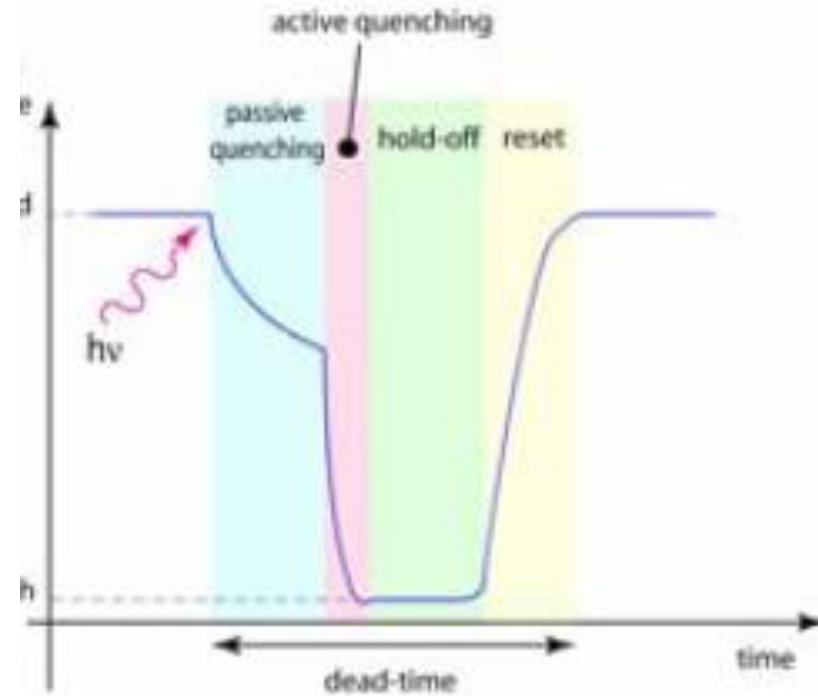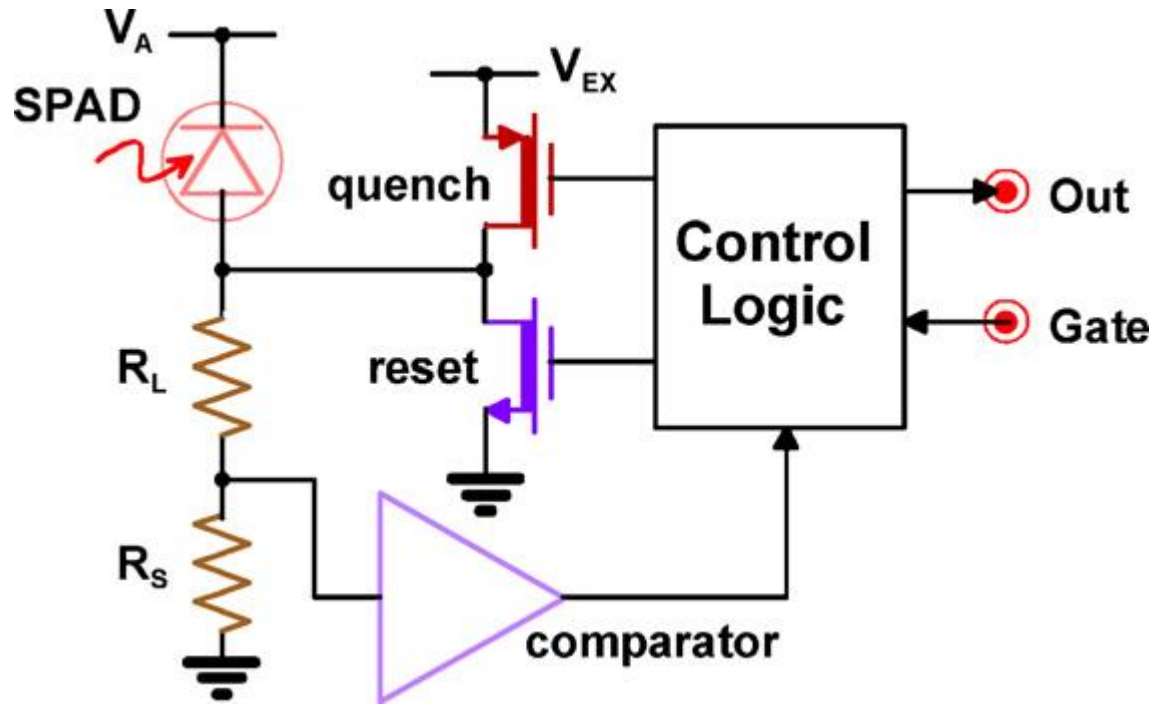- High sensitivity in blue and UV

Applications
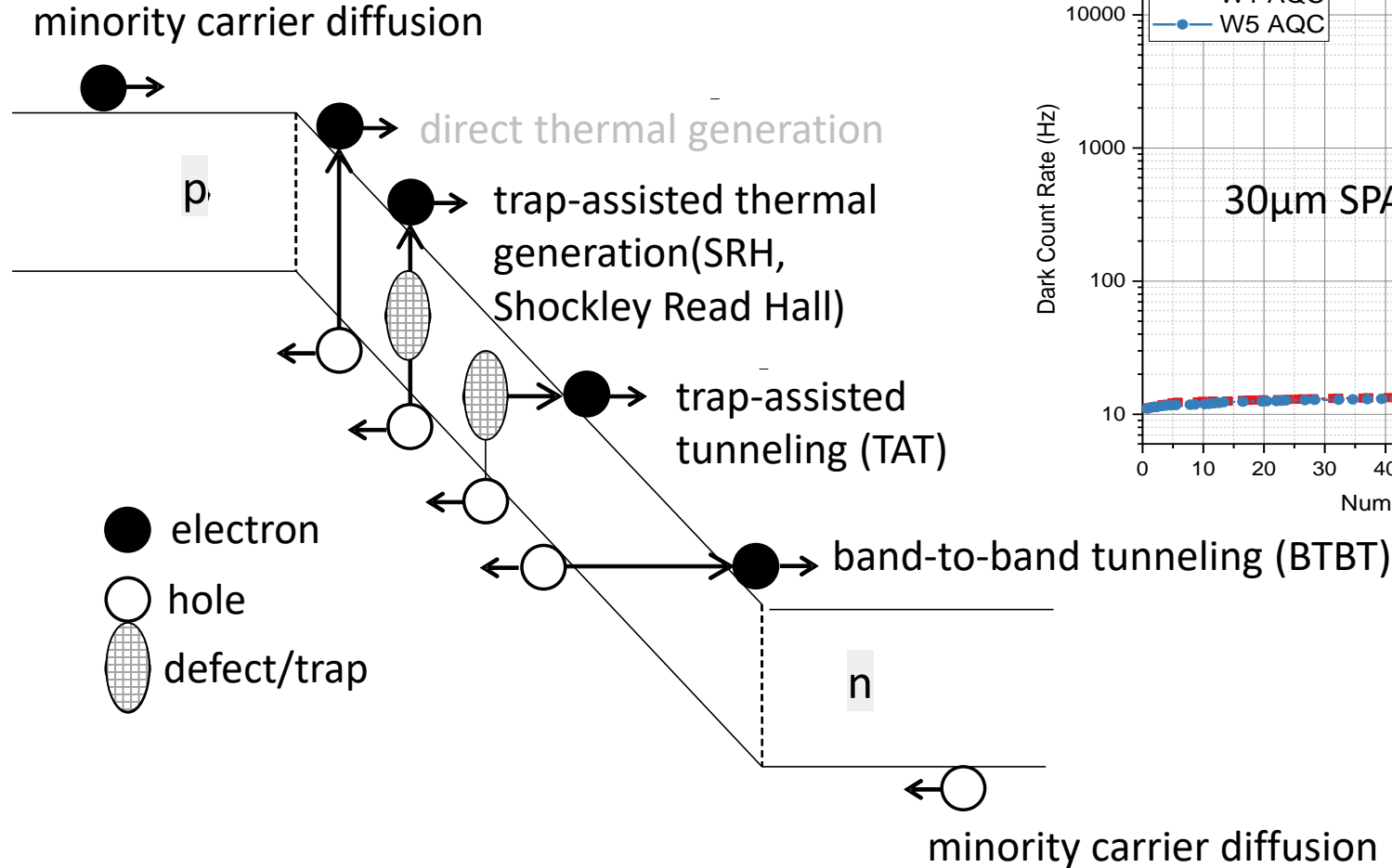
- LIDAR, Raman spectroscopy, low light imaging, FLIM
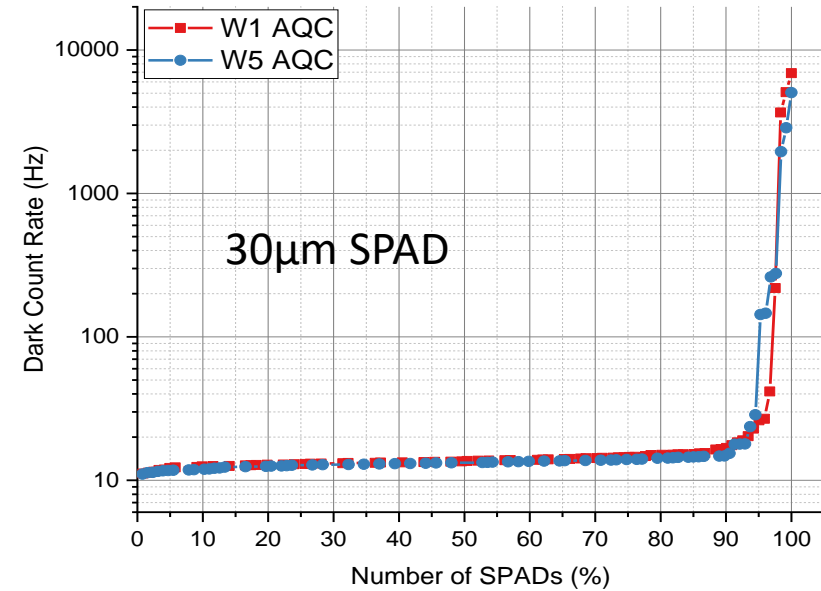
Fraunhofer IMS
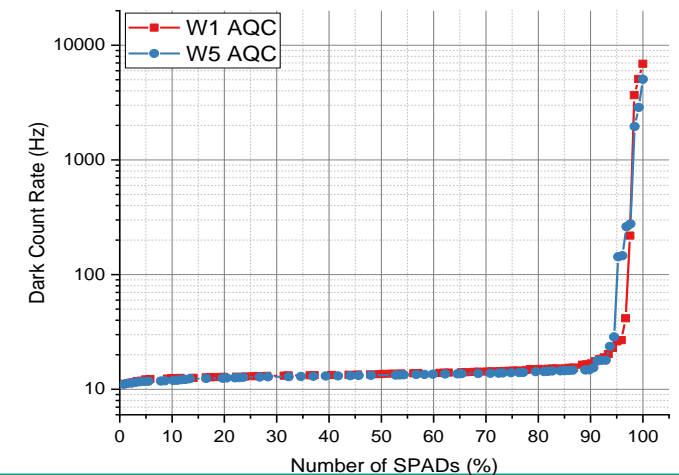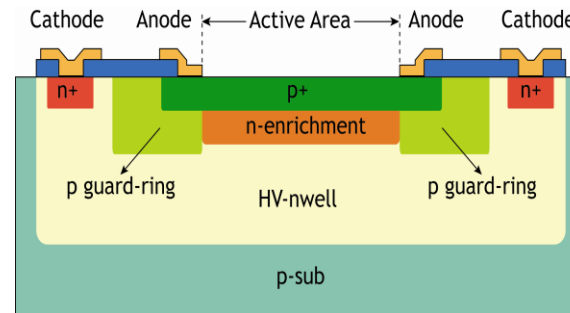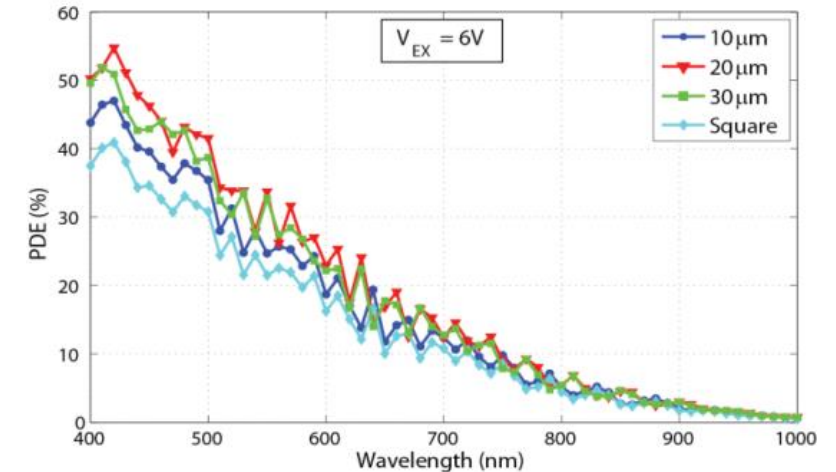
CSPAD
Active Quenching

F. Zappa et al., Sensors and Actuators A: Physical Volume 153, Issue 2, 3 August 2009, Pages 197-204

CSPAD
Sources for dark counts

minority carrier diffusion

direct thermal generation

trap-assisted thermal generation(SRH, Shockley Read Hall)

trap-assisted tunneling (TAT)

band-to-band tunneling (BTBT)

● electron

○ hole

defect/trap

minority carrier diffusion

p

n

30µm SPAD

$$DCR_{total} = DCR_{SRH} + DCR_{TAT} + DCR_{BTBT} + DCR_{Diff}$$

CSPAD
Dark Count Rate

World's lowest Dark Count Rate (DCR) for CMOS integrated SPADs:

- Band2Band tunneling was reduced in order to lower the DCR at low temperatures (2. Generation)

- Down to **0.04 cps/mm²** by cooling to 160 K or
  400 cps/mm² at 267 K

- "Hot SPADs" could be deactivated

- DCR at higher temperature is limited by diffusion current from the non-depleted area, fully depleted BSI or an n-buried layer can reduce this current

$4 \cdot 10^{-4}$ cps/µm²

@ 267 K

Single SPADs

$4 \cdot 10^{-8}$ cps/µm²

@ 160 K

Digital SiPM
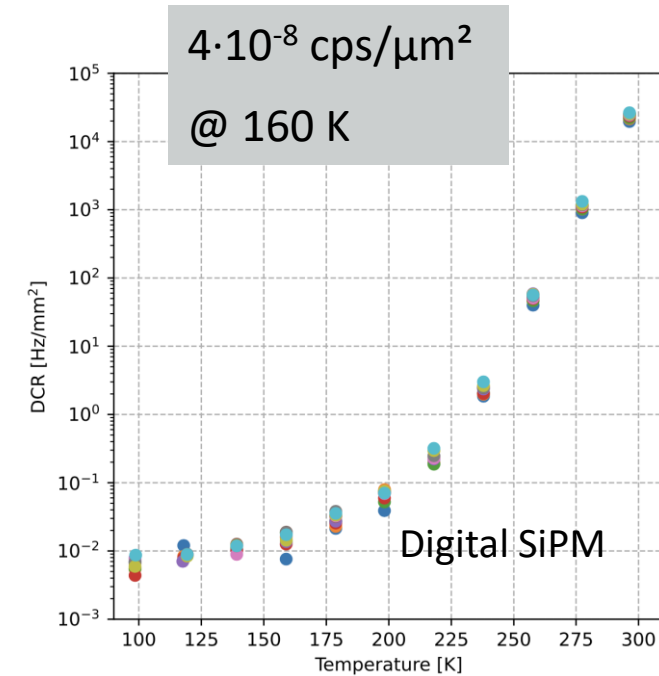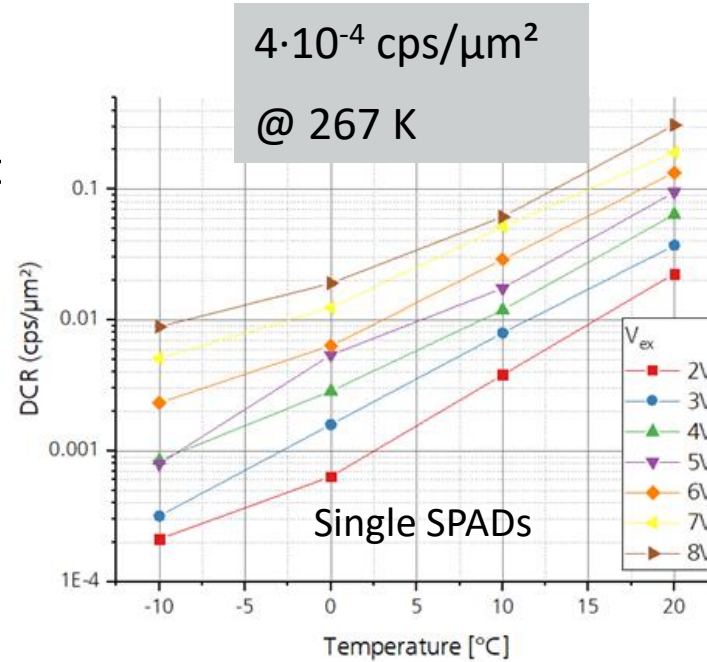
Fischer, P., SPAD Array Chips with Integrated Readout with High Fill Factor and Low Dark Count Rate at Low Temperatures, 15th Pisa Meeting on Advanced Detectors (May 2022)

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CSPAD Development
Linear sensor for spectroscopy applications
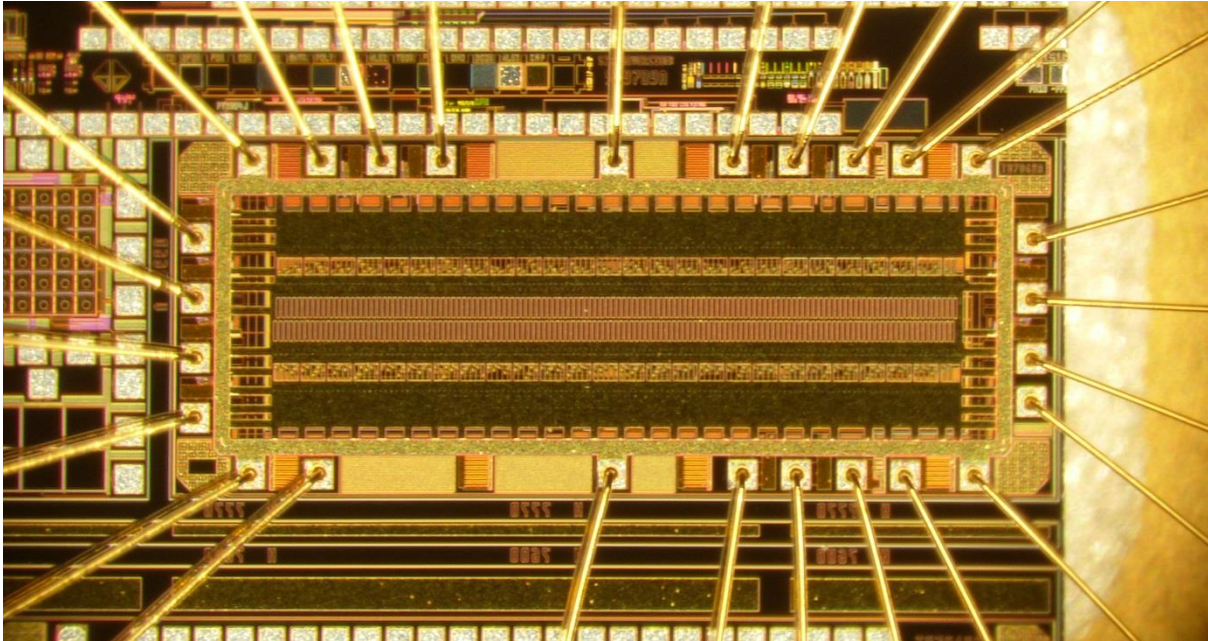
Specifications

- Pixel pitch: 20 μm (along sensor)
- SPAD area: 14 μm × 76 μm
- Pixel count: 2 × 128
- Fill factor: 60 %

- Measurement period: 2.95 μs
- Typ. Gating width: 12.5 ns
- Crosstalk: 13 %

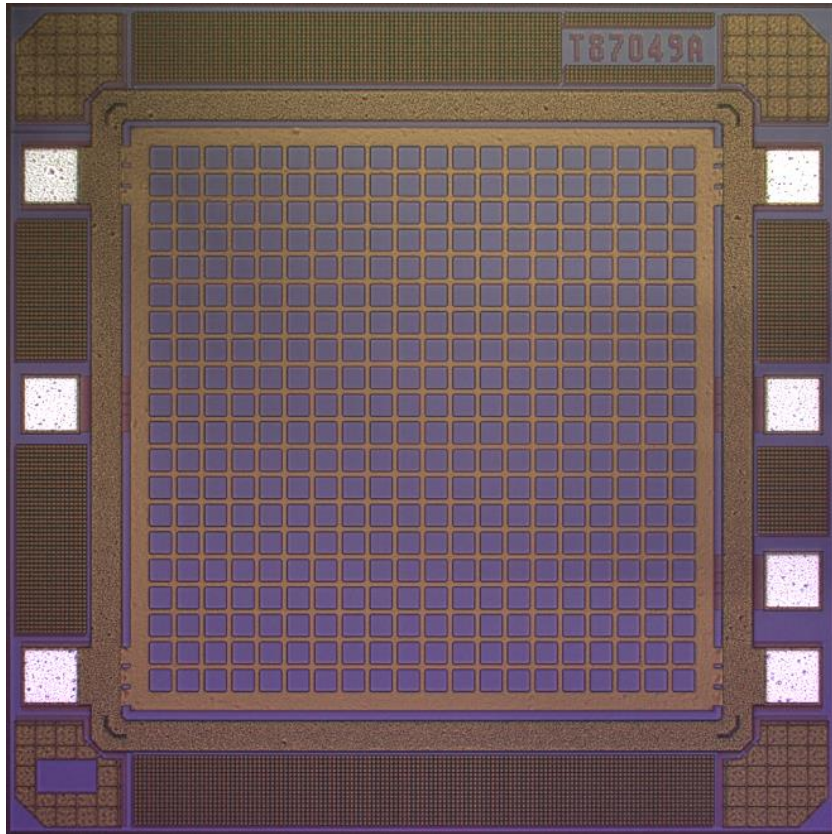+ several line sensors for LIDAR applications

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CSPAD Development
Analog Silicon Photo Multiplier

Photograph of SiPM designed and fabricated at IMS
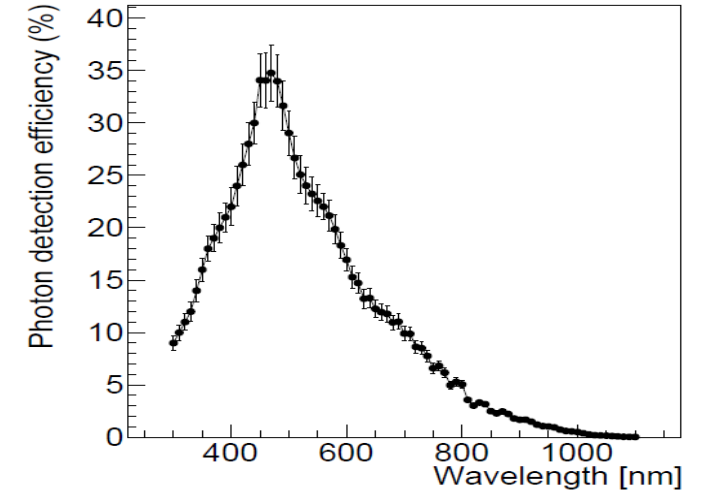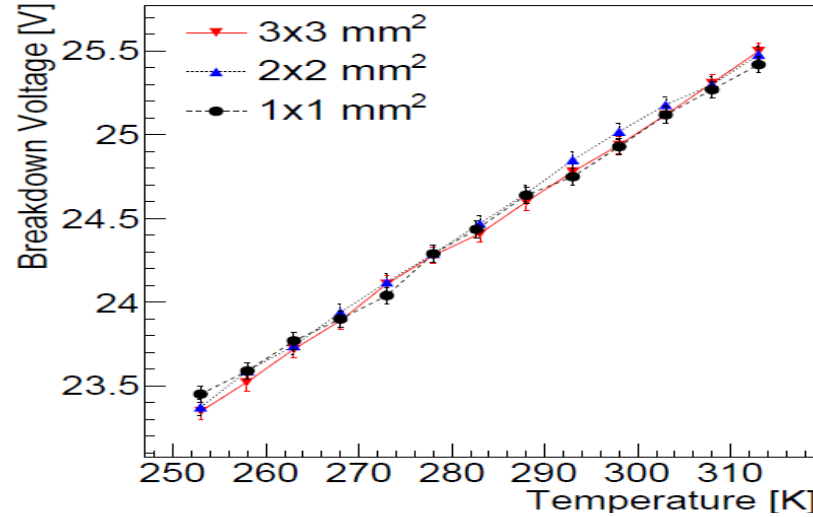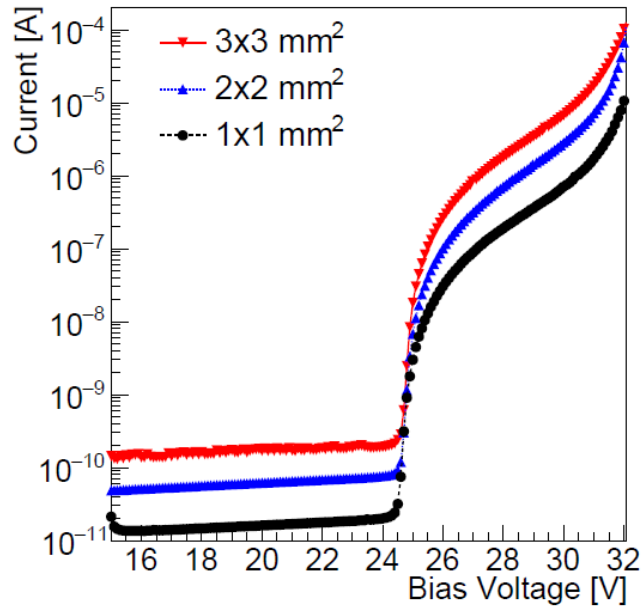
- **SiPM specifications**

  - Pixel pitch: 50 µm

  - Array size: 1 mm × 1 mm

  - Fill factor: 68 %

  - Dead time: 80 ns

  - Breakdown voltage: 26 V

- **CMOS integration enables**

  - Amplifiers
    $\Rightarrow$ increase output signal amplitude

  - Impedance converters
    $\Rightarrow$ increase timing resolution
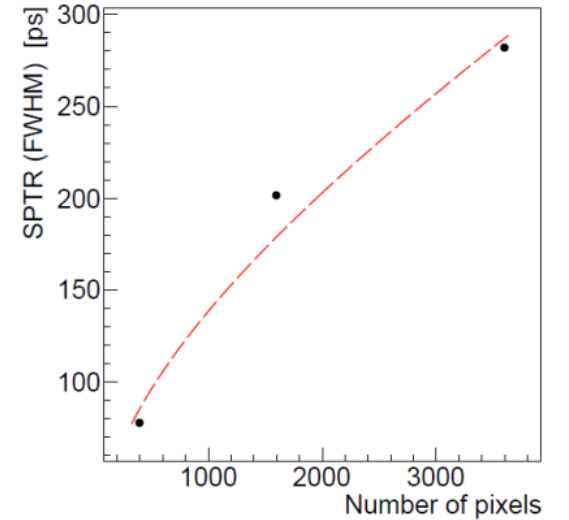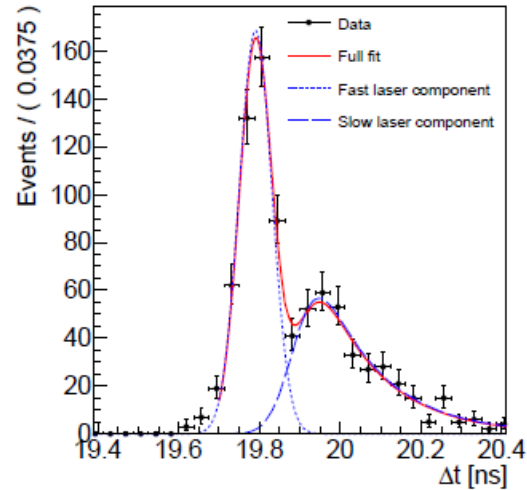
  - deactivation of hot pixels

  - in-pixel memory

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External CSPAD Use
Analog Silicon Photo Multiplier

SiPM area $[\text{mm}^2]$	Dark count rate $[\text{KHz/mm}^2]$	Cross talk %
1	166.2 ± 0.4	5.3 ± 0.4
4	188.6 ± 0.2	5.8 ± 0.2
9	232.2 ± 0.1	5.7 ± 0.3

TABLE II

DARK COUNT RATE AND CROSS TALK FOR THE DIFFERENT SiPMs AT A REFERENCE OVERVOLTAGE OF 2.5 V.

X. Liang et al., "Silicon photomultipliers with area up to 9 mm² in a 0.35 nm CMOS process", IEEE J. ELEC. DEV. SOC. 2019
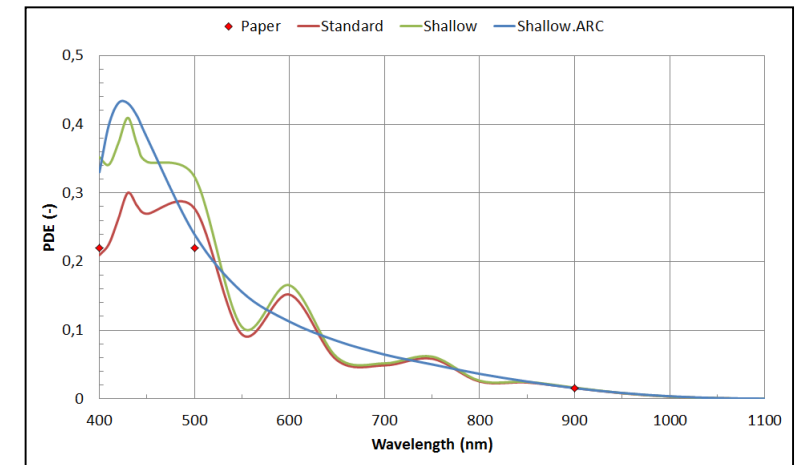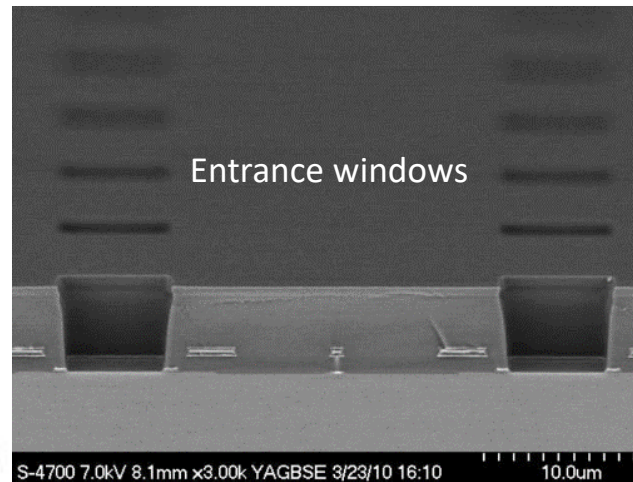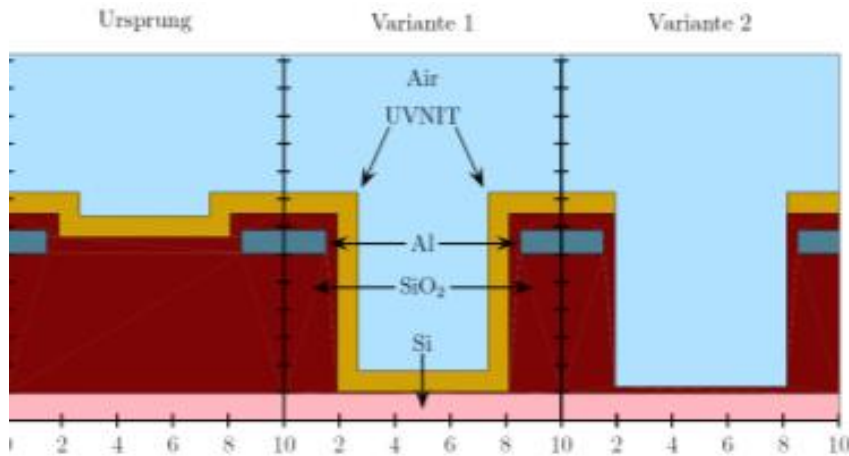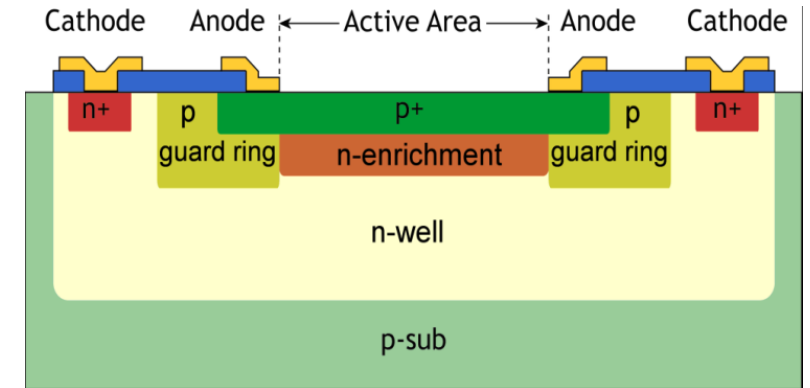
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External CSPAD Use
Additional Developments Analog Silicon Photo Multiplier

- Development DOSE(Deep Optical Stack Etching) + ARC (Anti Reflective Coating)

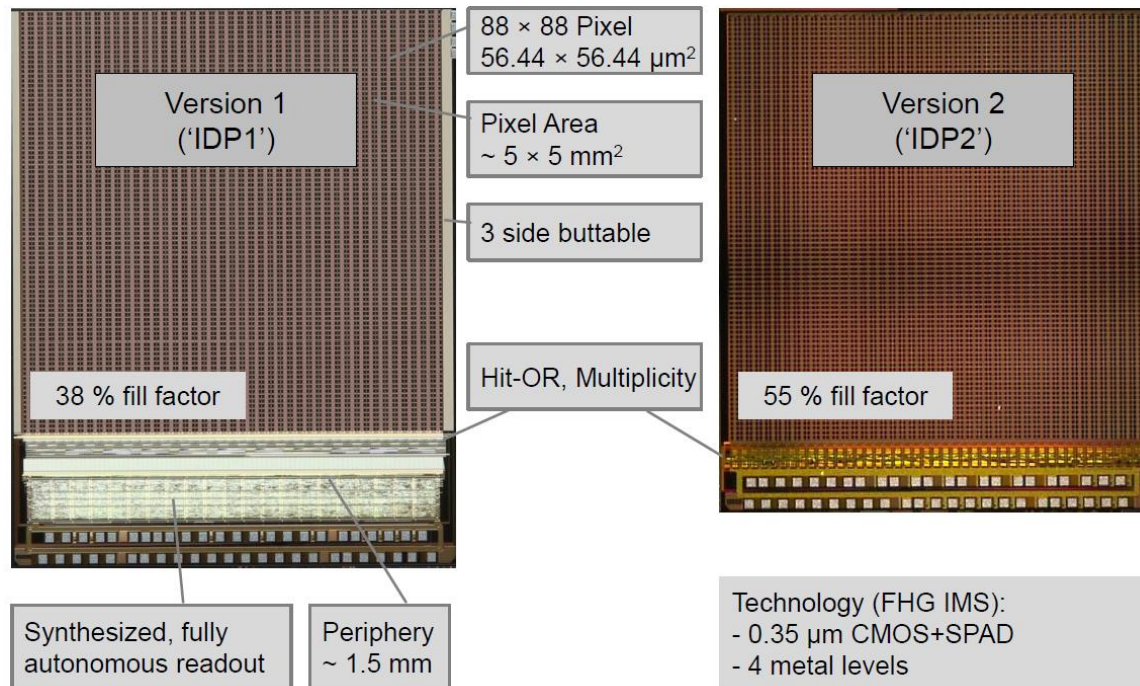- For PET SPADs shallow p+ doping (PDE Improvement)

Entrance windows
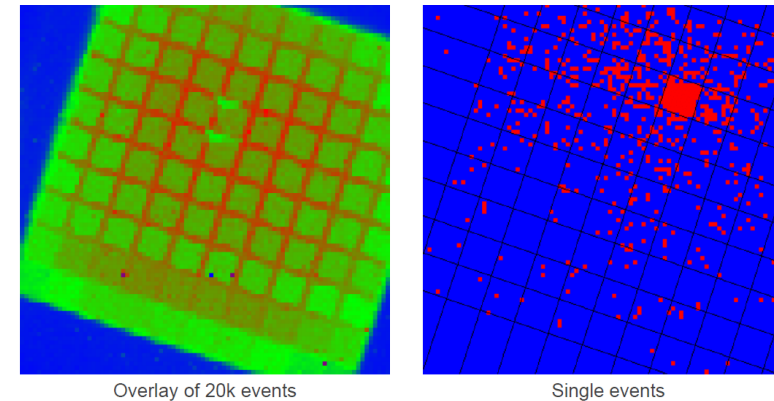
External CSPAD Use
Digital Silicon Photo Multiplier

88*88 SPAD array with full 2D readout (dSiPM)

Goal is to use full 2D image information to study scintillators, do imaging (fluoresence, night vision, astronomy), do physics (Compton scattering ..)

Version 1 ('IDP1')

88 × 88 Pixel
56.44 × 56.44 µm^2

Pixel Area
~ 5 × 5 mm^2

3 side buttable

Hit-OR, Multiplicity

38 % fill factor

Synthesized, fully autonomous readout

Periphery ~ 1.5 mm

Version 2 ('IDP2')

55 % fill factor

Technology (FHG IMS):
- 0.35 µm CMOS+SPAD
- 4 metal levels

Scintillator measurements:

LYSO arrays with 0.48 mm pitch

Overlay of 20k events

Single events

P. Fischer, Universität Heidelberg, IEEE NSS 2014, Seattle, 10-15.11.2014

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3D Integration (Back-SPADs)
Motivation: MiSPiA smart-pixel for direct TOF
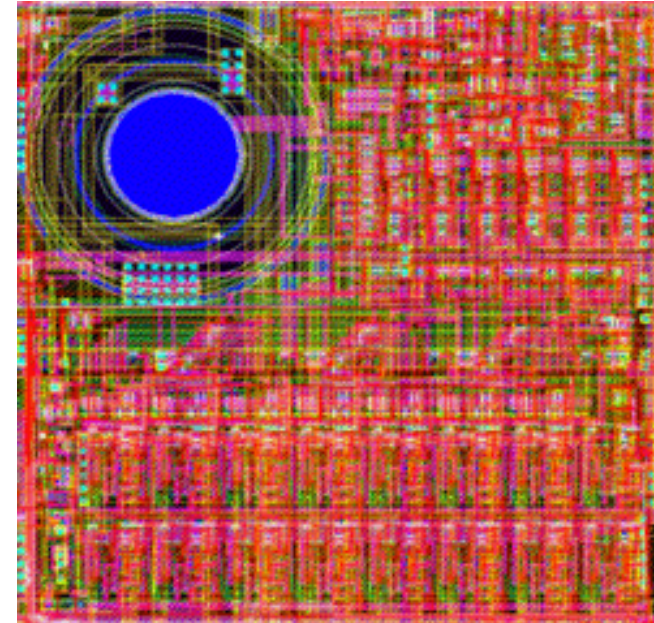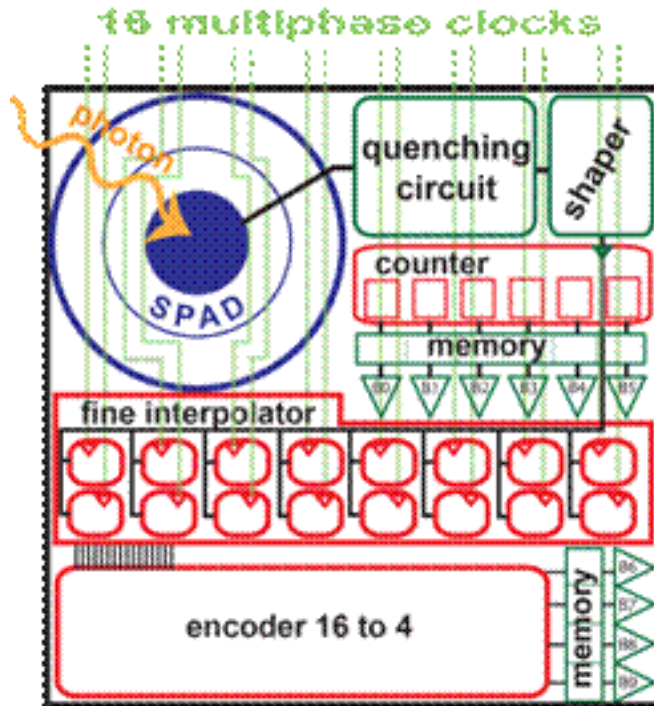
- Block diagram (left) and Layout (right) of the SPAD based smart pixel, showing the main components
- The pitch is 150µm; the SPAD has 30µm diameter (Pixel fill factor 3.14%)

MiSPIA (everyphotoncounts.com)
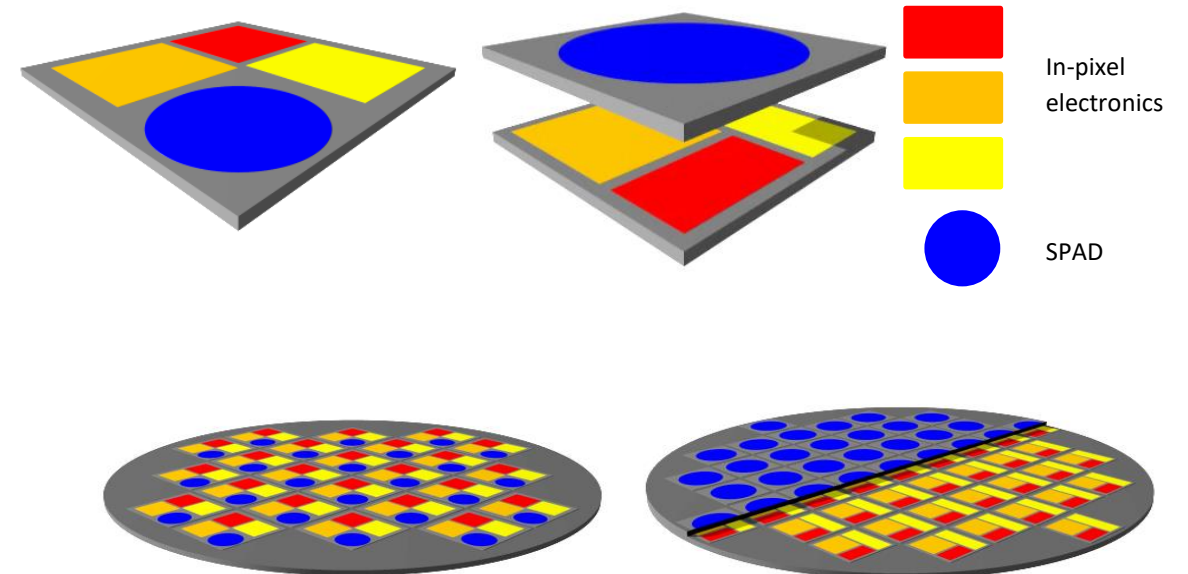
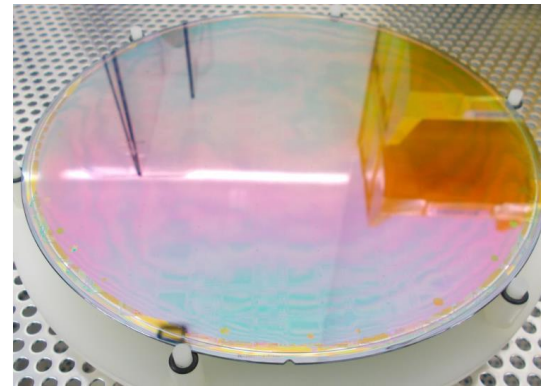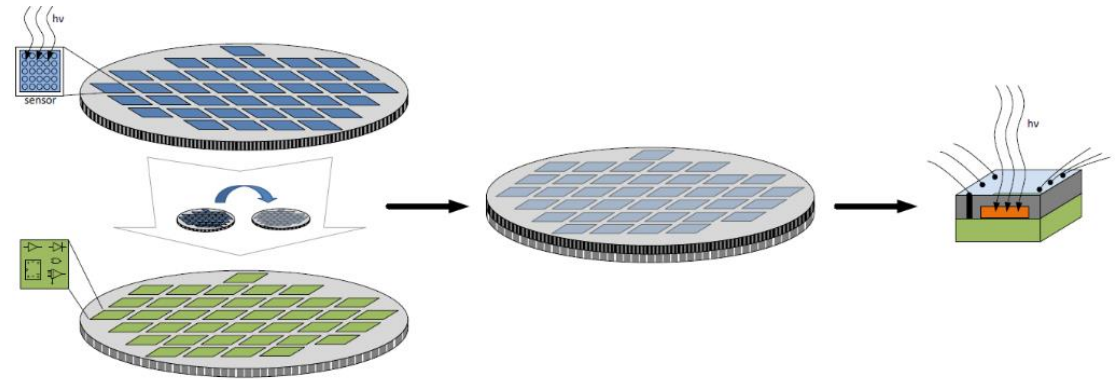# 3D Integration (Back-SPADs)
Concept: Wafer-To-Wafer Bonding

- Optical Sensor with maximum fill-factor, optimized substrate-doping, …

- Huge read-out circuitry needed, dense logic → 2-wafer-solution (also foundry CMOS or Sensor wafer possible)

- Straight, symmetric wiring necessary between pixel and read-out → wafer-stacking

- Fine pitch interconnect between wafers required →"µVias" with ALD

In-pixel electronics

SPAD

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3D Integration (Back-SPADs)
Integration technology

- Direct 8" wafer bonding

  - Layout and process optimization for planarity

  - Multi-stage chemical mechanical planarization (CMP)

  - Alignment analysis (accuracy < 1 μm)

  - Bonding interface analysis by scanning acoustic microscopy (SAM)

- Combination of technology nodes

  - High performance electronics with ultra-low noise SPADs

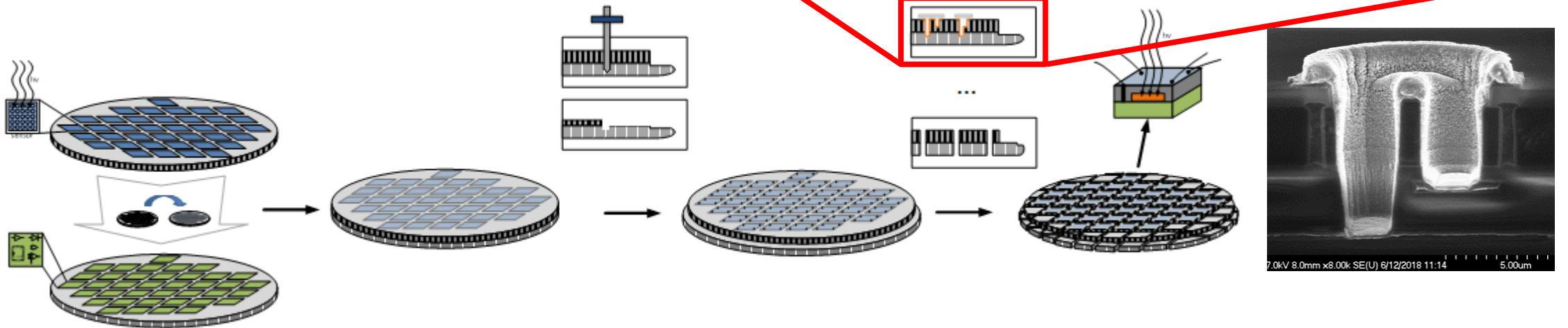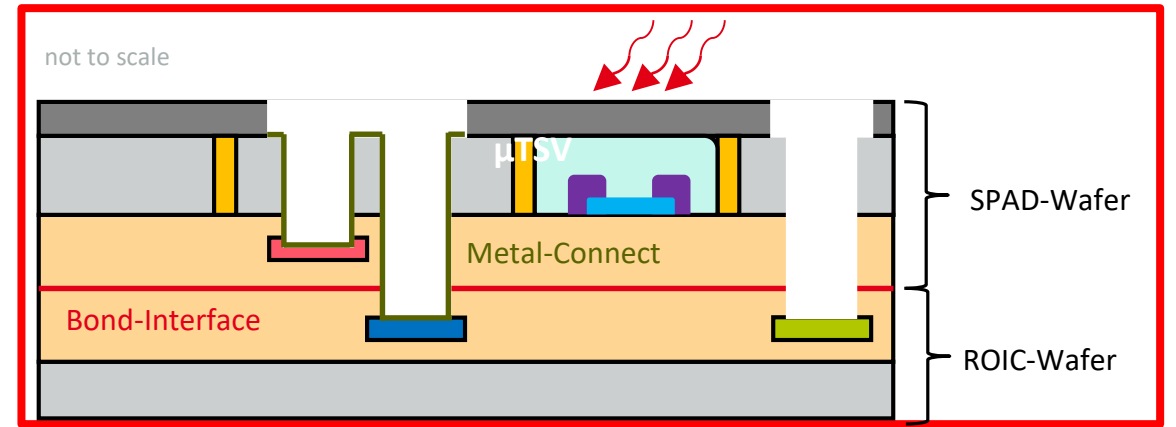 - Read-out close to sensor area

Wafer stack

SAM image

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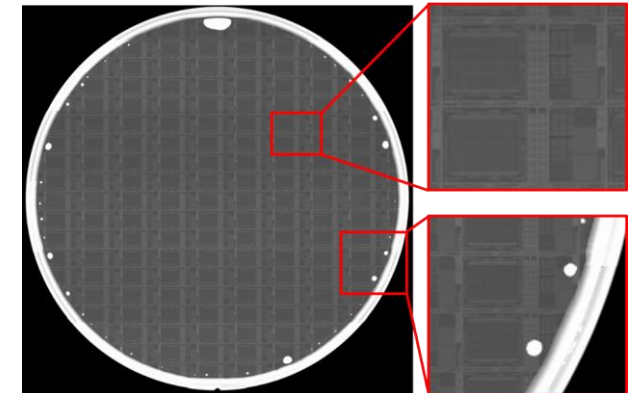
3D Integration (Back-SPADs)
ALD for µVias

- **Connection of sensor and read-out wafers**

- "µVias" with ALD

■ Trenches	■ SPAD-Top-Metal
■ Guard-Ring	■ ROIC-Top-Metal
■ Isolation	■ Wire-Bond-Pad
■ Anode	■ Silicon
■ Cathode	■ Bondoxid
■ Well	

3D Integration (Back-SPADs)
CSPAD LIDAR Sensors

- **Connection of sensor and read-out wafers**

- Wafer-2-wafer solution for backside-illuminated LIDAR-Sensors

- Several LIDAR demonstrators designed and fabricated

- W2W interconnect "µVia" with ALD

CSPAD

- Array with $\geq$ 10k pixels (x4 SPADs; x2 Vias) in fab

  - Photon timing and counting mode

  - Variable coincidence settings (Each pixels with 4 SPADs)

  - In-pixel time-to-digital converters (TDC) and built-in TDC monitoring

  - Adaptive background light suppression (Reduced sunlight noise)

  - Flexible Resolution (Region of Interest)

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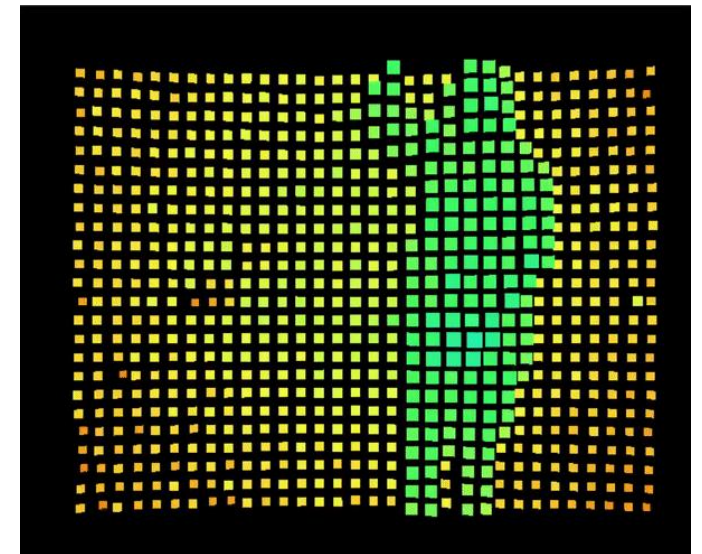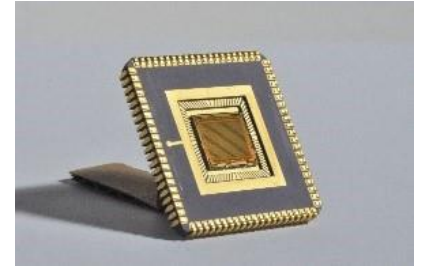
3D Integration (Back-SPADs)
EPI and Doping Profile

Change from SOI -> EPI Wafers (reduced DCR)

- Optimized doping profile and silicon thickness for (high avalanche efficiency, fully depleted, PDE> 40% for 300-800 nm)

- Anti reflective coating (now optimized for 905nm LIDAR applications, but other wavelengths possible)

Challenges:

- Etch-Stop -> doping selective etching necessary -> HNA

- CMP-planarization

- Backside passivation for fully depleted diodes

Detection efficiency *(simulation)*

d_{target}

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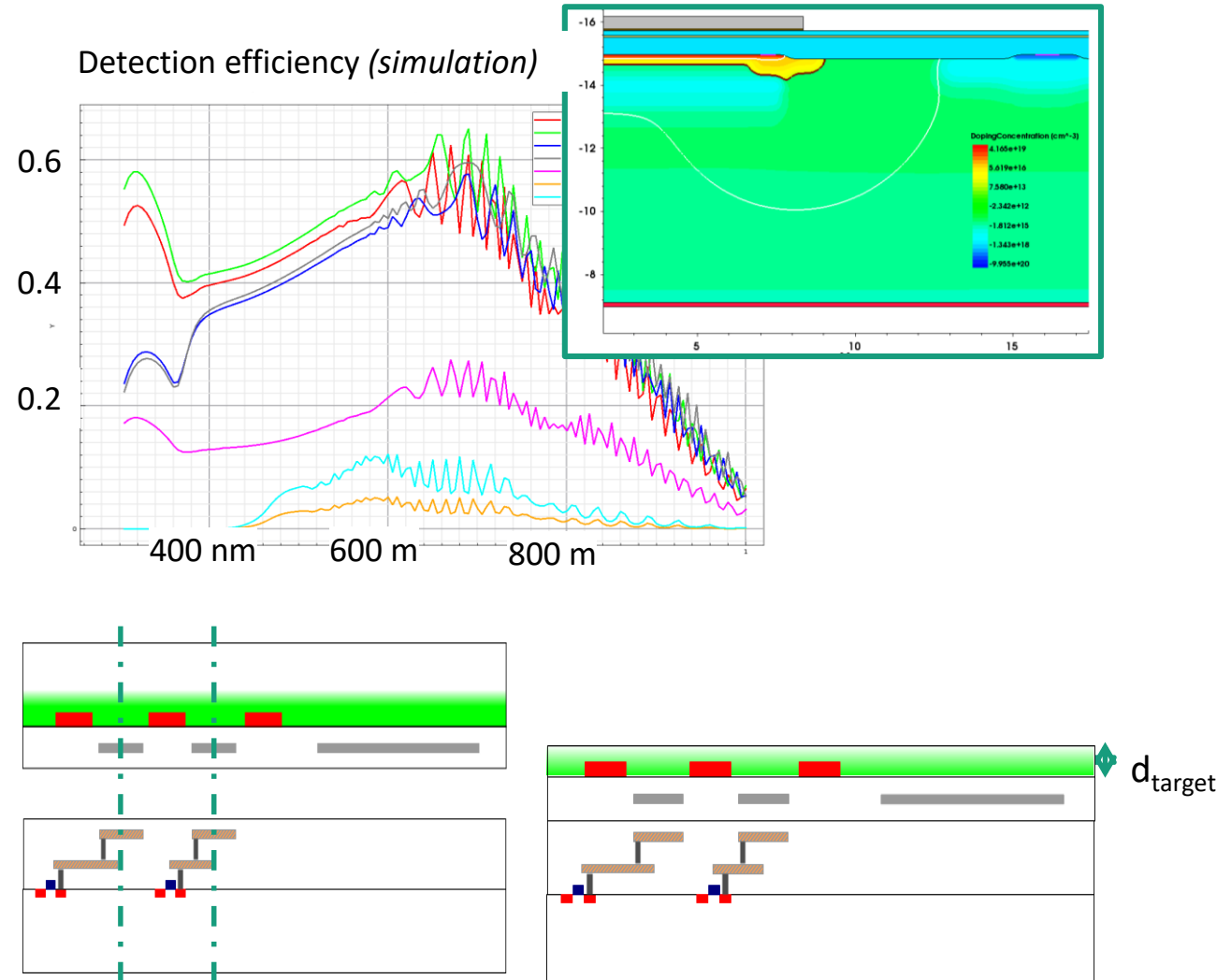
3D Integration (Back-SPADs)
Low Temperature PureB deposition

- Deposition of a few nm thick boron film

  - similar to boron delta doping

  - very good passivation

  - no degradation due to EUV, DUV, UV radiation

  - Full depletion of the film is possible

  - CMOS Backend compatible

  - P+ doping above BOX of the
    SOI wafer is not necessary

  - Passivation for EPI wafer (Back SPADS)
    could be solved
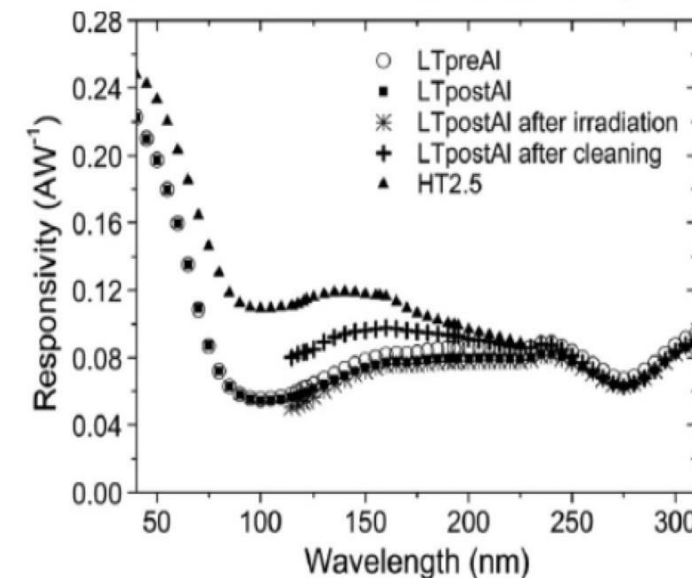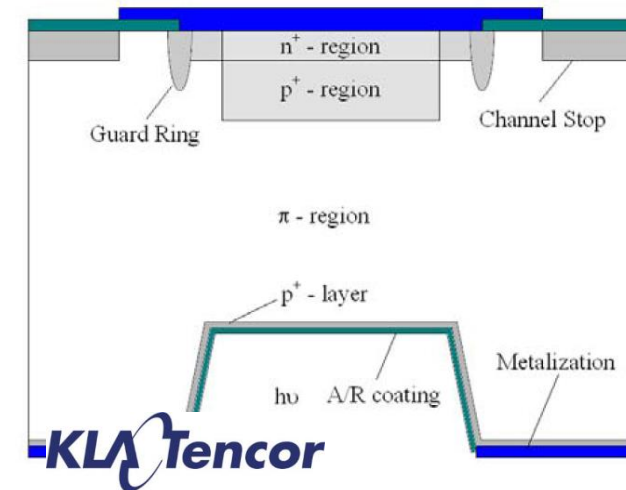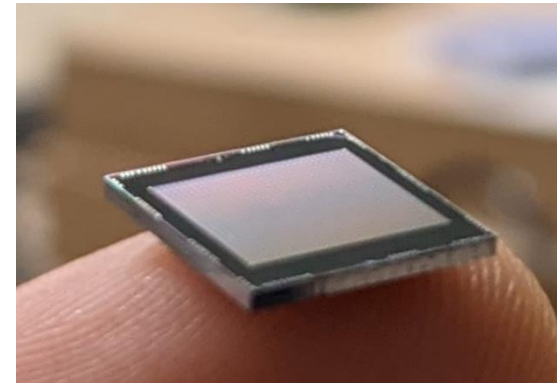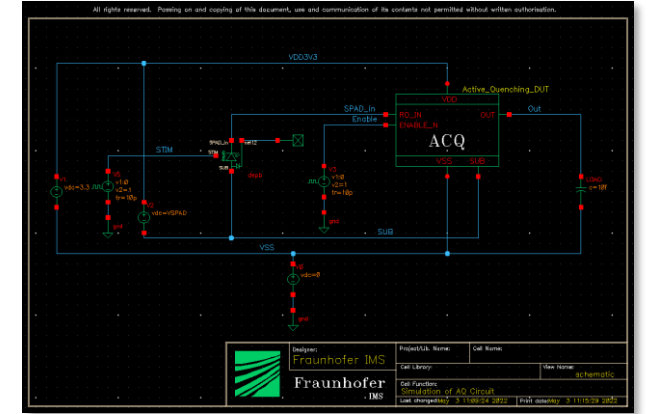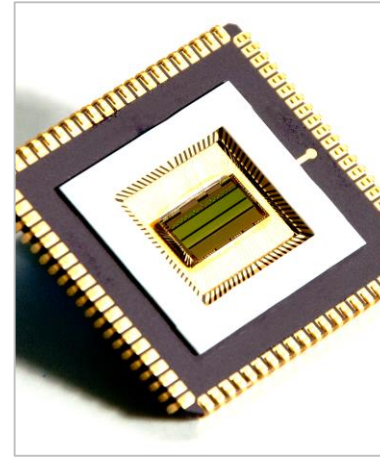
Circuit Design

- Long term experience in circuit design for image sensors (>10 years SPADs)

- Advanced simulation tools for performance improvement

- High performance quenching circuits

- High precision timing electronics (TDC)

- Goal 20 ps timing resolution

- Cadence tool set up

Summary

- Introduction to the in CMOS integrated SPAD technology CSPAD

- Presenting the DCR results and limits

- Next step for digital SiPMs -> 3D Integration with in-pixel (Micro Cell) electronics

- 3D Integration developments at Fraunhofer IMS

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https://www.ims.fraunhofer.de/en/

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- »Vision 2022« Oct. 04.-06., Hall 10- booth 10E76