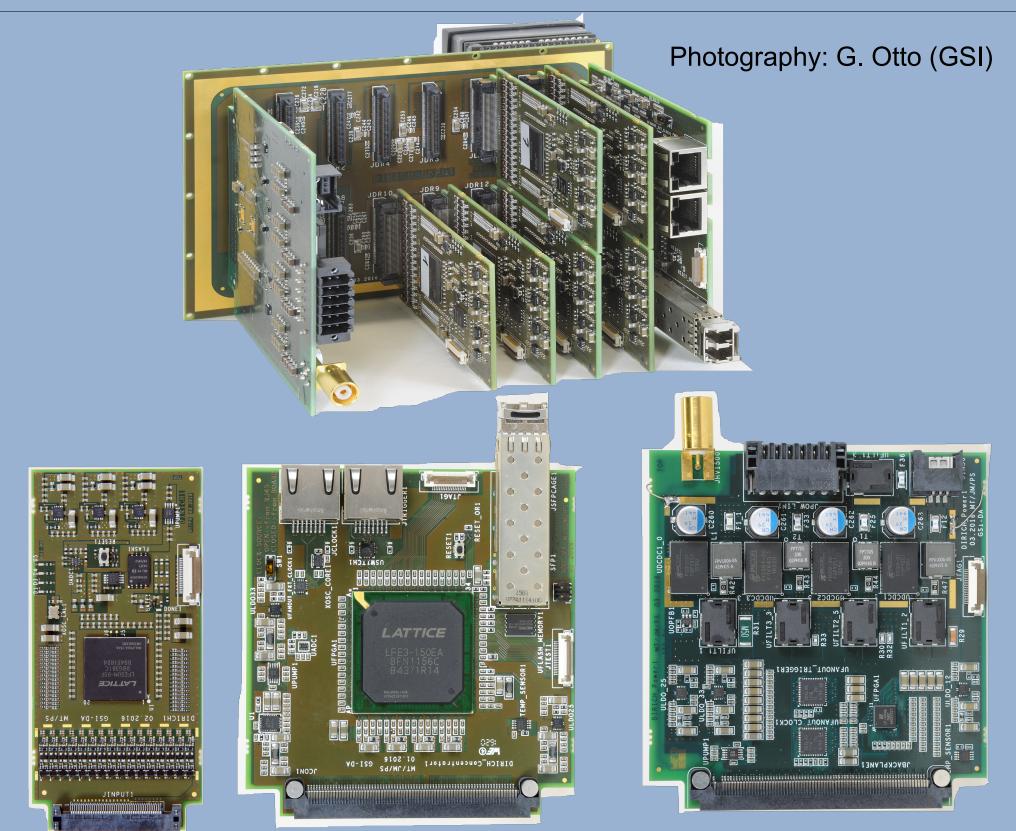


Qualification of DIRICH readout chain

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DIRICH readout chain

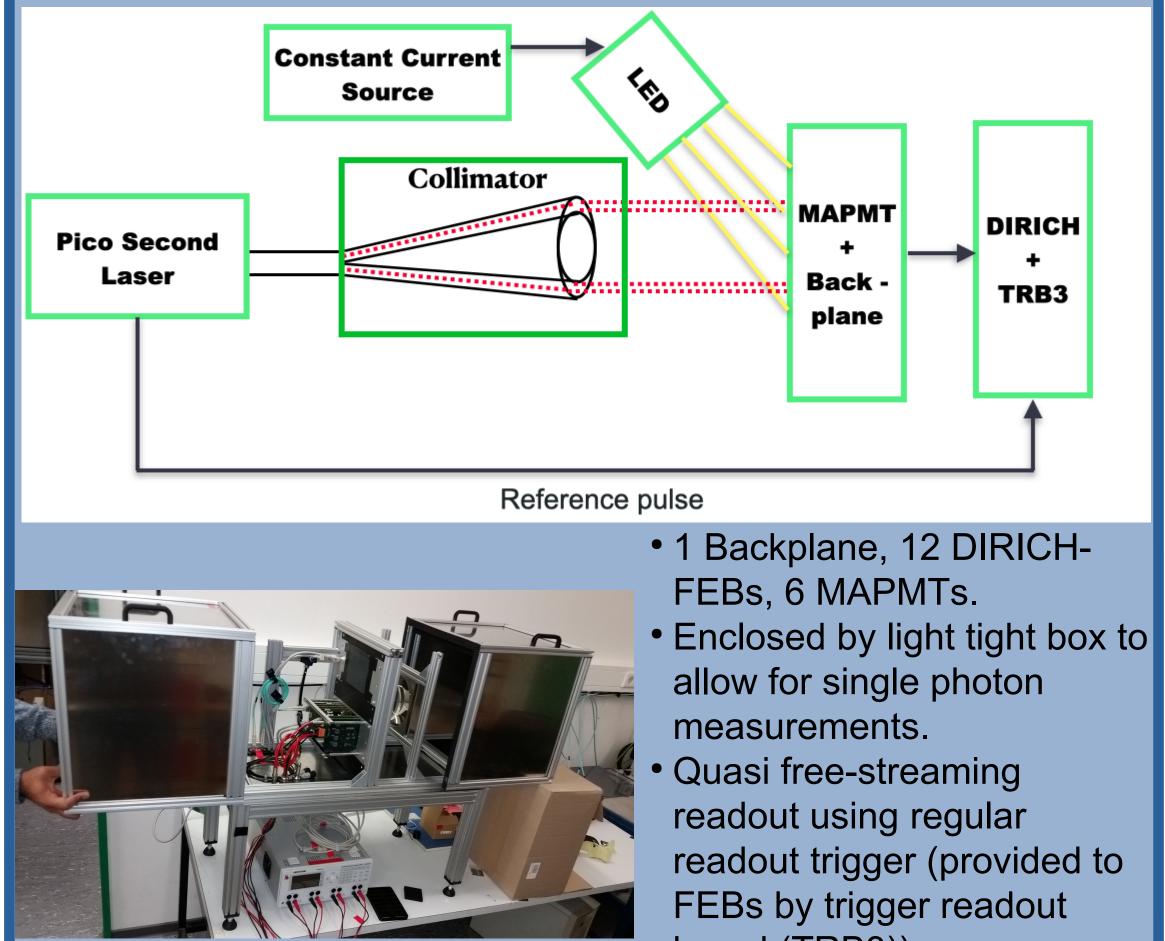


- Low power modular FPGA based readout chain.
- Six 64ch HAMAMATSU H12700 MAPMTs and readout electronics connected by backplane which provides light and gas tight seal.

DIRICH front-end module (FEB) :

- Reads out half MAPMT (32 + 1 channels). • Each channel features own inverter amplifier, FPGA based discriminator and TDC (Lattice
- ECP5).
- Leading and trailing edge measurements \rightarrow Time over Threshold.
- Leading edge timing precision ~ 20 ps RMS.

Measurement set-up



Power module

Combiner module :

 Combines data from 12 DIRICH-FEBs to 2.4 Gbit link to common readout interface. Distributes clock input to individual FEBs.

Power module :

• Distributes high voltage for PMTs (~ -1000V). • Distributes low voltages to read out modules via onboard DCDC convertors $(32V \rightarrow \{1.1, 1.2, 2.5, 3.3V\}).$

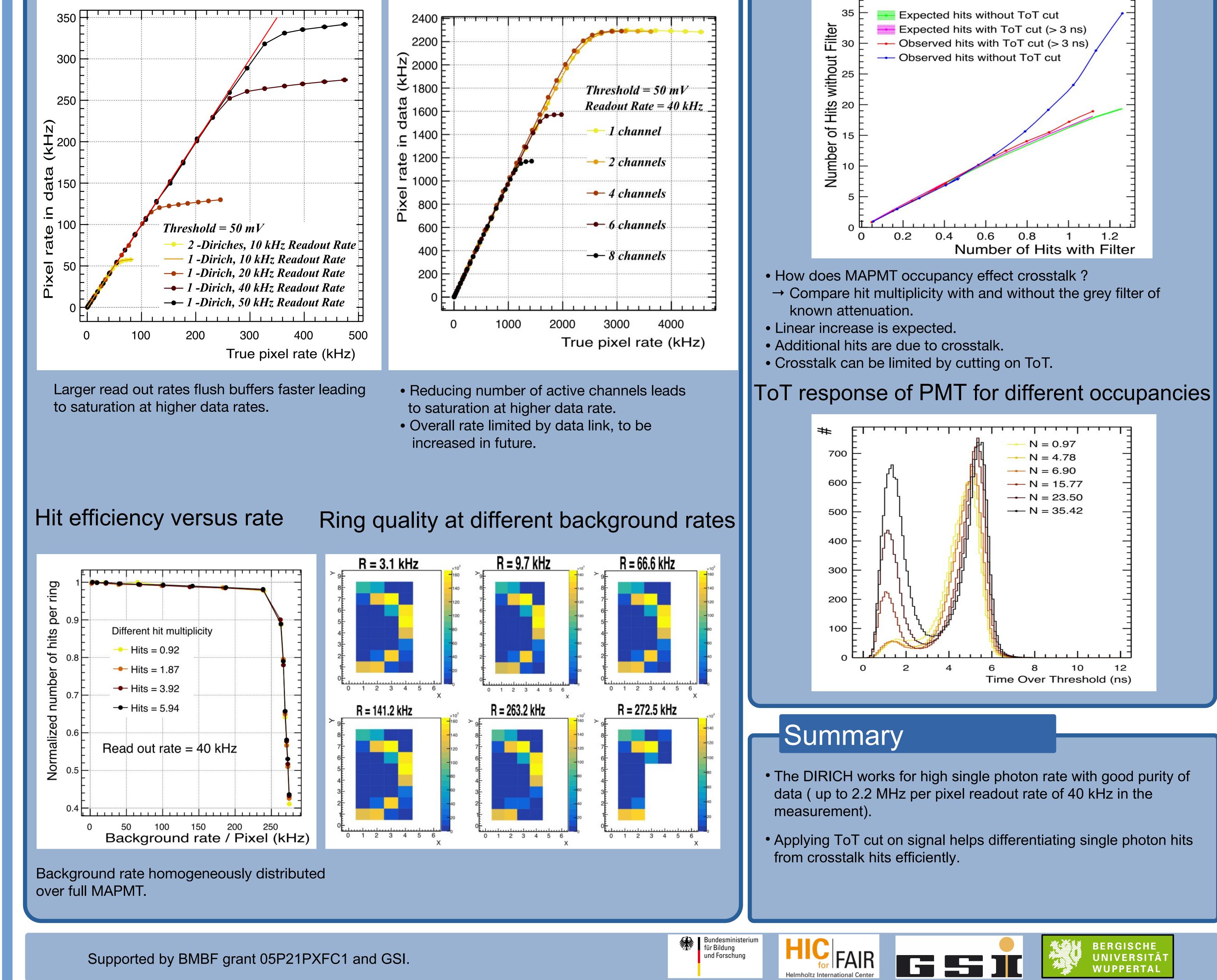
- board (TRB3)). • 2 light sources : Picosecond
- pulse Laser (Ring), Pulsed LED (homogeneous).

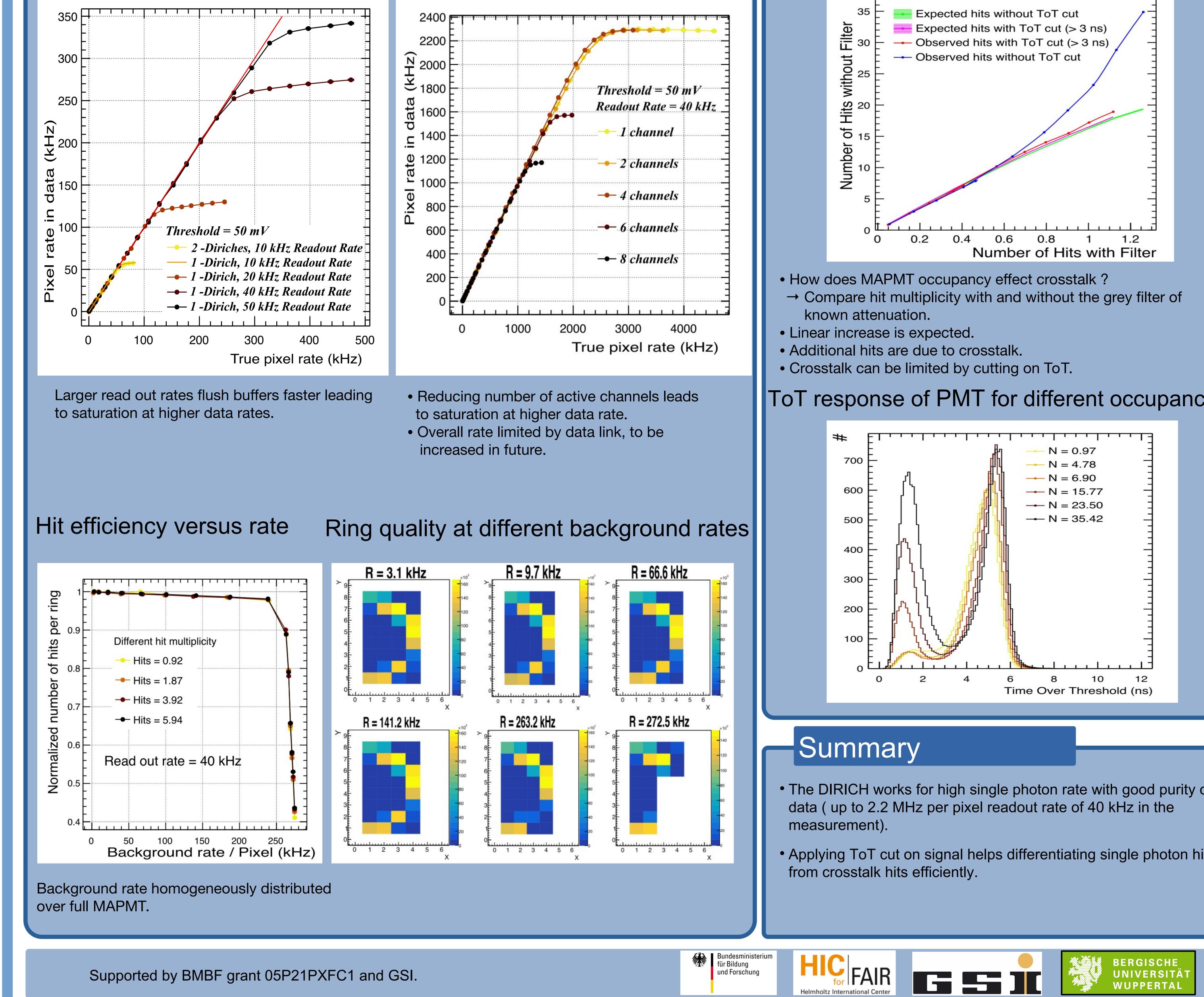
Rate capability measurement

Combiner

DIRICH

Rate limit single DIRICH channel





Crosstalk suppression using ToT

