Development of an integrated housing for SIPM for future RICH photon-detectors

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Overview

- The housing of photo-sensors for future RICH detectors is a complex task, regardless of the sensor choice, due the **many requirements**.
  In order to save on the required resources and simplify the design, **different functions should be possibly integrated all together**.
- **This led to the development of the, today operational, LHCb/RICH focal surface photo-sensor array, for Hamamatsu MAPMT.**
  - See presentation: *The LHCb RICH Upgrade*, A. Sergi, this conference.
- For the LHCb/RICH Upgrade II, for the Run 5 of the LHC at CERN, the MaPMT will be replaced since they do not fully fulfill the detector requirements. The baseline sensor is Silicon Photo-Multiplier (SiPM)
  - See presentation: *The LHCb RICH Upgrade II*, S. Wotton, this conference
  - See presentation: *A novel fast-timing readout chain for LHCb RICH LS3 enhancements and prototype beam tests*, F. Keizer, this conference.
  - The FTDR document on Upgrade II has been recently approved by LHCC

Overview 2

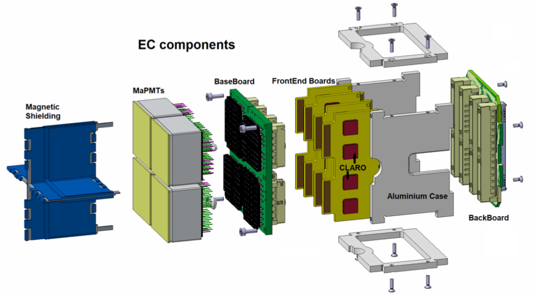
- For SIPM-like sensors, some sort of **active cooling** is required: the **passive cooling used for MAPMT is certainly not suitable** to keep the sensors at low temperatures of many tens of centigrade degrees below zero.
- For the LHCb/RICH Upgrade II, for the Run 5 of the LHC at CERN, **several possibilities are being investigated**.
  A **local cooling** strategy is being investigated first, to cool down a region as small as possible around the sensor only, exploiting the industrial technologies existing today for cooling of solid state devices by many applications.
  Different technologies probably need to be combined, up to an external **cryostat** enclosing (part of) the RICH detector, for a **global cooling** of the RICH detector.

Housing photo-sensors: LHCb/RICH at LHC

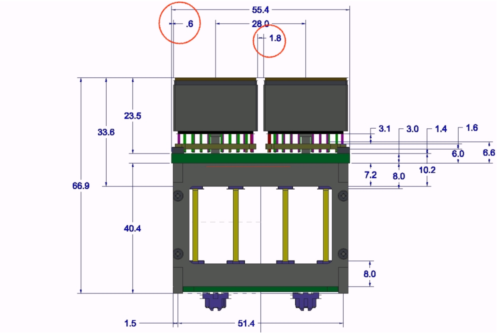
- Main requirements for the photo-sensor housing, regardless of the sensor choice, include the following:
    - structural stability to house and secure in place the sensor, the read-out boards as well as any other ancillary system;
    - **close-packing with large and uniform filling factor** on a large surface
    - **provide electrical connections** from/to the sensors, **thermal dissipation** functionalities for heat transfer to the cooling system and electromagnetic shielding
    - provide support for possible optical components (lenses and/or optical filter) and for components for calibration systems
    - ease of access for repair and maintenance.
- A **modular solution**, based on fully autonomous functional units, is preferred, for ease of construction, maintenance and repair
- In order to save on the required resources and simplify the design, **different functions should be possibly integrated together**.

MaPMT for LHCb/RICH Upgrade I

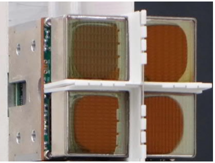
- Modular unit: Elementary Cell (EC) which consists of
  - A Base-Board (BB) with custom sockets to house the MaPMTs. It provides power, common High Voltage (HV) to the photocathodes of the MaPMTs, resistor divider chain(s) which supply potential(s) to the dynodes and connect the MaPMT anodes to the Front-End Boards.
  - Front-End Boards, each equipped with eight CLARO chips.
  - A backboard, which interfaces the FEBs to the Digital Board for configuration and read out.



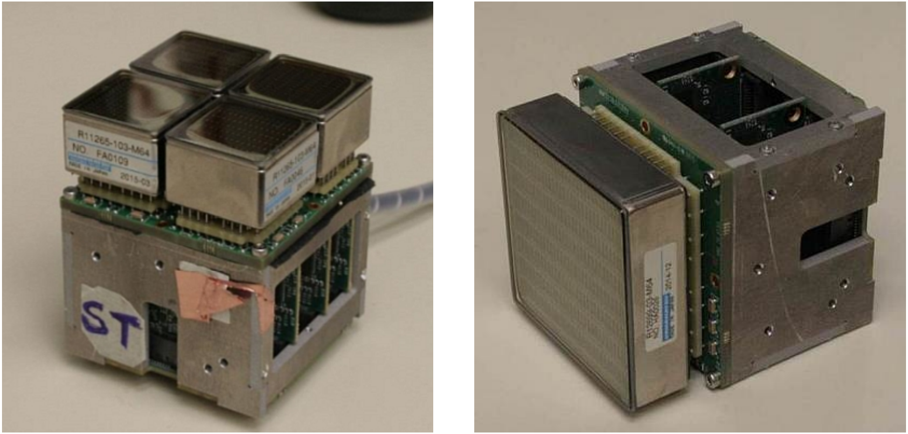
MaPMT for LHCb/RICH Upgrade I 2



Magnetic Shielding is not drawn.



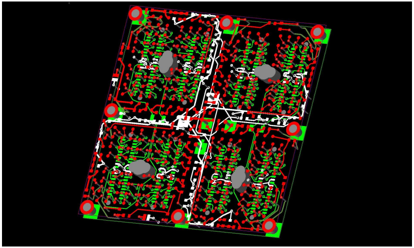
MaPMT for LHCb/RICH Upgrade I 3



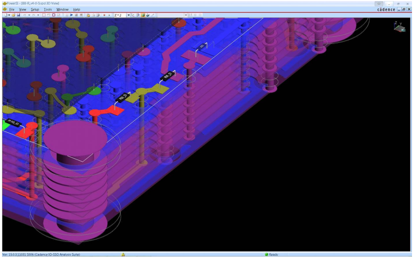
Base-Board Passive Cooling Design

- Base-Board: thick $(3.1\,\mathrm{mm})$ PCB
- Relevant for cooling is the internal structure, designed on purpose.
- Copper layers $(6 \times 0.105\,\mathrm{mm})$ to help heat conduction

The internal structure of the Base-Board: 3D view of the electrical routing.



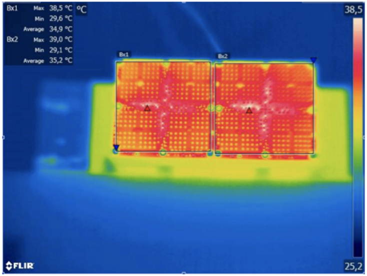
The internal structure of the BB: 3D view of the passive internal copper layer

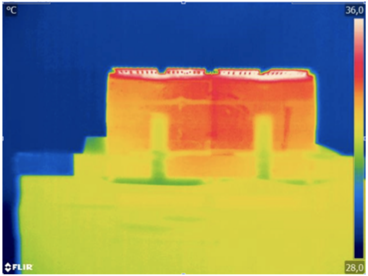


NB: old prototype, not the final routing and thermal layers design.

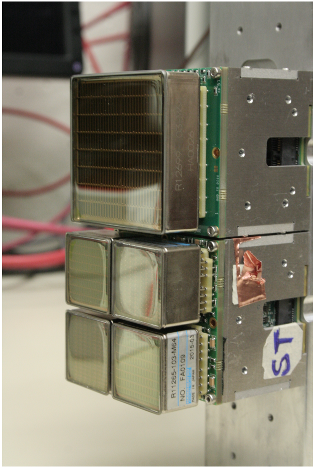
Base-Board Passive Cooling Design 2

- Separated signal and thermal GNDs, the latter thermally connected to the Aluminum case
- 8 metalized holes connected to the case, for mechanical fixing and heat exchange, between the layers and to the case via the screws





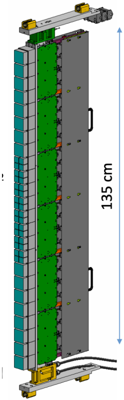
EC-R and EC-H on a cold-bar (prototypes)

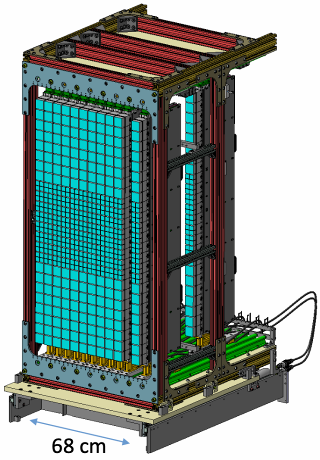


- The ECs are arranged in columns.
- One EC-R and one EC-H are shown on a cold-bar (all prototypes).
- The cold-bar sets a rough thermal reference.
- The design for SiPM might be an evolution of this one, with the thermal reference kept at a low enough temperature and thermally insulated as far as possible.

LHCb/RICH upgrade-I cooling system

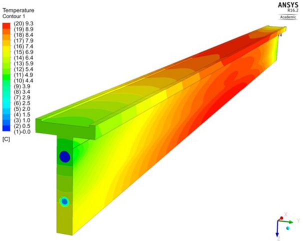
- Columns of EC form the PhotoDetector plane assembly

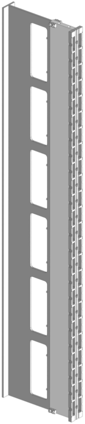


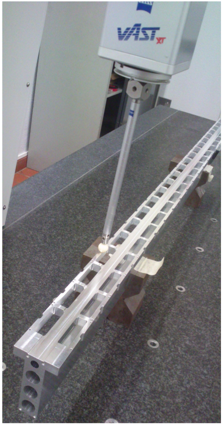


LHCb/RICH upgrade-I cooling system 2

- The structural backbone of the columns is an aluminum T-piece (called cold-bar)
- The EC Aluminum case is connected to the cold-bar which has two ducts for coolant circulation, for effective passive cooling.
- Maximum temperature of the MaPMT: 35° C (to avoid high dark-count rates and degradation of the MaPMT photocathode).

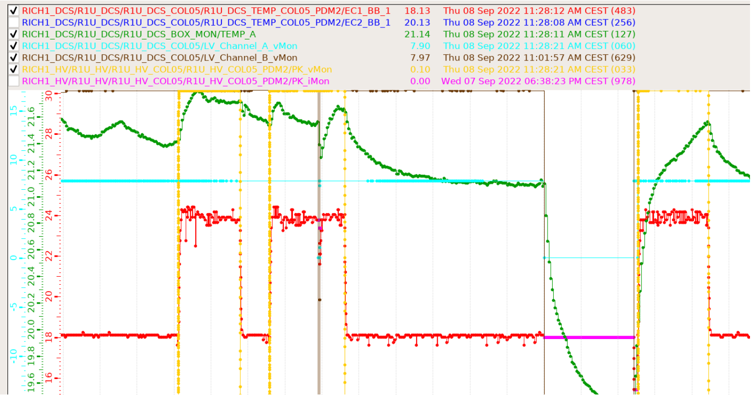






LHCb/RICH upgrade-I cooling system 3

- PT1000 have been integrated on the Base-Board, and readout to monitor the temperature at the Base-Board
- To be done also for SiPM



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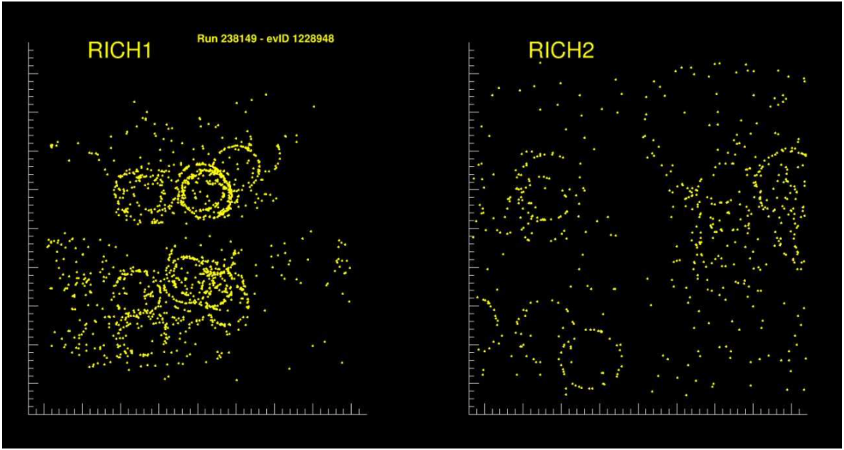
☐	RICH1_DCS/R1U_DCS/R1U_DCS_COL05/R1U_DCS_TEMP_COL05_PDM2/EC2_BB_1	20.13	Thu 08 Sep 2022 11:28:08 AM CEST (256)
☑	RICH1_DCS/R1U_DCS/R1U_DCS_BOX_MON/TEMP_A	21.14	Thu 08 Sep 2022 11:28:11 AM CEST (127)
☑	RICH1_DCS/R1U_DCS/R1U_DCS_COL05/LV_Channel_A_vMon	7.90	Thu 08 Sep 2022 11:28:21 AM CEST (060)
☑	RICH1_DCS/R1U_DCS/R1U_DCS_COL05/LV_Channel_B_vMon	7.97	Thu 08 Sep 2022 11:01:57 AM CEST (629)
☑	RICH1_HV/R1U_HV/R1U_HV_COL05/R1U_HV_COL05_PDM2/PK_vMon	0.10	Thu 08 Sep 2022 11:28:21 AM CEST (033)
☐	RICH1_HV/R1U_HV/R1U_HV_COL05/R1U_HV_COL05_PDM2/PK_iMon	0.00	Wed 07 Sep 2022 06:38:23 PM CEST (978)

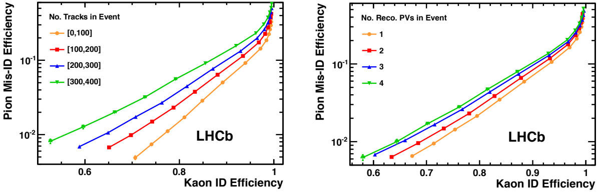
Rings from collisions!



RICH in Upgrade II

- PID capability of charged hadrons fundamental in the LHCb physics program
- PID performance known to be affected by a high detector occupancy

First data from Run1



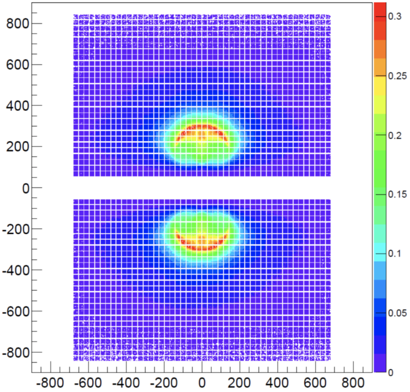
- Goal: Keep/improve the current performance for Upgrade II at the HL-LHC extending also the high-momentum limit

RICH in Upgrade II

- Expected maximum occupancy (in limited regions of RICH1) in 2022: ~ 0.3; known to be manageable from Run-1 and Run-2
- In Upgrade II:
  - far too high occupancy in the detector (in particular in the central region of RICH1): without any change wrt the Upgrade I detector, occupancies in excess of 100% are expected in RICH1
  - relatively large overall Cherenkov resolution

    $\sigma_\theta = \sigma_{\text{focusing}} \oplus \sigma_{\text{chromatic}} \oplus \sigma_{\text{pixelsize}}$

Expected occupancy in RICH1 for Upgrade I



Design strategy for Upgrade II

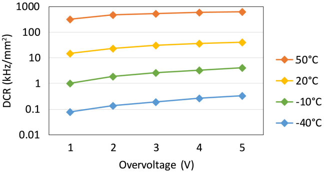
Reduce occupancy	Reduce the angular granularity pixel size and/or focal length. Readout timing information: the first time-resolved RICH New optical design to spread out high-occupancy region
Improve photon yield	Sensors with enhanced PDE and large active area fraction
Improve pixel size uncertainty	Reduce the pixel size
Improve chromatic uncertainty	Sensors with with enhanced red-shifted PDE Choice the gas radiator
Improve focusing uncertainty	Optical design and lightweight optics fabrication technologies
Keep low background/noise	Narrow time bins in readout
Keep low noise	If SiPM: cool it down.

New photo-sensor/photo-detector development

- For the Upgrade II, the MultiAnode-PMT (MaPMT) do not completely fulfill requirements, in particular pixel size ($3\,\mathrm{mm}$) and time resolution ($\sim 200\,\mathrm{ps}$).
- The baseline candidate photosensor for replacement are SiPMs.
- SiPM have the potential to meet all the the requirements after a vigorous R&D program targeted to LHCb/RICH:
  - improving intrinsic radiation hardness $\Longrightarrow$ work in strict contact with industrial partners;
  - enable operating at low enough temperature (plus, possibly, annealing) $\Longrightarrow$study a suitable cooling system.
  - After that: shape the geometry of the design to obtain a large and uniform filling factor for the active areas.
- Need to characterize, improve and design for: correlated noise, time-response, low-temperature, radiation tolerance, light collection system, engineering....
- Synergies among several LHCb/RICH groups to fully characterize SiPM; sinergies outside LHCb are welcome.

SiPM well-known limitations

- High Dark Count rate (DCR) and correlated noise (cross-talk, after pulses, ...)
- DCR depends on temperature, it can be mitigated by cooling



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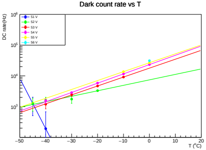
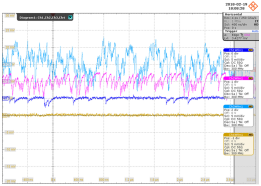
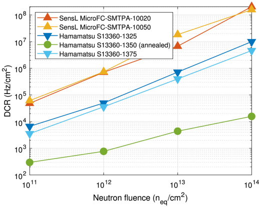


[CERN-THESIS-2021-034.pdf]

- DCR depends heavily on irradiation
- It can be mitigated by cooling and annealing





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SiPM for the LHCb/RICH

- The foreseen measurement of arrival times introduces short bins in time which, adding to the space bins given by pixels, helps a lot with DCR suppression, making DCR less critical.
  See presentation: *A novel fast-timing readout chain for LHCb RICH LS3 enhancements and prototype beam tests*, F.Keizer, this conference.
- In addition, the possibility of reducing radiation levels using neutron shielding around (parts of) the RICH is under investigation, in synergy with other LHCb detectors.
- Moreover, DCR adverse effects can be mitigated by using micro-lensing to reduce the physical SiPM area while keeping the effective pixel size in the range of ≈ 1 mm to avoid too many channels, and reducing sensor capacitance.

Housing for SiPM for LHCb/RICH Upgrade II

- A new housing PCB is needed for integration of SiPM in the current electro-mechanical structure
- Main **challenges**
  - integrate into the Elementary-Cell some sort of **active local cooling** with the other ancillary services.
  - maximize the geometry acceptance of the full PhotoDetector array (filling factor inside every module and among different modules) using optical adapters
  - signal coupling of the SiPM/Base-Board: the Base-Board complexity is driven by the number of channels which increases for larger number of channels because of higher densities, constraints on Front-End Board (FEB), readout chips channels and full readout scheme

LHCb/RICH SiPM Cooling

- The approach used for the housing of the MAPMT proved **very successful**. Therefore, we plan to continue to pursue it, by changing passive into active cooling.
- Strategy of cooling for Upgrade II
  - It depends on the required SiPM temperature
  - Local cooling: to cool down a region as small as possible around the sensor only, providing thermal insulation as close as possible to the sensor, thus minimizing the mass to cool and avoid problems with low temperatures of nearby objects, such as the radiator gases, using multiple cooling stages with several technologies
  - Global cooling: to cool down the full (or a part of if) PhotoDetector Assembly (PDA) into a cryostat
  - A **combination of more techniques**, Local plus Global, will be most likely required.

LHCb/RICH SiPM Cooling Requirements

- Need to cool down both the sensors (SiPM) and the electronics
- Large PhotoDetector Area: 4 planes, $\sim 1\,\mathrm{m}^2/\mathrm{planes}$ each
- Large optical window, $\sim 1\,\mathrm{m}^2$ separating the gas radiator from the PDA Asssembly
- Volume of the PDA: $1.5 \times 0.7 \times 0.5\,\mathrm{m}^3$
- Considering a pixel size of $1\,\mathrm{mm}^2$ (30%) + $9\,\mathrm{mm}^2$ (70%) the estimates number of channels: ~ 400000/plane
- Power estimate for electronics (FastRICH + TDC: $5 \div 10\,\mathrm{mW}$/channel + other components): $\sim 5\,\mathrm{kW}$/plane

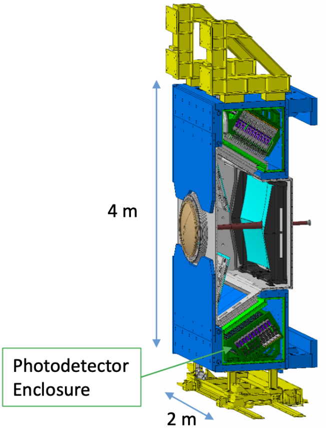
Local cooling concept: new housing

- Cooling of solid state devices is today targeted by many applications, also at the industrial/commercial level.
- Possible technologies include
  - miniaturized active Peltier coolers; but radiation hardness has to be checked;
  - fluid micro-channel cooling technologies
  - miniature cryo-coolers
- Options for similar problems have been studied in LHCb.
- We are in the process to try to figure out the most promising approach and will look for expert advice (we cannot probably test all the possibilities....),
- Any of these technologies are to be integrated as much as possible in the housing or nearby. Cold fingers, capable to extract enough power, need to be placed as close as possible to the housing.

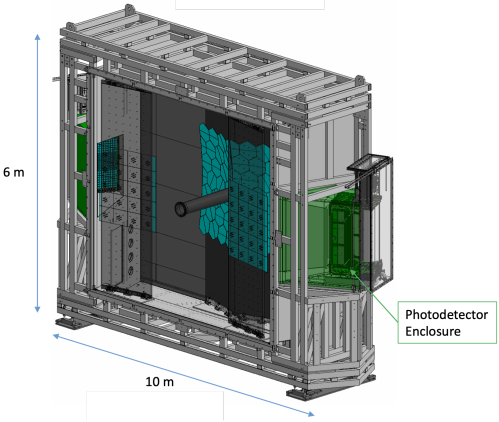
Global Cooling Strategy

- Cryostat including the full (or a part of) PDA

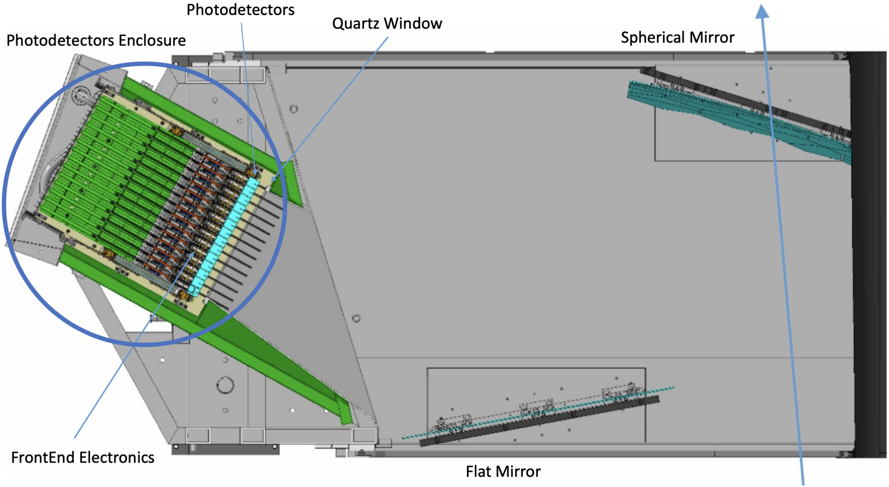
RICH1



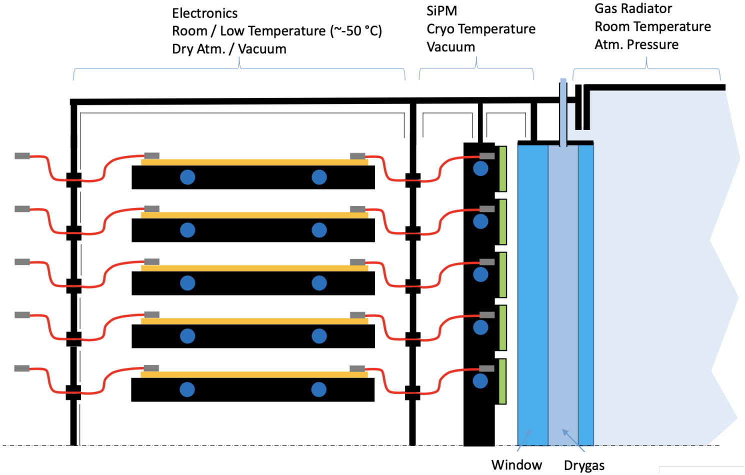
RICH2



Global Cooling Strategy



Global cooling strategy: cryostat



Electronics
Room / Low Temperature (~-50 °C)
Dry Atm. / Vacuum

SiPM
Cryo Temperature
Vacuum

Gas Radiator
Room Temperature
Atm. Pressure

Global cooling strategy: cryostat 2

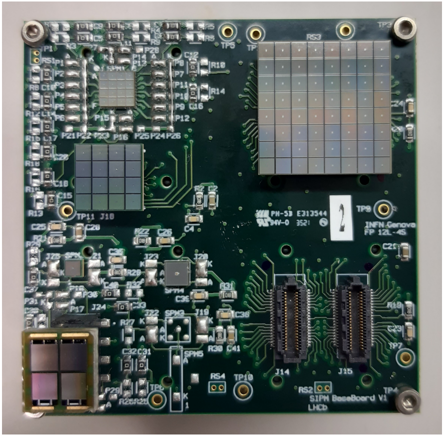
- Critical issues include
  - A large mass to cool and keep cold and thermal leaks.
  - Possible thermal interference among the ambient temperature gas radiator, in order to avoid gas condensation due to the nearby cooled sensors.
  - Quartz windows separate the SiPM region from gas radiator regions. To mitigate the thermal effect on the gas volume is to install two windows separated by vacuum/drygas
- Investigation on the feasibility is on-going.

Development Plan for Local Cooling

- Expert-advised market survey for available technologies.
- Modify the Base-Board to host SiPM instead of MAPMT (done) and test different SiPM (on-going).
- Base-Board with full geometrical acceptance SiPM coverage (in production).
- Thermal cooling measurements (started), and comparison with thermal simulations, aimed at modeling of thermal transfers
- First prototype with integrated cooling design in 2023.
- Details follow.

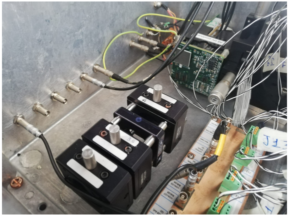
SiPM Evaluation Base-Board

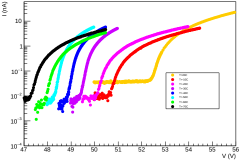
- A first evaluation Base-Board housing SiPM already produced
- Fully compatible with the Upgrade I EC housing
- Housing various SiPM types (including Hamamatsu and FBK SiPM) for test purposes
- Possibility of reading both positive or negative SiPM signals (to be more flexible for the readout electronics)
- Tested successfully both in laboratory and in Autumn 2021/July 2022 testbeam periods

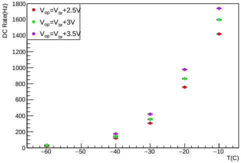


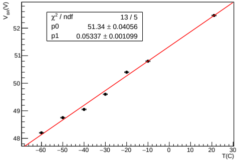
SiPM Base-Board prototypes: test in lab

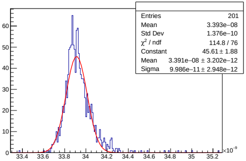
- Fully automatic setup able to measure IV-curves/gain/DC rate/time resolution/... up to 8 channels
- System setup includes a laser with ps pulses, fast pre-amplifiers, a multichannel digitizer, several multimeters, an oscilloscope





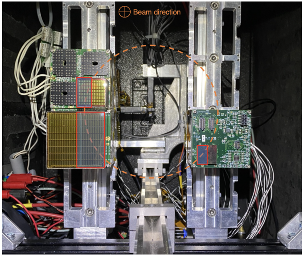


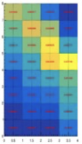


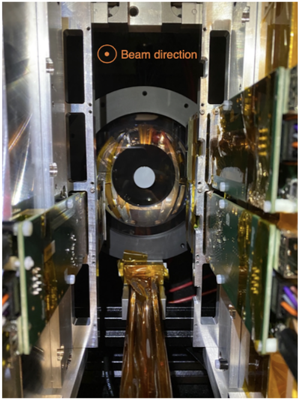


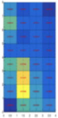
TestBeam with SiPM Base-Board

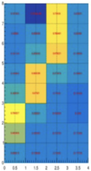
- First test on beam of the opto-electronic chain with fast-timing information using the new SiPM Base-Board [See Floris Keizer's talk]





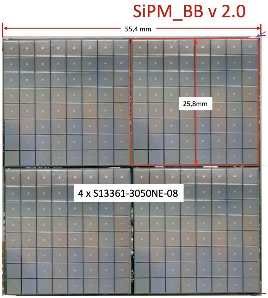


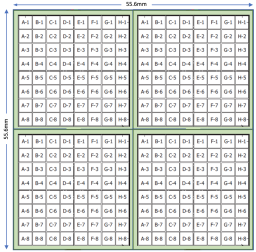




SiPM Base-Board prototype

- A prototype of the Base-Board housing SiPM has been designed and it is currently in production
- It houses 4 SiPM matrices with LGA (Hamamatsu S13361-3050NE-08)
- Main technological challenges:
    - achieved a high fill factor
- It will be tested both in laboratory and in the next testbeam period in one month time (October 2022)





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A-2	B-2	C-2	D-2	E-2	F-2	G-2	H-2	A-2	B-2	C-2	D-2	E-2	F-2	G-2	H-2
A-3	B-3	C-3	D-3	E-3	F-3	G-3	H-3	A-3	B-3	C-3	D-3	E-3	F-3	G-3	H-3
A-4	B-4	C-4	D-4	E-4	F-4	G-4	H-4	A-4	B-4	C-4	D-4	E-4	F-4	G-4	H-4
A-5	B-5	C-5	D-5	E-5	F-5	G-5	H-5	A-5	B-5	C-5	D-5	E-5	F-5	G-5	H-5
A-6	B-6	C-6	D-6	E-6	F-6	G-6	H-6	A-6	B-6	C-6	D-6	E-6	F-6	G-6	H-6
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A-1	B-1	C-1	D-1	E-1	F-1	G-1	H-1	A-1	B-1	C-1	D-1	E-1	F-1	G-1	H-1
A-2	B-2	C-2	D-2	E-2	F-2	G-2	H-2	A-2	B-2	C-2	D-2	E-2	F-2	G-2	H-2
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A-4	B-4	C-4	D-4	E-4	F-4	G-4	H-4	A-4	B-4	C-4	D-4	E-4	F-4	G-4	H-4
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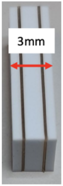
A-8	B-8	C-8	D-8	E-8	F-8	G-8	H-8	A-8	B-8	C-8	D-8	E-8	F-8	G-8	H-8

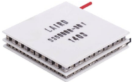
First SiPM BB prototype with active cooling

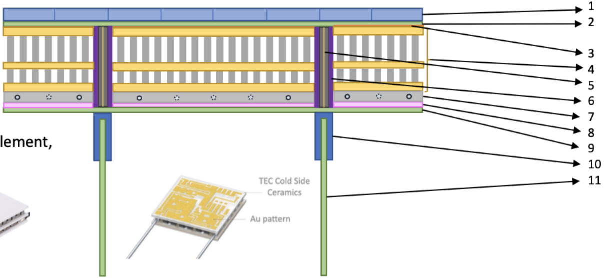
- New version currently under design will include some pioneering prototype for active cooling

#5



#4: Double element, dT max 90°C



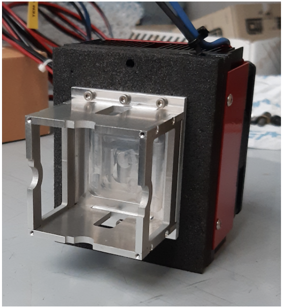


Legend:

1. SiPM matrix (8 x 8 S13361-3050NE-08)
2. SiPM signals fan-out PCB
3. Silicon conductive paste with high thermal conductivity
4. Two Stages Peltier cell (2nd stage with doubled thickness compared to the first, to keep the same useful cold area)
5. Silicon rubber with vertical gold wires (SiPM to FEB fan-out)
6. Silicon rubber holder
7. Metal heatsink with possible liquid cooling
8. Thermal insulator
9. Baseboard PCB
10. Front-End Board connector
11. Fron-End Board

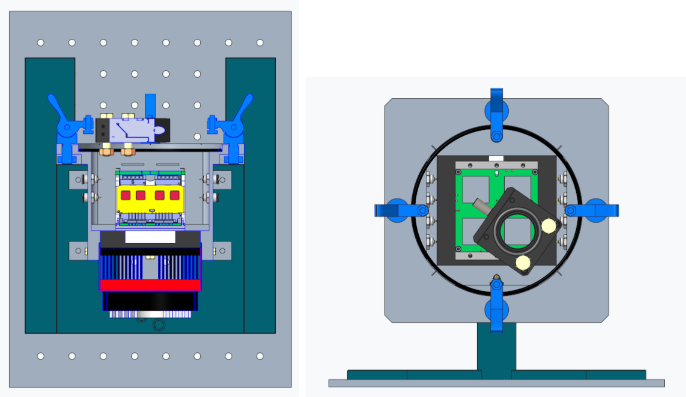
First SiPM Base-Board with active cooling

- Test of a system equipped with Peltier cells on-going to measure the effectiveness of cooling and orient the design
- A direct-to-air thermoelectric cooling assembly equipped with Peltier modules is used



First SiPM Base-Board with active cooling 2

- An enclosure with a transparent quartz window to house the full EC has been designed
- Modified FEBs have been produced to be able to reroute the SiPM signals

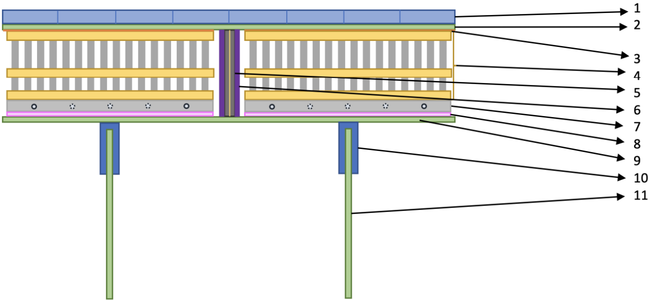


Courtesy of Cecilia Rossi and Antonello Mercenaro, INFN Genova

Conclusions

- Start from the robust design for MAPMT and try to adapt.
- From MAPMT to SiPM: no challenge (with the same pixel size)
- From passive to active cooling: it looks like challenging, whatever strategy, either local or global cooling.
- A SiPM Evaluation Base-Board (without cooling) already produced and tested both in lab and in testbeams
- A SiPM Base-Board prototype currently in production and ready to be tested at the next testbeam in October2022
- Design of a BaseBoard with integrated cooling already developed: to be produced in 2023
- A cryogenic cooling is under study
- A full campaign of tests foreseen in the next months

Spare Slides



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10. Front-End Board connector
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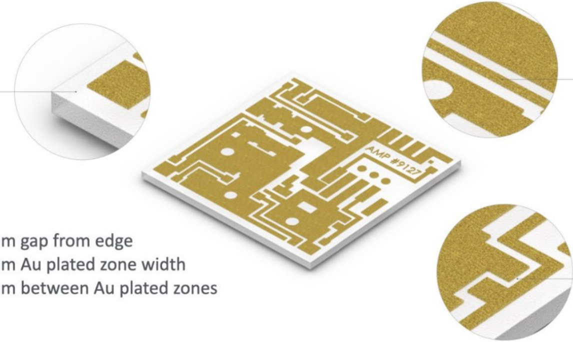
THREE BASIC DESIGN RULES FOR AU PATTERNS

There is a simple rule “3x100um”. The shape and complexity of Au pattern can be any then



Min 100um
gap from edge

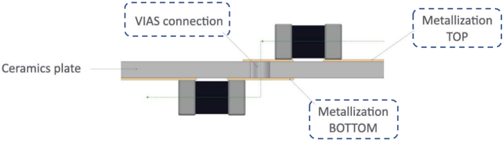
Min 100um
Au zone width

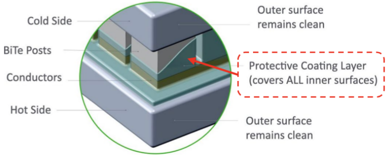
Min 100um
distance between

1. Min 100um gap from edge
2. Min 100um Au plated zone width
3. Min 100um between Au plated zones

Au pattern can be applied to one or both sides of the ceramic substrate.

For application with Dew Point and condensation risks, TEC can be provided with a protective coating





The connection between AU patterns on each side can be created using VIAs

Cooling requirements for Upgrade I - RICH1

Number of circuits (loops):	2
Nominal heat power:	$2 \times 3.45\,\mathrm{kW}$
Max. temperature of the photon detectors:	$< 35\,^\circ\mathrm{C}$
Max. temperature of electronics	$< 50\,^\circ\mathrm{C}$
Coolant:	Fluorinated fluid: 3M Novec$^{\mathrm{TM}}$ 649, 7100 or C_6F_{14}
Heat transfer medium:	Liquid mono-phase
Minimum temperature at the PDA inlet:	$\sim 11\,^\circ\mathrm{C}$
Temperature difference of the coolant (PDA outlet), ΔT:	$5\,^\circ\mathrm{C}$
Maximum pressure at the PDA inlet:	$< 2\,\mathrm{bar}$
Pressure drop in the PDA:	$\sim 0.7\,\mathrm{bar}$
Leak rate, in total:	$< 0.05\,\mathrm{l/day}$
Typical flow of the coolant:	$1750\,\mathrm{l/h}$

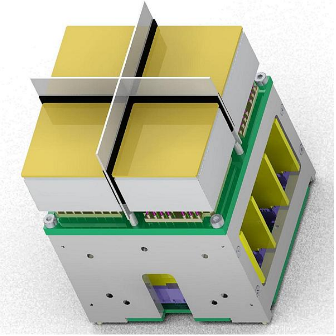
Component	Power
Digital Boards, LV (7 V, 3.4 A):	6 kW
Front-end ASIC Boards (0.128 W/board)	250 W
The high voltage divider boards	650 W
Total power per Column	311 W
Total power	6.9 kW

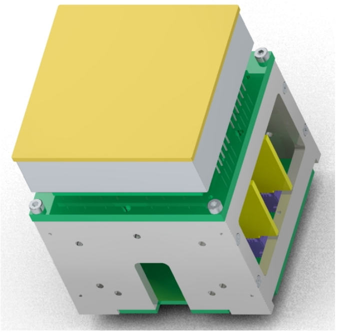
Cooling requirements for Upgrade I - RICH2

Number of circuits (loops):	2
Nominal heat power:	$2 \times 2.1\,\mathrm{kW}$
Max. temperature of the photon detectors:	$< 35\,^{\circ}\mathrm{C}$
Max. temperature of electronics	$< 50\,^{\circ}\mathrm{C}$
Coolant (Fluorinated fluid) [9]:	3M Novec$^{\mathrm{TM}}$ 649, 7100 or C_6F_{14}
Heat transfer medium:	Liquid mono-phase
Minimum temperature at the PDA inlet:	$\sim 11\,^{\circ}\mathrm{C}$
Temperature difference of the coolant (PDA), $\Delta T_{inlet-outlet}$:	$5\,^{\circ}\mathrm{C}$
Maximum pressure at the PDA inlet:	$< 2\,\mathrm{bar}$
Pressure drop in the PDA:	$\sim 0.7\,\mathrm{bar}$
Leak rate, in total:	$< 0.05\,\mathrm{l/day}$
Typical flow of the coolant:	$1060\,\mathrm{l/h}$

Component	Power
Digital Boards, LV (7 V, 3.4 A):	3.6 kW
Front-end ASIC Boards (0.128 W/board)	150 W
The high voltage divider boards	650 W
Total power per Column	175 W
Total power	4.2 kW

MaPMT for LHCb/RICH Upgrade I

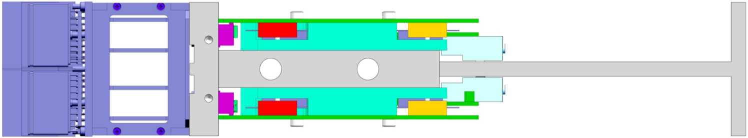


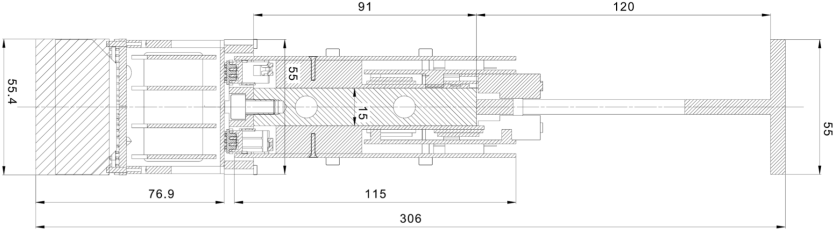


MaPMT for LHCb/RICH Upgrade I

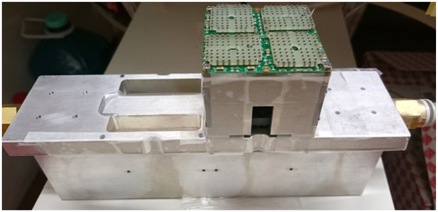
Bare Aluminium (Alu) case

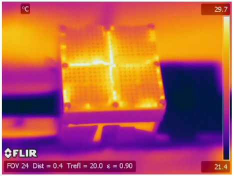
LHCb/RICH upgrade-I cooling system

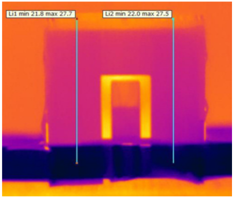


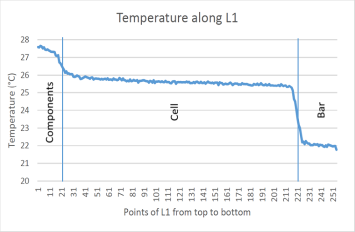


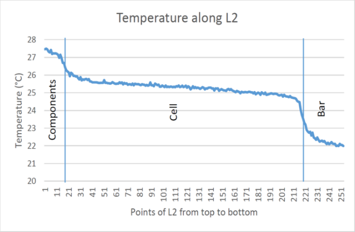
LHCb/RICH upgrade-I cooling system











Detector Design for Upgrade II

- Main requirements
  - Single-photon Cherenkov angle uncertainty $\sigma \lesssim 0.4/0.2\,\mathrm{mrad}$ (RICH1/RICH2)
    a factor 2 better than expected for Run3
  - Number of detected photons per saturated track: $\gtrsim$ 40/30 (RICH1/RICH2)
  - Maximum signal occupancy ≈ 0.2 (space and time bins)
  - Signal/noise ratio: average Dark Count Rate occupancy ≈ 0.001 (space and time bins); plus cross-talk, after-pulse.....
  - Provide the system with timing capabilities (event gating and photon ToD)
  - Active area fraction: $\gtrsim$ 0.8.
  - Integrate the detector with its own system for monitoring and calibration, to improve the systematic uncertainties.
  - Plus, of course, many other requirements: recovery time, robustness to magnetic fields (could remove magnetic shield in RICH1 freeing space), feasibility of large-area implementation, uniformity, stability, rad-hardness, ageing, cooling, bandwidth limit, greenify whatever possible......

Detector Design for Upgrade II 2

- All this require and translates into the following sub-systems requirements.
  - New optical design.
  - New photo-sensors.
  - New readout for a time-resolved RICH.
  - New calibration/monitoring system with sub-ns precision
    and relative/absolute detector efficiency online measurement/calibration.
  - New radiator gases? TBD.
  - Aerogel? TBD.
    See presentation: *Study of new aerogel radiators for the LHCb RICH upgrade*, A. Lozar, this conference.