RAS Working Group meeting 18.11.2021

Participants: A. Apollonio, A. Asko, D. Barrientos, M. Barros Marin, P. Bell, R. Berberat, H. Boukabache, M. Brucoli, C. Cala Franco, E. Calvo Giraldo, N. Chatzigeorgiou, A. Coronetti, G. Daniluk, S. Danzeca, J. Emery, L. Felsberger, B. Fernandez Adiego, E. Fortescue-Beck, G. Foucard, T. Gingold, P. Gkountoumis, J. L. Gomez Costa, E. Gousiou, R. K. Grimmer, G. Iadarola, P. Jurcso, S. Kaufmann, I. Kozsar, M. Krupa, T. Ladzinski, M. Lipinski, I. Lopez, N. Magnin, C. Martinez, K. J. Motala, S. Ramberger, V. Schramm, J. Serrano, J. Spasic, L. Strobino, B. Todd, N. Trikoupis, S. Uznanski, E. Van der Bij, P. Van Trappen, W. Viganò, N. Voumard

The slides are available on Indico:

https://indico.cern.ch/event/1096112/

The meeting has been organised as a joint meeting between the Electronics Community Forum and the RASWG of the ATS sector. Two presentations were given:

Documentation Set for Industrial Production - Speaker: P. Bell

P. Bell presented necessary documentation for the production of PCBs and PCB assemblies, a, in his words, important topic which often times is not prepared correctly, therefore important to discuss. Throughout the whole process the documentation should be complete and accurate, as well as kept up-to-date. Missing details may cause problems in the process and lead to not receiving a reasonable quote. Furthermore, this may affect the quality and reliability of the production.

The design office provides a set of documents for a generic specification establishing a link between the EDA files specific to the individual design and the application of industrial manufacturing standards (see slide 4). Three main services are provided for electronics production: the design office, the prototyping workshop and an outsourcing service.

Three major steps describe the production process (see slide 5). The Bare PCB manufacturing produces generally the most expensive single component. Therefore, it is important to provide comprehensive documentation at this point. P. Bell pointed out that it is the better approach to have all documentation in one file which can be split into two categories (see slide 8). He outlines that a human readable summary should be available to enable the design office to quickly review the design. EDA templates for PCB production are provided by the design office (see slide 9). P. Bell points out that the specification template forms the basis of the contract. It doesn't define details, but defines which processes are used and what is to be considered for manufacturing. He furthermore recommends to avoid specifying the optional

_stack-up.pdf if this is not needed. For stack-up files a software of Polar Instruments is used (see slide 12), since contracted manufacturers also use this software which avoids complications. Furthermore, this facilitates to require and keep design changes made by the manufacturer at CERN. This prevents any manufacturer from having an advantage and enables CERN to use the complete files for future tenders.

Regarding quality and acceptance, P. Bell recommends to specify necessary controls in detail. In industry, for instance, a electrical test is standard but if not specified it will not be performed by the manufacturer. This is especially important for the PCB being the single most expensive component in the production.

For the PCB assembly as the next step, P. Bell outlines that the documentation set should be comprised of two kinds of files, human readable ones and the CAD files.

Finally, P. Bell reiterated the recommendation to provide a thorough documentation already at the beginning of the process to receive an accurate quote and better costs. He also underlines that such documentation should be consistent throughout different designs. A designer should try to avoid pushing boundaries in the design and manufacturing specifications, i.e. to not over-specify and to avoid going close to the limits. Related design practices are for example Design for Manufacturing or Design for Sourcing, often summarised under the umbrella of Design for Excellence (DfX), see slide 2. One should also make sure that the used contractors are aware of the required industry standards.

Slide 25 provides a link to the design office twiki pages for standard libraries and their FAQ:

- https://twiki.cern.ch/twiki/bin/view/Electronic%20Modules/ComponentLibraries
- https://twiki.cern.ch/twiki/bin/view/ElectronicModules/WebHome

Questions and Discussion after the Presentation:

E. Gousiou asked what could be done by the designer before consulting the design office to ease the work. P. Bell replied to follow the presented strategy. What can be done as a starting point is to use the CERN libraries (see link above) and send new components if they are missing to the centralised service in order to add those to the libraries. This enables the design office to perform a Design Rule Check and check the design by using internal scripts which require the design to fit to the standardised libraries. As a second aspect, P. Bell points out to not over-specify, for example should “controlled impedances” only be requested if it is actually necessary for the functioning of the design. Such a request may change the way the PCB is manufactured and may lead to compromising other areas of the manufacturing process (quality) which should be addressed early. It is also helpful to design schematics each time in a similar way if possible.

B. Todd asked if there is a way to test a design also non-destructive. P. Bell replied that the microsectioning using test coupons is essentially non-destructive, because the

manufacturer produces an extra area of the PCB which is to be cut off to verify the whole process. The coupon uses exactly the same materials and manufacturing processes as the PCB to verify those. It is also placed on the edges where potential defects should in generally be the most extreme. In addition to this it is also possible to include an additional trace impedance test there using a standardised coupon with designated test pads. Manufacturers can use a test probe from Polar Instruments to get a nominal value for a representative trace on a coupon for each panel. This can be delivered in a report.

W. Viganò asked about potential consequences if a design has been sent to the design office with all documentation guidelines followed and a produced PCB assembly is received which passed a functional test, but after some time for instance during a thermal cycling test defects such as a delamination of the PCB may be discovered. He therefore asks how many days one would have to report and claim this defect to the manufacturer. P. Bell answers that for such a case it is good to have good manufacturer relations. For the specific case the initial step would be to check the manufactured test coupon. This could be used to account the sub-contractor and prove whether this defect has been present before. Then it is to be checked who is responsible and what are the contractual issues. In general, this is a matter of negotiation then. W. Viganò raised the additional point of who would pay for the components then which need to be purchased again. P. Bell also answered here that this would be a negotiation issue which may depend on the manufacturer relationship. It would depend a lot on whether CERN, as well as the manufacturer, would work together on future projects.
Edit P. Bell: BE-CEM-EPR agreements with manufacturers require this. It is not by default but it’s possible to make them responsible for complete damages if agreed in advance.

E. Calvo Giraldo commented that with the end of production a board may still change by any future design stage. Therefore, the documentation is not finished at this point. She asks how to handle any documentation which is created during the following life cycle phases and how this can be added to the initial documentation set. Another question is about the fields to be filled in the templates. In her experience these fields are often left empty. She asks if there is any recommendation or guideline how they should be filled. P. Bell replies that for now the EDA archives only contain the designs. For instance, there is nothing to include testing files. He points however to EDMS where multiple parent documents can be added or a link to the EDA archive can be created within for instance a testing directory. This would work without moving the files to other locations. E. van der Bij adds that it was originally foreseen to add one empty document to the EDA archive. This is the specification file which can be freely used by the user. E. Calvo Giraldo adds that it would be very useful if there would be some kind of recommendation for people how to do it. Especially since there are many different ways of doing this. P. Bell agreed and said that this is a good point to further discuss in the future.

S. Uznanski commented that many struggle with documentation. He thanks the design office that they take care of a big part of this documentation and points to the used pyramid (see slide 24) as a really good approach. He asks if the documentation may

be made more lightweight, for example whether some data or standards can be linked. P. Bell highlights that for this it is nevertheless important to think of both the human readable side of the files and the detailed files to which S. Uznanski agreed, that it is often a problem for operating systems that they do lack documentation and that designers are not at CERN anymore.

Discussion on the Electronics Design Dependability Checklist – Speaker/Moderator: B. Todd

B. Todd presented a checklist (see indico page) for dependable electronics design prepared in 2019 together with W. Viganò and several others working on reliable electronics. The main part of this checklist is a single page which contains a total of 44 questions a designer may or should ask themselves for designing electronics not only to "work" but also to achieve a higher reliability product – focusing on dependability aspects. These questions are divided in the five categories: System Level, Board Level, Electronics – Schematic & Printed Board, Bill of Materials, Test, and Maintenance. Furthermore a 3-tier-scheme is used classifying the single aspects in 'required', 'strongly advised', and 'advised'. Today's discussion is meant to be a kickoff for future discussions and the improvement of the checklist, moreover a potential merging with other existing checklists being managed by the electronics forum. The goal would be to augment any design review guidelines from the electronics forum with the pertinent questions regarding dependable design; not to create two (or more) separate sets of lists.

S. Uznanski agreed, commenting that such checklists have started to be discussed. The goal is to gather the different checklists and to work towards a single or maybe multiple linked documents. There will be a small working group with E. van der Bij, P. Bell, E. Gousiou and himself to work towards this. When doing so this working group will reach out to the RASWG. B. Todd agreed that such an effort is necessary, it would be very useful to establish such synergies between the Electronics Community Forum and the RASWG.
S. Uznanski also added that such a checklist strongly depends on the individual system and application. Some may require thorough design checks while for instance a monitoring system may not require to follow strictest guidelines. B. Todd replied that this describes a risk-based approach, which is one of the core skills of the RASWG. A. Apollonio added that there should be a document which defines the criticality of individual systems, driving the level of integrity a system needs.
P. Bell added that he strongly supports the checklist approach, because most problems experienced generally come from something that is forgotten during the entire process. B. Todd agreed and W. Viganò furthermore added that the goal of creating the presented checklist was to keep it as simple as possible to have something user-friendly and lightweight.

E. van der Bij asked if it may be a way of making people aware by showing them types of mistakes that have been made in the past. For example to show what has happened when capacitors have not been derated properly, to show near or real misses and their

consequences. B. Todd said that this is a very important point and added that there is or may be some reluctance to show our failures. What can already be done, and would be low cost, would be to consider change notes of designs.

J. Serrano posted into the chat that tools should also be shared, also posting a link to an existing script of C. Gentsos which takes the netlist of designs and allows to extract voltages applied on capacitors and to compare these to the rated values: https://ohwr.org/project/ed/wikis/Capacitor-voltage-rating-analysis-script
this can be used to identify capacitors in the design that are not properly derated.