Documentation for Production PCBs and Assembly

P. Bell, R. Berberat, S. Kaufmann

Quality & Reliability Start with Documentation

- Clear and concise
- Complete, include all information
- Up-to-date

Part of DfX: Design for Excellence

- Design for Manufacture
- Design for Reliability
- Design for Sourcing

Goals

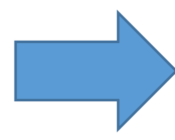
Target	Approach
Accurate quotation	• Human readable summary • Easy to read and digest • Highlight key process-defining features
Within specification	• Referring to industrial standards • Proper tolerances
Acceptable quality	• Quality controls and reports clearly defined
Minimum cost	• Easy quoting reduces margin
Retain intellectual property	• Don’t allow changes which are not reflected in the design

Three Layers

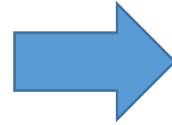
Design

Generic Specification

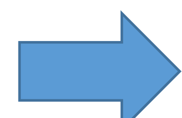
Industry Standards



EDA or design files

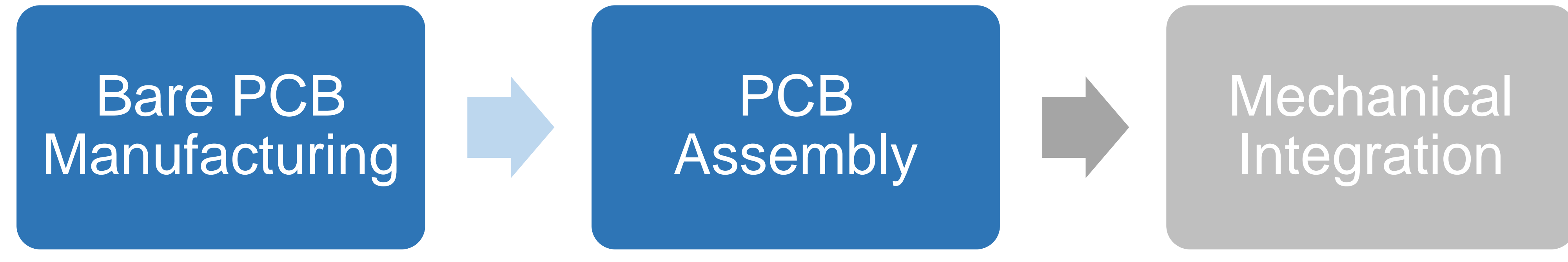


Standard documents, generic for all designs



- IPC-2221A
- IPC-6011, IPC-A-600
- IPC-A-610, J-STD-001
- etc

Three Major Steps



Bare PCB Manufacturing

Bare PCB Manufacturing

The PCB is the most critical single component in an assembly

→If the PCB fails, **the entire assembly will be scrapped**.

Traditionally:

- Engineering drawings, sent as Gerbers + drill file.
- Often including any notes as “fab notes”, directly on the drawings.
- PDF of Gerbers if you’re friendly.

Broadly classified into two categories

Specification

- Human readable summary
- Standardised template
- Refers to IPC
- Easy quoting
- Highlight unique features

Production Files

- Engineering Drawings
- Detailed fab notes
- Gerber files
- Drill file

EDA Template

Specification

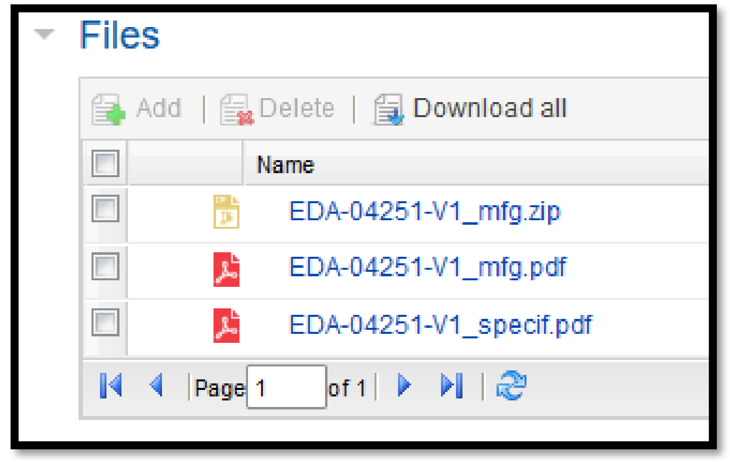
- *_specif.pdf*, summary specification

Optional:

- *_stack-up.pdf* (only when relevant)

Production Files

- *_mfg.zip,* CAD files (Gerbers + drill) for programming machines
- *_mfg.pdf*, human readable PDF of Gerbers + drill file



Specification (*_specif.pdf, _stack-up.pdf*)

Forms the basis of the contract

- Board dimensions, final thickness, number of layers
- Surface finish (default to ENIG)
- Minimum hole size
- Controlled impedances (yes/no)
- Press-fit components (yes/no)
- Filled and capped vias (yes/no)
- etc

- Standard template for IPC requirements, packaging requirements, quality reports, halogen free base material (CERN directive IS41), etc

Specification

Design Office

FIQ51-1

TE/MPE/EM Electronic Modules

PCB Fabrication Specification

Designation

Number	
Title	*Date:* 26-Nov-2018
Customer	
Contact electronics-design-office@cern.ch	*Etude/Design:* P. Vulliez

PCB should be manufactured with Panasonic Megtron-6

Mechanical Description

External Size (mm):	280.0mm x 322.3mm	Thickness [mm]:	2.45
PCB type :	Multilayers 22 Layers	Panel:	NO

Finished Copper Thicknesses Requirements

External Layers [μm]:	50μ	Internal Layers - Planes [μm]:	17.5/70u
Holes Walls [μm]:	25μ	Internal Layers - Signals [μm]:	17.5μ

Board Finish Requirements

Silkscreen On Top:	YES	Silkscreen On Bottom:	YES
Silkscreen Colour:	White		
Soldermask On Top:	YES	Soldermask On Bottom:	YES
Soldermask Colour:	Green		

Surface Finish: ENIG - Electroless Nickel/Immersion Gold according to **IPC-4552**

Thicknesses: **Ni: 3μm min - 6μm max / Au: 0.05μm min - 0.125μm max**

Additional Information

Minimun Track Width:	0.090mm	Minimum Track/Pad Clearance:	0.085mm
Minimum Hole Diameter:	0.25mm	Wedge Aluminium Wire Bonding:	NO
Buried Holes:	NO	Blind Holes:	YES
		Filled and Capped Vias:	YES **/*
Press-Fit Through Holes:	YES	Card Edge Connector:	NO
Specified Stackup:	YES *	Controlled Impedance:	YES *
Electrical Test:	YES	Test Coupons Required:	YES

* = Voir/See http://edms.cern.ch/nav/EDA-03452-V3-0 -> Manufacturing -> EDA-03452-V3_mfg.pdf

Laminate And Copper Foils Requirements

Base material, when used, shall be flame retardant rated **UL 94V-0** laminate glass fiber epoxy and conform to L94 according to **IPC-4101/128** , halogen-free. Copper shall be **type H** with pits and dent, **class B**. When procuring base material the following are required: minimum **TG 150°C**, minimum **TD(5%) 350°C**, minimum **T-288 35min**, maximum Z-axis thermal expansion coefficient above **TG 280PPM/°C** (alternatively Z-axis thermal expansion coefficient between 50-260°C of **3.5%** maximum is acceptable).

Prepreg material shall conform to P94 according to **IPC-4101/128**, halogen-free and be subjected to the same requirement set forth for the laminate base material.

All internal layer copper foils shall conform to **IPC-4562/3 CU-E3, class 2**

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Design Office

FIQ51-1

TE/MPE/EM Electronic Modules

Additional Plating Requirements

Finished external layers and plated through holes plating shall be **25μm**.
The copper plating shall be performed with plating chemistries/processes commensurate with the maximum aspect ratio plated hole in the board. The aspect ratio is defined as the ratio of the board thickness divided by the smallest drilled hole diameter on the board.

The quality of the copper plating shall be verified according to **IPC-TM-650**, **2.4.18.1** as to tensile strength and according to **IPC-TM-650, 2.4.2.1** as to ductility.

Thieving may be added outside the circuit board border to compensate for high density areas on the board. For thieving within the borders of the circuit board approval is required.

Vias/Through Holes Requirements

Non functional lands shall not be removed on layers 1, 2, 3, N-2, N-1 and N. Other non functional lands may be removed as long as no removal on adjacent layers occurs.

Negative etchback is not allowed. Positive etchback is permissible to 0.2mils maximum.

All holes are located on the basic modular grid system. All holes shall be located within a 3-mils-diameter of true position. Drilling should be according to **IPC-DR-572**.

Via holes are specified as to drilled hole size ; for these holes the finished hole size is for reference only Holes receiving component leads or pins are specified as to finished hole size.
** Holes Cap plating shall be in accordance to **IPC6012C-3.6.2.11.2** Fig 3.16 and table 3-10 Class 3: Copper thickness min 12μ. Dimples over resin filling max 50μ. Bumps/protrusion over resin filling max 50μ.

Additional Board Finish Requirements

Solder mask over bare copper according to **IPC-SM-840**, class H. All fiducials, lands and holes, except vias, shall be free of solder mask material.

Silkscreen shall be with permanent, organic, non-conductive and RoHS compliant ink. Silkscreen ink must be capable to withstand peak temperatures of 260-270°C for a duration of 60 seconds and at least 3-4 cycles without discoloration.

An identification marking shall be applied on the PCB. It shall contain the PCB manufacturer logo, UL marking, date-code and surface finish according to **J-STD-609**. Marking shall be applied on silkscreen and located in the indicated area near the TE/MPE logo.

Additional Quality Control Requirements

The printed wiring board, and test coupon when used in lieu of a production board, shall be according to **IPC-2221 and IPC-2222, type 3, class2**. Date code and PCB manufacturer logo shall be present on test coupons for traceability.

Acceptance of finished printed boards shall be in accordance with **IPC-A-600, class 3**.

Fabrication and inspection shall be according to **IPC-6011 and IPC-6012, class 3**.

The maximum allowable bow and twist shall be **0.75%**.

All quality controls shall be performed per **IPC-TM-650** procedures and per **IPC-4552**.

Packing Requirements

Boards shall be wrapped in sulfur-free neutral PH wrapping paper and shipped in vacuum-sealed anti-static bags.

A humidity indicator and desiccant may be inserted in the bags.

Quality Documentation To Be Delivered

A certificate of conformity shall be delivered with the PCB's. It shall declare all material used (laminate exact type, soldermask, silkscreen, etc) and their respective lot numbers.

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Stack-Up (with impedance simulation)

S:\billerea\EDA V1-0\worklib\top\physical\EDA- V1_stackup.sci   Units: Millimetres

Polar

Layer	Stack up	Supplier	Supplier Description	Description	Type	Processed Thickness	εr	Copper Layer Type
						0.020	4.000	
1						0.035		Signal
						0.100	4.300	
2						0.035		Plane
						0.400	4.300	
3						0.035		Mixed
						0.400	4.300	
4						0.035		Plane
						0.400	4.300	
5						0.035		Plane
						0.100	4.300	
6						0.035		Signal
						0.020	4.000	

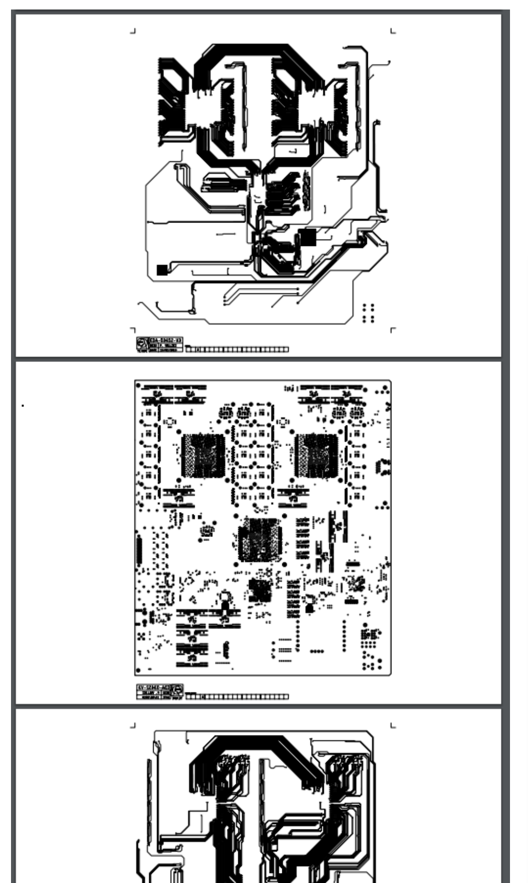
1.60 +0.16 / -0.16

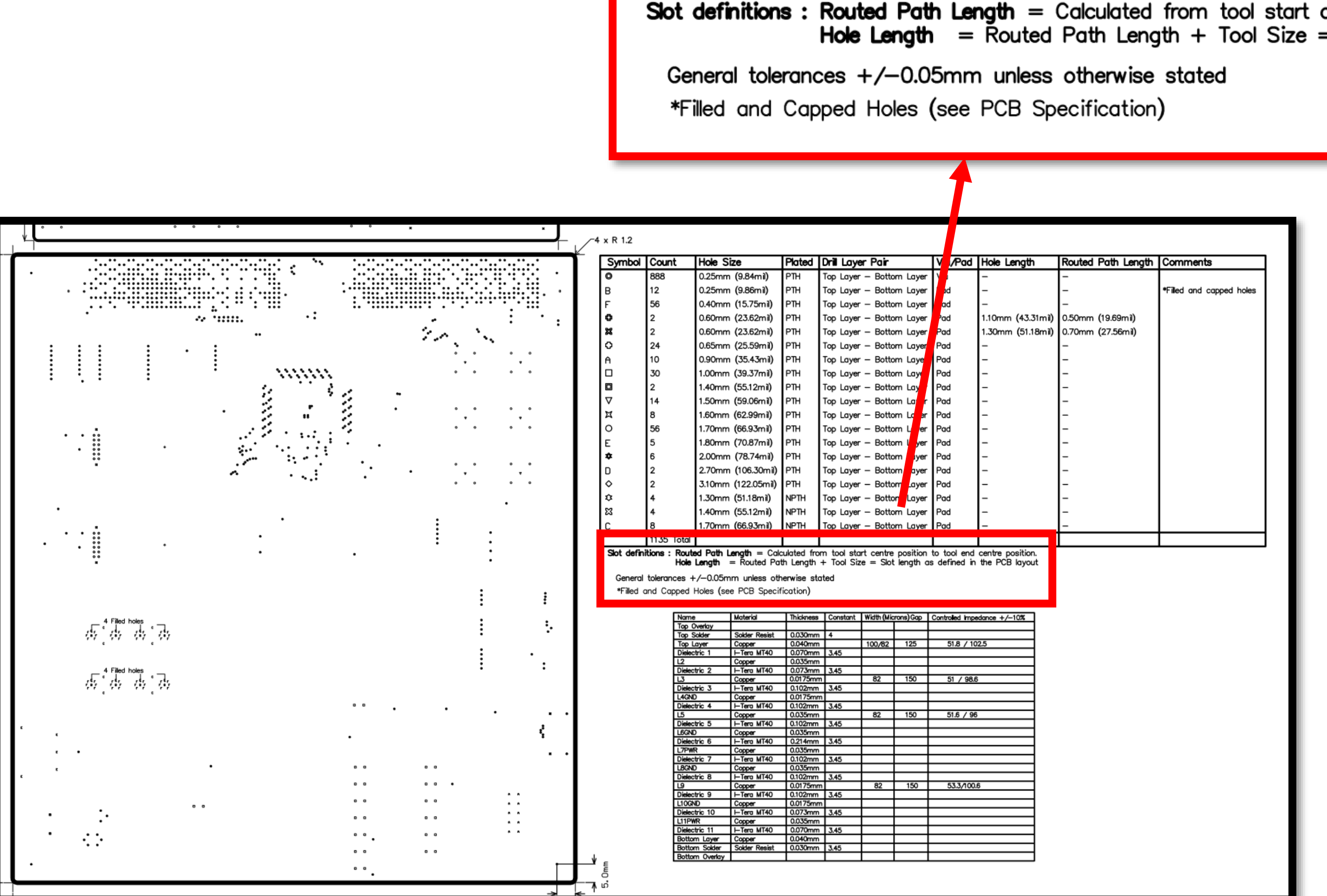
Structure Image	Impedance ID	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Calculated Impedance	Target Impedance	Tol (+/-%)	Ground Strip Separation (D1)	CI Notes-1
	1	Coated Microstrip 1B	1	2	0	0.150	0.150	0.000	50.070	50.000	10.000	0.000	
	2	Edge Coupled Coated Microstrip 1B	1	2	0	0.100	0.100	0.150	100.650	100.000	10.000	0.000	
	3	Offset Coplanar Waveguide 1B1A	3	2	4	0.100	0.100	0.000	75.710	75.000	10.000	1.000	short 75 ohms lines on TOP layer are not achievable. validated at ~61ohms. D1 is 1mm to avoid impact on the lines
	4	Offset Coplanar Waveguide 1B1A	3	2	4	0.330	0.330	0.000	49.510	50.000	10.000	1.000	D1 is 1mm to avoid impact on the lines
	5	Coated Microstrip 1B	6	5	0	0.150	0.150	0.000	50.070	50.000	10.000	0.000	
	6	Edge Coupled Coated Microstrip 1B	6	5	0	0.100	0.100	0.150	100.650	100.000	10.000	0.000	

Manufacturing (*_mfg.pdf, _mfg.zip*)

- PDF print of engineering drawings
- Includes all layers: copper, mask, silk, paste, drill, panelisation
- Specific fab notes
  - Only to give detail on points already included in Specification!
- Stack-up table again in fab notes if relevant.

Manufacturing Drawings





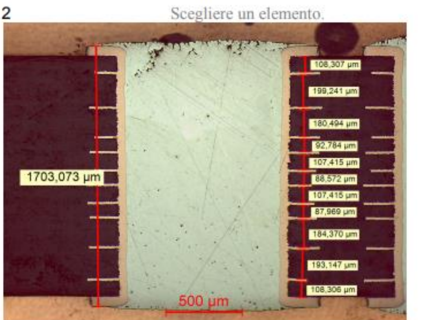
Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

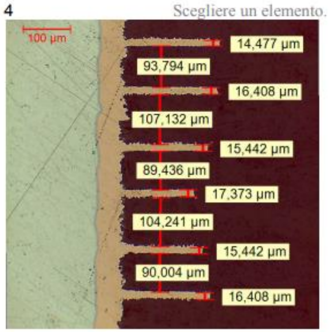
General tolerances +/−0.05mm unless otherwise stated

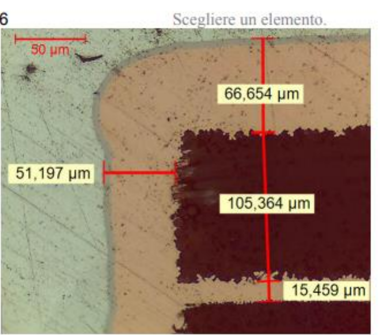
*Filled and Capped Holes (see PCB Specification)

Quality and Acceptance

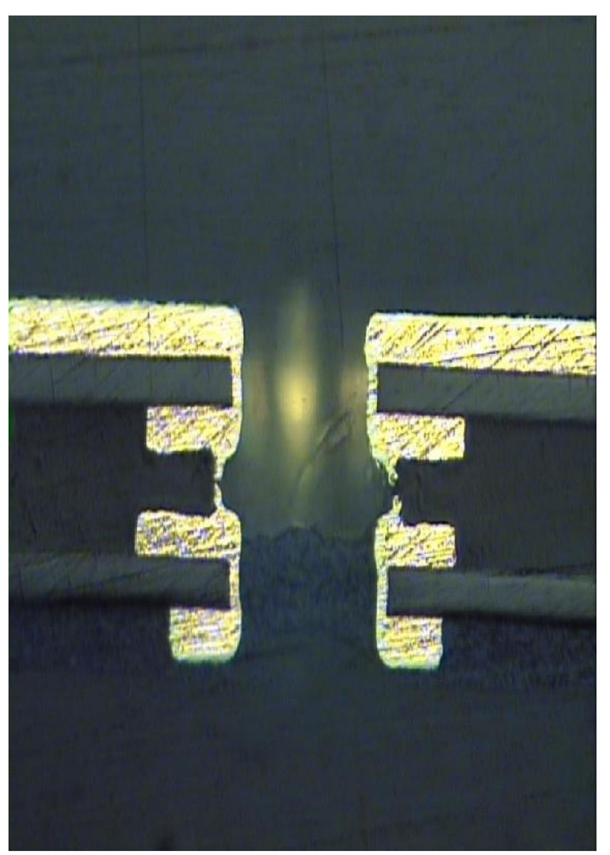
- Electrical test (flying probe)
- Micro-section report
- Test coupons (if >2 layers)
- Impedance control if relevant (coupons + test report)

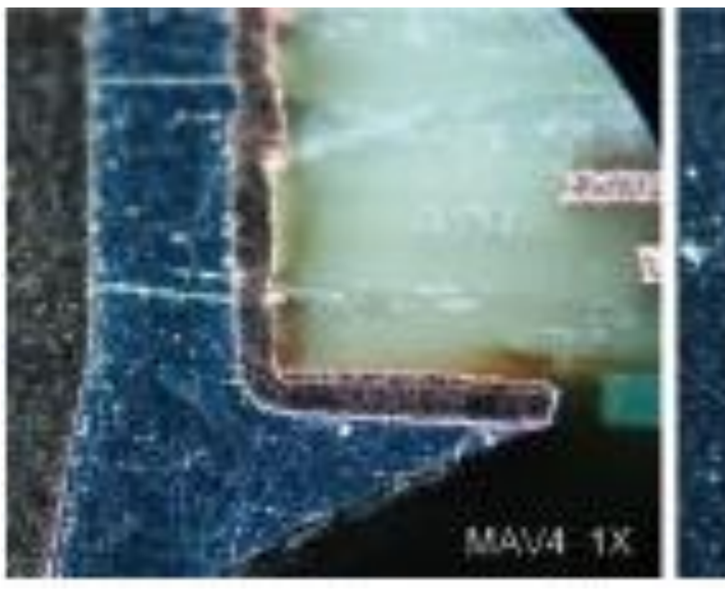


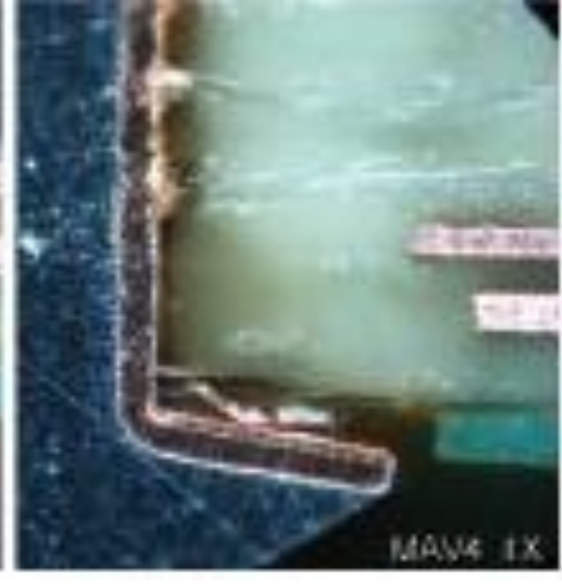




What can go wrong…







PCB Assembly

Design Specific Documentation

Human Readable

- Bill of Materials (BoM)
- Colour plans
- Clearly show process steps: SMT top, SMT bot, THT top, post assembly, etc.

Machine Files

- Solder paste stencil
- SMT pick & place (top/bot)

Optional:

- ASCII CAD or ODB++
- AOI

Bill of Materials (BoM)

Controls Electronics & Mechatronics

EDA-04443-V1-0

(Les composants doivent etre fournis ROHS autant que possible) **Liste de matériel / Material List** (Parts must be supplied ROHS as much as possible)

CERN			
Client/Customer:		Through pins:	49
DATE:		SMD pins on TOP:	810
Dessinateur/Drawn by:		SMD pins on BOTTOM:	122
BE/CEM/EPR	Board dimensions: 140.0x50.8mm (Components on TOP: 244 [SMD=215], on BOTTOM: 40 [SMD=40])	Total nb of pins:	981

Ref.	Qty	SCEM	Description	Value	Fournisseur/Manufacturer	Part Number	Boitier/Outline
Circuit Imprimé / Printed Circuit Board							
EDA-04443-V1	1		**NA62 Active CFD** Printed Circuit Board (bare)		Panel of 2 PCBs		140.0x50.8mm
Matériel monté sur le PCB / Parts mounted on the PCB							
C1,C18,C20	3		50V 5% SMD Ceramic Capacitor - Class1 NP0/COG	1nF	GENERIC	CC0402_1NF_50V_5%_NP0	0402
C2->C7,C9->C11 C13,C19,C21->C28 C30,C32->C34 C36,C38,C40->C48 C52->C55,C57->C59 C61->C68,C70,C73 C74,C76,C78,C80 C83,C86,C93,C94 C100	60		16V 10% SMD X7R Ceramic Capacitor	10nF	GENERIC	CC0402_10NF_16V_10%_X7R	0402
C8,C17,C31,C35 C89	5		10V 10% SMD X7R Ceramic Capacitor	10uF	GENERIC	CC0805_10UF_10V_10%_X7R	0805
C12,C29,C37,C39 C49->C51,C56,C60 C69,C75,C77,C79 C81,C82,C84,C85 C87,C102->C135	52		16V 10% SMD X7R Ceramic Capacitor	100nF	GENERIC	CC0402_100NF_16V_10%_X7R	0402
C14	1		50V 5% SMD Ceramic Capacitor - Class1 NP0/COG	120pF	GENERIC	CC0402_120PF_50V_5%_NP0	0402
C15	1		50V 0.25pF SMD Ceramic Capacitor - Class1 NP0/COG	6pF	GENERIC	CC0402_6PF_50V_0.25PF_NP0	0402
C16	1		16V 10% SMD X7R Ceramic Capacitor	22nF	GENERIC	CC0402_22NF_16V_10%_X7R	0402
C71,C72	2		50V 5% SMD Ceramic Capacitor - Class1 NP0/COG	56pF	GENERIC	CC0402_56PF_50V_5%_NP0	0402
C88,C90,C91,C96 C97,C99	6		10V 20% SMD X5R Ceramic Capacitor	47uF	GENERIC	CC1206_47UF_10V_20%_X5R	1206
C92,C95,C98,C101	4		10V 10% SMD X7R Ceramic Capacitor	1uF	GENERIC	CC0805_1UF_10V_10%_X7R	0805
D1	1		Small Signal Diode		FAIRCHILD SEMICONDUCTOR	BAV99	SOT23
IC1,IC4	2		Ultrafast SiGe Voltage Comparator		ANALOG DEVICES	ADCMP582BCPZ	LFCSP16
IC2	1		900 MHz Differential Amplifier		TEXAS INSTRUMENTS	LMH6553SD	DFN8
IC3	1		Gain 4 Stable, Wideband Voltage Limiting Amplifier		TEXAS INSTRUMENTS	OPA699ID	SOIC8
IC5	1		Voltage-Controlled Gain Amplifier		TEXAS INSTRUMENTS	VCA824IDGST	SOP5

Colour Plan

SMD Top

Color	Qty	Reference	IPN	VALUE	OUTLINE
	5	PT1-PT5	3224J-1-501R	500	3224J
	1	IC17	ADA4932-2YCPZ	_	LFCSP-24
	2	IC7, IC12	ADCMP567BRPZ	_	LFCSP32
	2	IC1, IC4	ADCMP582BCPZ	_	QFN50P300X300X100-17N-S145

TE/MPE/EM Design Office

ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE
EUROPEAN ORGANISATION FOR NUCLEAR RESEARCH
GENEVE

EDA-[redacted]-V1-0

TOP

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Machine Files

- General advice:
  - ASCII CAD (export from Altium) or OBD++ streamlines programming
  - ALWAYS manage the panel layout in CAD, do not leave it to the PCB manufacturer.

  → Panel data in P&P + stencil!

- P&P for each component:
  - Reference
  - x-position
  - y-position
  - Rotation
  - Part number

To Reiterate…

Goals

Target	Approach
Accurate quotation	• Human readable summary • Easy to read and digest • Highlight key process-defining features
Within specification	• Referring to industrial standards • Proper tolerances
Acceptable quality	• Quality controls and reports clearly defined
Minimum cost	• Easy, clear quoting reduces margin
Retain intellectual property	• Don’t allow changes which are not reflected in the design

→ Human readable
→ Standard templates
→ Don’t over-specify
→ Contract basis

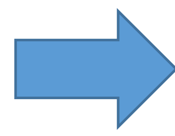
→ Changes not allowed unless clearly discussed

Three Layers

Design

Generic Specification

Industry Standards



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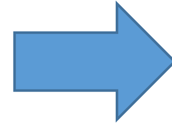
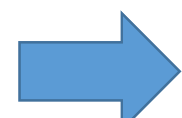


Standard documents, generic for all designs

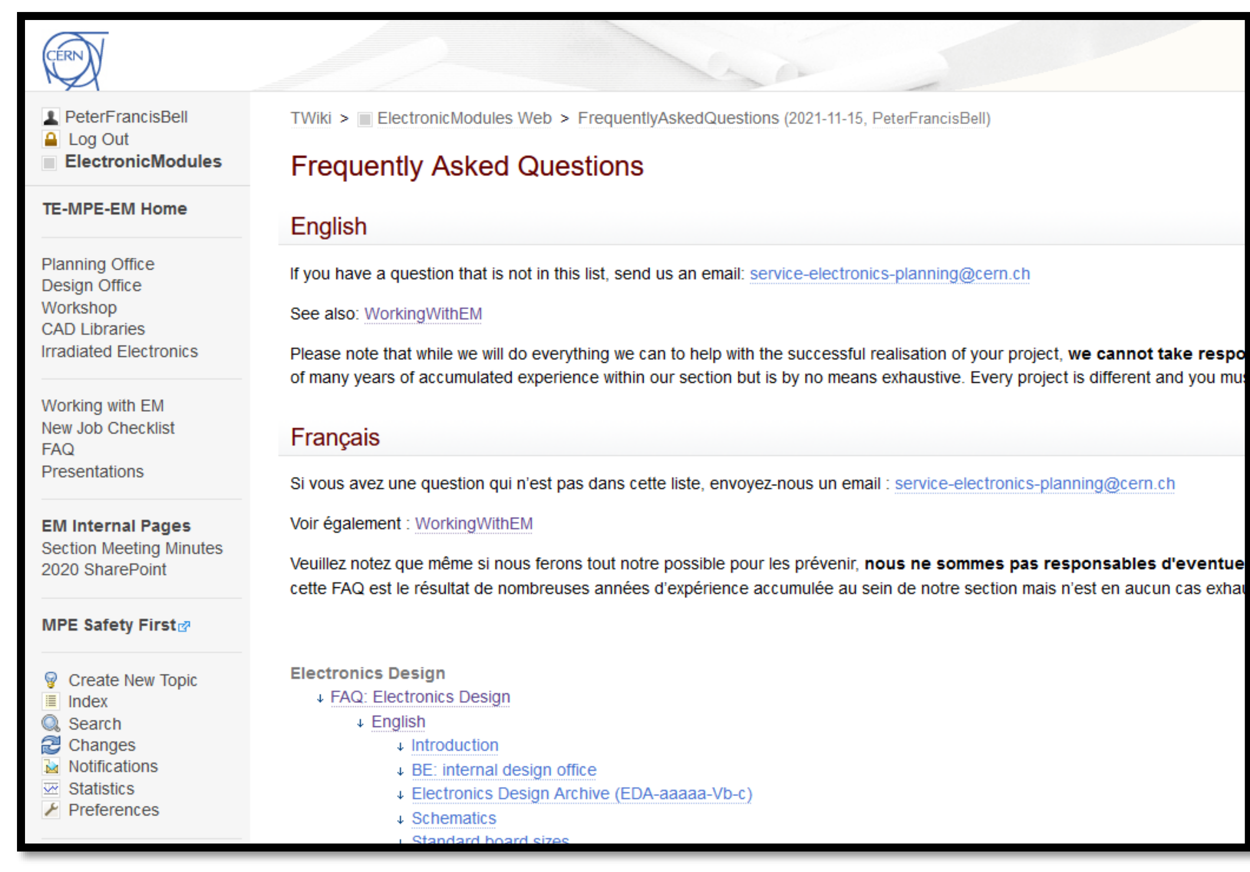


- IPC-2221A
- IPC-6011, IPC-A-600
- IPC-A-610, J-STD-001
- etc

Final Tips

Start with standard libraries

- https://twiki.cern.ch/twiki/bin/view/ElectronicModules/ComponentLibraries
- Available for Altium and Cadence
- Very well maintained and standardised
- “For free” to the CERN community



Frequently Asked Questions

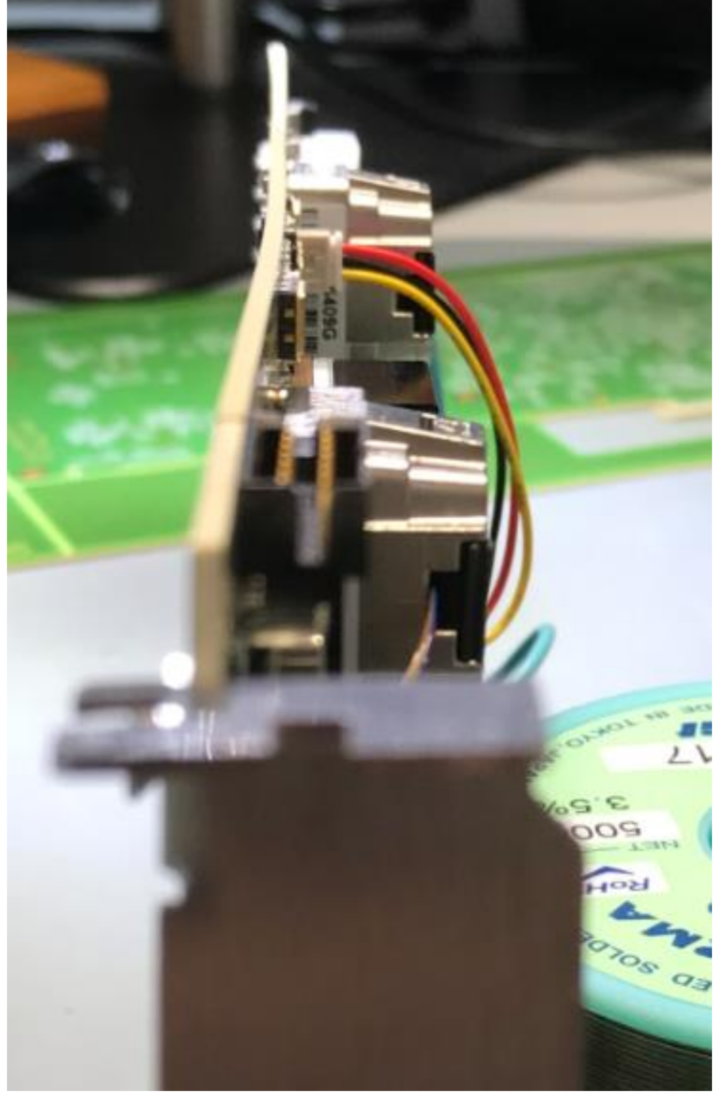
- https://twiki.cern.ch/twiki/bin/view/ElectronicModules/WebHome

Thank you for your
attention!

CERN

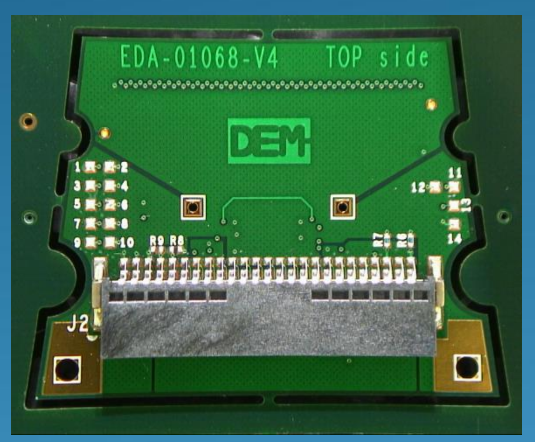
BE

Controls
Electronics &
Mechatronics



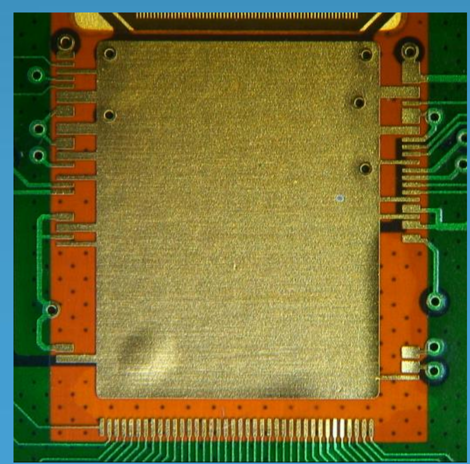
UNRELIABILITY AT CERN

Practical case: poor outsourcing practices



Does this board look like rocket science?

- Double-sided SMD
- 1 CoB (chip on board)
- 2 connectors
- 12 resistors/capacitors

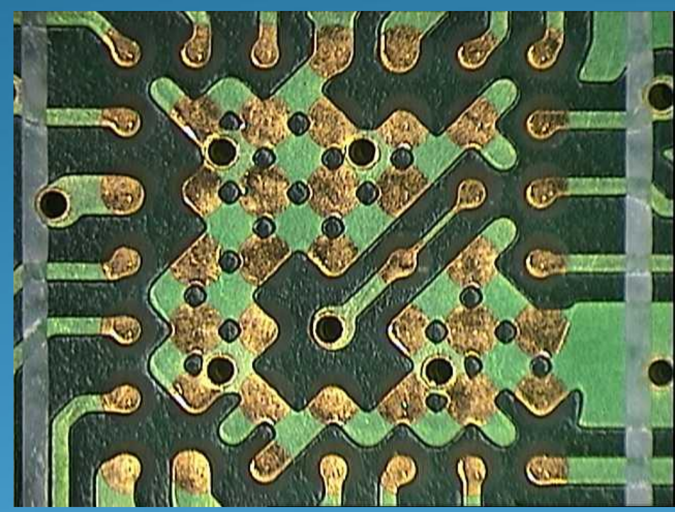


- 600+ boards
- 50% yield due to PCB delamination

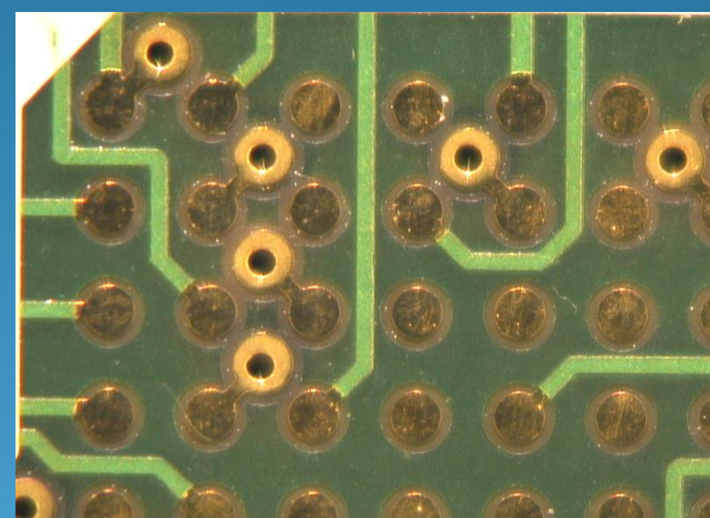
UNRELIABILITY AT CERN

Poor design practices: some examples

BGA design classics



Every ball shall have an individual pad with the same shape, except on certain occasions for reliability improvement



Vias close to BGA pads shall be tented to avoid solder wicking inside it and thus ensure homogene solder volume in joints