### **Next generation vertex detectors based on bent CMOS sensors wafers**

**Magnus Mager (CERN)**  *on behalf of the ALICE collaboration*  **IAS Program on High Energy Physics (HEP 2022) 13.01.2022**





# **Overview**



### **‣1. Motivation**

- large scale MAPS in HEP: ALICE ITS2
- proposal for **ITS3**
- performance predictions

- mechanical flexibility
- beam test results

- mechanics
- preparation of wafer-scale "super-ALPIDE"

### **‣2. Thin, bent sensors**

- test beam results
- design of wafer-scale chips

### **‣3. Wafer-scale sensors**

### **‣4. Next generation MAPS technology node: 65 nm**

### **‣5. Outlook**







# 1. Motivation











- ‣ Study of QGP in heavy-ion collisions at LHC
	- i.e. up to O(10k) particles to be tracked in a single event
- ▶ Reconstruction of charm and beauty hadrons
- ▶ Interest in low momentum (≤1 GeV/c) particle reconstruction



### **ALICE LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)**







### **6 layers:**

2 hybrid silicon pixel

 $\Lambda$ 

- 2 silicon drift
- 2 silicon strip

### **Inner-most layer:**

 radial distance: 39 mm material:  $X/X_0 = 1.14\%$ pitch: 50  $\times$  425  $\mu$ m<sup>2</sup> **rate capability:** 1 kHz

**7 layers:**  all MAPS 10 m2, 24k chips, 12.5 Giga-Pixels

 $\mathbf{Z}$ 

### **Inner-most layer:**

 radial distance: 23 mm material:  $X/X_0 = 0.35\%$ pitch: 29  $\times$  27  $\mu$ m<sup>2</sup> **rate capability:** 100 kHz (Pb-Pb)

LS2

Inner Tracking System

### Muon Forward Tracker

### **new detector**

**5 discs, double sided:** based on same technology as ITS2









# MFT

### **ITS2 overview**

### Outer Barrel (OB)

- **3 Inner Layers: 12+16+20 Staves 1 Module / Stave**
- **9 sensors per Module**
- **96 Modules to be produced (including one spare barrel)**







### Inner Barrel (IB)

- **2 Middle Layers: 30+24 Staves 2**⨉**4 Modules / Stave 2 Outer Layers: 42+48 Staves 2**⨉**7 Modules / Stave**
- **2**⨉**7 sensors / Module (Middle and Outer Layers are equipped with the same Module**
- **1880 Modules to be produced (including spares)**

### **ITS2 overview**

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*Good news: it is installed and commissioned in ALICE!*

# **ITS2 overview**



**27 cm** 

ALICE

**CALL TO BE DESIGN Report** September<br>Layon September

Upgrade of the<br>Inner Tracking

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Outer Barrel (OB)

# **PIXEL**

**A CERN for climate change** 

**96 Modules to be produced** 

**(including one spare barrel)** 



**2007** 



**(Middle and Outer Layers are** 

1880 Modules to be produced a second produced by the produced of the produced and

**(including spares)**

**Type and Contact of the United States of the United States and Type Action** 



**9 sensors**

**Cold Plate**

**Space Frame**

**Total:** 

 $-24$ 

 $-12.5$  GPixel  $-12.5$ 

**- 10 m2**

 $Bean$ 

*Good news: it is installed and commissioned in ALICE!*

147 cm

il

### **LHC pilot beam results September 2021, 900 GeV proton collisions**





### **LHC pilot beam results first, coarse results**

Primary vertices YZ correlation, nContributors > 0



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A new instrument has been taken into operation successfully!



# **ITS2 inner barrel**

- ITS2 is expected to perform according to specifications or even better
- ‣ The Inner Barrel is ultra-light but rather packed → further improvements seem possible
- ‣ **Key questions: Can we get closer to the IP? Can we reduce the material further?**



### ITS2: assembled three inner-most half-layers





### **Material budget a closer look**





- Observations:
	- Si makes only **1/7th** of total material
	- **irregularities** due to support/cooling
- ▶ Removal of water cooling
	- **possible** if power consumption stays below 20 mW/cm2





- ▶ Removal of the circuit board (power+data) - **possible** if integrated on chip
- ‣ Removal of mechanical support
	- **benefit** from increased stiffness by rolling Si wafers

### **ITS3 the idea (1): make use of the flexible nature of thin silicon**















### **ITS3 the idea (2): build wafer-scale sensors**







- ▶ Chip size is traditionally limited by CMOS manufacturing ("reticle size")
	- typical sizes of few cm<sup>2</sup>
	- modules are tiled with chips connected to a flexible printed circuit board
- ▶ New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
	- actively used in industry
	- a 300 mm wafer can house a sensor to equip a full half-layer
- -



### *- requires dedicated sensor design*



### **ITS3 detector concept**

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### ‣ Key ingredients:

- 300 mm wafer-scale sensors, fabricated using stitching
- thinned down to 20-40 μm  $(0.02-0.04\% X_0)$ , making them flexible
- bent to the target radii
- mechanically held in place by carbon foam ribs

### ‣ Key benefits:

- extremely low material budget:  $0.02 - 0.04\% X_0$ 
	- (beampipe: 500 μm Be: 0.14% X0)
- homogeneous material distribution: negligible systematic error from material distribution







### The whole detector will consist of six (!) sensors (current ITS IB: 432) – and barely anything else

# **ITS3 performance figures**

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### pointing resolution



improvement of factor 2 over all momenta



tracking efficiency



large improvement for low transverse momenta

**[ALICE-PUBLIC-2018-013]**

# **Lambda-c (Λc)**

### schematic view of a Λ<sub>c</sub> decay

- ‣ Analysis difficult due to large combinatorial background:
	- O(10k) charged particles in a central Pb-Pb collision
- ‣ Discrimination of background via:

- Particle identification (relatively low yield of protons and Kaons wrt. pions)
- **Topology: cut on DCA of single** tracks (before making the combinations) and decay vertex position (needs combinations)









**p**

**π**





**Lambda-c (Λc) (2)**



- Large improvement of S/B + significance due to better separation power of secondary decay vertex ( $\Lambda_c \approx 60 \text{ }\mu\text{m}$ )
- range Magnus Magnus Mager (CERN) | wafer-scale, bent CMOS | HEP2022 | 13.01.2022 | 16















# **Flexibility of silicon**

- ‣ **Monolithic** Active Pixel Sensors are quite flexible
	- already at thicknesses that are used for current detectors
- ‣ Bending force scales as (thickness)-3
	- large benefit from thinner sensors
- ‣ Breakage at smaller radii for thinner chips
	- again benefit from thinner sensors
- **‣Our target values are very feasible!**



- quite flexible
	- for current detectors



# **Flexibi**

- $\blacktriangleright$  **Monolith** quite flex
	- already for cur
- ‣ Bending force scales as (thickness)-3
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# **Flexibility of silicon**



### **Bending ALPIDE exampl**

tension wire

**PERSONAL** 

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foil

**CONTRACTORS** 

### 50 μm-thick ALPIDE

### $R = 18$  mm jig

# **Bent ALPIDEs**

- ‣ A number of prototypes with bent ALPIDEs were produced
	- several different ways were explored (bending before bonding, or vice versa, different jigs)
	- "feeling" for handling thin silicon was gained
- ‣ By now, we have a full mock-up of the final ITS3, called "μITS3"
	- 6 ALPIDE chips, bent to the target radii of ITS3









### **Beam tests campaigns**

- ‣ A series of beam tests was performed in 2020 and 2021:
	- Jun 2020 (DESY): first bent chip
	- Aug 2020 (DESY): bent chip on cylinder
	- Dec 2020 (DESY): bent chip at large radii
	- Apr 2021 (DESY): bent chips at all radii, carbon foam
	- Jul 2021 (SPS): μITS3, "₩"
	- Sep 2021 (DESY): MLR1, "₩", carbon foam





### **Beam tests campaigns**

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	- Apr 2021 (DESY): bent chip radii, carbon foam
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	- Sep 2021 (DESY): MLR1, "₩", carbon foam

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**Intense and diverse programme throughout difficult times** 

**Many thanks to DESY and CERN/SPS!**

### **Beam tests 1st paper [doi:10.1016/j.nima.2021.166280](https://doi.org/10.1016/j.nima.2021.166280)**



Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale  $(10^{-1}$  to  $10^{-5}$ ) to show fully efficient rows. Each data point corresponds to at least 8k tracks.





Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment Available online 10 January 2022, 166280 In Press, Journal Pre-proof (?)

First demonstration of in-beam performance of bent Monolithic **Active Pixel Sensors** 

ALICE ITS project<sup>1</sup>

Show more  $\vee$ 

∞ Share ■ Cite

https://doi.org/10.1016/j.nima.2021.166280

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### Clearly proving that bent MAPS are working!

### **Beam tests**

- ‣ Studies are now repeated for all ITS3 radii (18, 24, 30 mm)
	- no effect depending on the radius observed
- ‣ Results also match the published results - where the chip was bent along the other direction

![](_page_28_Picture_5.jpeg)

![](_page_28_Figure_6.jpeg)

₹

otal

![](_page_28_Figure_7.jpeg)

### **efficiencies and spatial resolutions at different radii**

![](_page_28_Figure_11.jpeg)

![](_page_28_Picture_13.jpeg)

### **Beam tests more data**

- ‣ Very interesting geometries are becoming possible
- ‣ For instance, one can observe two crossings of the same particle

![](_page_29_Picture_5.jpeg)

double-crossing grazing

. . . . . . . . . . . . . . . . . G

![](_page_29_Picture_9.jpeg)

![](_page_29_Picture_10.jpeg)

![](_page_29_Picture_3.jpeg)

![](_page_29_Picture_4.jpeg)

![](_page_30_Figure_0.jpeg)

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### **Beam tests μITS3**

- ‣ <sup>μ</sup>ITS3, i.e. 6 ALPIDEs at ITS3 radii
	- two complete setups based on "gold" quality ALPIDE chips
	- one has a Cu target in the center: expect to see 120 GeV proton/pion–Cu collisions
- ‣ Several days of continuous data taking
	- detailed analysis ongoing

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![](_page_31_Picture_14.jpeg)

![](_page_31_Picture_10.jpeg)

![](_page_31_Picture_11.jpeg)

![](_page_31_Picture_6.jpeg)

### First "real" experiment, allows to study tracking/reconstruction

# **Beam tests μITS3**

![](_page_32_Figure_1.jpeg)

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![](_page_32_Picture_7.jpeg)

![](_page_32_Picture_8.jpeg)

![](_page_32_Picture_3.jpeg)

### First "real" experiment, allows to study tracking/reconstruction

### **Beam tests "curiosity"**

![](_page_33_Figure_4.jpeg)

- ‣ ₩ (won): ALPIDE bent into a "W" shape
	-
- 

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![](_page_33_Picture_8.jpeg)

![](_page_33_Picture_9.jpeg)

### This technology has a lot more to offer – time to be creative!

# 3. Wafer-scale sensors

![](_page_34_Picture_1.jpeg)

![](_page_34_Picture_3.jpeg)

### **Bending of wafer-scale sensors procedure**

![](_page_35_Picture_1.jpeg)

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![](_page_35_Picture_4.jpeg)

### 30 mm (layer 2) 50 μm dummy Silicon

### **Attachment of foam supports procedure**

- ‣ Assembly process being developed
- ‣ Different options under study (incl. vacuum clamping)
- ‣ Currently working solution based on segmented mylar foil

![](_page_36_Picture_11.jpeg)

![](_page_36_Picture_4.jpeg)

![](_page_36_Picture_6.jpeg)

![](_page_36_Picture_7.jpeg)

### **Layer assembly**

![](_page_37_Picture_3.jpeg)

![](_page_37_Picture_1.jpeg)

### 3-layer integration successful!

### **Carbon foam support structure**

- ‣ Different foams were characterised for machinability and thermal properties
- **Baseline is** ERG DUOCEL\_AR, which also features the largest radiation length

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![](_page_38_Picture_15.jpeg)

![](_page_38_Figure_3.jpeg)

![](_page_38_Picture_5.jpeg)

![](_page_38_Picture_6.jpeg)

### ALLCOMP\_HD

 $0.45 - 0.68$  kg/dm<sup>3</sup> 85-170 W/m·K

![](_page_38_Picture_9.jpeg)

![](_page_38_Picture_10.jpeg)

![](_page_38_Picture_11.jpeg)

### Carbon foam selection is complete

### **Layer assembly optimisation of glueing**

Carbon foam wedge: **ERG Duocel**  $[0.06 \text{ kg/dm}^3]$ Carbon fleece  $[8g/m<sup>2</sup>]$ 

Glue: Araldite 2011

![](_page_39_Picture_3.jpeg)

![](_page_39_Figure_4.jpeg)

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![](_page_39_Picture_16.jpeg)

![](_page_39_Picture_17.jpeg)

![](_page_39_Picture_5.jpeg)

![](_page_39_Picture_7.jpeg)

![](_page_39_Picture_8.jpeg)

### First assembly has shown glue penetration in the carbon foam by capillarity

Silicon

![](_page_39_Picture_11.jpeg)

![](_page_39_Figure_13.jpeg)

### Helps to really put the material budget down as much as possible

### **Layer interconnection "super-ALPIDE"**

![](_page_40_Picture_3.jpeg)

- ‣ To study the bending **and** interconnection of **large** pieces of processed chips, "super-ALPIDE" is built
	- consists of 1 silicon piece cut from an ALPIDE wafer (9x2 dies, approx 1/2 of layer 0)

### **Layer interconnection (2) "super-ALPIDE"**

- ‣ A bonding jig is being prepared
- ‣ the first row of ALPIDEs will be wire-bonded to an edge-FPC
	- just like the final detector,
- ‣ super-ALPIDE/L0 will be hold by an exoskeleton that:
	- mimics L1
	- and allows to interconnect all remaining ALPIDE dies

![](_page_41_Picture_7.jpeg)

![](_page_41_Picture_9.jpeg)

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![](_page_41_Picture_16.jpeg)

![](_page_41_Picture_17.jpeg)

![](_page_41_Picture_18.jpeg)

![](_page_41_Picture_19.jpeg)

### long wires for testing

![](_page_41_Picture_11.jpeg)

### edge bonds (like final ITS3)

![](_page_41_Picture_13.jpeg)

### Key R&D for combining electrical and mechanical prototypes

4. Next generation MAPS technology node: 65 nm

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![](_page_42_Picture_2.jpeg)

**CERN** 

# **65 nm prototypes, MLR1**

- ‣ First submission in TowerJazz 65nm
- scoped within CERN EP R&D WP1.2
- significant drive from ITS3
- + important contributions from outside (not ALICE) groups
- ‣ Contained several test chips
	- radiation test structures
	- pixel test structures
	- pixel matrices
	- analog building blocks (band gaps, LVDS drivers, etc)

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![](_page_43_Picture_17.jpeg)

~12 mm

![](_page_43_Figure_2.jpeg)

~16 mm

![](_page_43_Picture_5.jpeg)

Very versatile first submission, combining what was initially planned for 2 MPWs

# **65 nm prototypes, MLR1**

 $~12$  mm

![](_page_44_Figure_2.jpeg)

- ‣ Fully processed wafers are back by now
- Plenty of material ready for testing, literarily thousands of chips
- ▶ Produced with 4 different process splits
	- TCAD-guided optimisations in collaboration with foundry, comparable to TJ180nm

![](_page_44_Picture_12.jpeg)

![](_page_44_Figure_13.jpeg)

~16 mm

![](_page_44_Picture_4.jpeg)

![](_page_44_Picture_5.jpeg)

![](_page_44_Picture_10.jpeg)

### **65 nm prototypes, MLR1 Digital Pixel Test Structure (DPTS)**

- ▶ Most "aggressive" chip in MLR1
- $\rightarrow$  32  $\times$  32 pixels, 15 µm pitch
	- sizeable prototype, allows for "easy" test beam integration
- ‣ Asynchronous digital readout with ToT information
- ‣ Allows to verify:
	- sensor performance
	- front-end performance
	- basic digital building blocks
	- SEU cross-sections of registers

![](_page_45_Picture_11.jpeg)

![](_page_45_Figure_13.jpeg)

![](_page_45_Picture_15.jpeg)

scintilator

### 3 ALPIDE 2 DPTS 3 ALPIDE

![](_page_46_Picture_10.jpeg)

![](_page_46_Picture_11.jpeg)

![](_page_46_Picture_4.jpeg)

**scintilator** 

### XY-stage

### **First beam test** XY-stage **Telescope with DPTS**

- ‣ Scintillator with 1mm hole can be used to trigger on narrow beam spot
- ‣ 6 precision linear stages with remote control allow to precisely align 2 DTPS and scintillators

![](_page_46_Picture_3.jpeg)

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3 ALPIDE (ref) 3 ALPIDE (ref) 2 DPTS (DUT) 1 PMT (trg) 1 PMT 1 PMT (trg) (anti)

![](_page_47_Picture_6.jpeg)

![](_page_47_Picture_1.jpeg)

![](_page_47_Picture_3.jpeg)

30 mm

![](_page_48_Picture_5.jpeg)

30 mm

![](_page_48_Picture_1.jpeg)

![](_page_48_Picture_2.jpeg)

![](_page_49_Picture_5.jpeg)

30 mm

![](_page_49_Picture_1.jpeg)

![](_page_49_Picture_2.jpeg)

![](_page_50_Picture_5.jpeg)

![](_page_50_Picture_2.jpeg)

![](_page_50_Picture_3.jpeg)

### Scintillator (veto)

![](_page_51_Figure_1.jpeg)

first few % of total statistics analysed

![](_page_51_Picture_3.jpeg)

![](_page_51_Picture_4.jpeg)

‣ Beam spot and trigger tuned to illuminate a small area

![](_page_51_Picture_7.jpeg)

![](_page_52_Figure_1.jpeg)

first few % of total statistics analysed

![](_page_52_Picture_3.jpeg)

![](_page_52_Picture_4.jpeg)

### **DPTSD** wafer: 22 version: 1 split: 4 (opt.)  $V_{\text{pwell}} = -1.2 \text{ V}$

- $V_{sub} = -1.2 V$  $I_{reset} = 10 \text{ pA}$  $I_{bias} = 100 \text{ nA}$  $I_{biasn} = 10 nA$  $I_{db} = 100 \text{ nA}$
- ‣ Beam spot and trigger tuned to illuminate a small area
- ‣ Looking at tracks without hit in the DPTS, a clear 100% shadow is seen

![](_page_52_Picture_10.jpeg)

![](_page_52_Picture_11.jpeg)

![](_page_53_Figure_1.jpeg)

first few % of total statistics analysed

![](_page_53_Picture_3.jpeg)

![](_page_53_Picture_4.jpeg)

### wafer: 22

- version: 1 split: 4 (opt.)  $V_{\text{pwell}} = -1.2 \text{V}$  $V_{sub} = -1.2 V$  $I_{reset} = 10 \text{ pA}$  $I_{bias} = 100 \text{ nA}$  $I_{biasn} = 10 nA$  $I_{db} = 100 \text{ nA}$  $V_{casn}$  = 300 mV  $V_{cash} = 250$  mV
- ‣ Beam spot and trigger tuned to illuminate a small area
- ‣ Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- ‣ **166/166** tracks in region of interest

![](_page_53_Picture_12.jpeg)

- ‣ Beam spot and trigger tuned to illuminate a small area
- ‣ Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- ‣ **166/166** tracks in region of interest - similar for second chip **(162/162)**

![](_page_54_Picture_12.jpeg)

![](_page_54_Figure_1.jpeg)

first few % of total statistics analysed

**DPTSE** wafer: 22  $chip: 1$ version: X split: 4 (opt.)  $V_{\text{pwell}} = -1.2 \text{ V}$  $V_{sub} = -1.2 V$  $I_{reset} = 10 \text{ pA}$  $I_{bias} = 100 \text{ nA}$  $I_{biasn} = 10 nA$  $I_{db} = 100 \text{ nA}$  $V_{casn} = 300 \text{ mV}$ 

![](_page_54_Picture_5.jpeg)

![](_page_54_Picture_6.jpeg)

![](_page_55_Figure_1.jpeg)

first few % of total statistics analysed

![](_page_55_Picture_3.jpeg)

![](_page_55_Picture_4.jpeg)

‣ Beam spot and trigger tuned to

illuminate a small area

- version: 1 split: 4 (opt.)  $V_{\text{pwell}} = -1.2 \text{ V}$  $V_{sub} = -1.2 V$  $I_{reset} = 10 \text{ pA}$  $I_{bias} = 100 \text{ nA}$  $I_{biasn} = 10 nA$  $I_{db} = 100 \text{ nA}$  $V_{casn} = 300 \text{ mV}$  $V_{cash} = 250$  mV
- ‣ Looking at tracks without hit in the DPTS, a clear 100% shadow is seen

- The area matches precisely the DPTS
- split: 4 (opt.)  $V_{\text{pwell}} = -1.2 \text{ V}$  $V_{sub} = -1.2 V$  $I_{reset} = 10 \text{ pA}$  $I_{bias} = 100 \text{ nA}$  $I_{biasn} = 10 nA$
- ‣ **166/166** tracks in region of interest
	- similar for second chip **(162/162)**
	- and even for both in coincidence **(83/83)**

![](_page_55_Picture_14.jpeg)

![](_page_56_Figure_1.jpeg)

![](_page_56_Picture_3.jpeg)

![](_page_56_Picture_4.jpeg)

‣ Beam spot and trigger tuned to

illuminate a small area

- version: 1 split: 4 (opt.)  $V_{\text{pwell}} = -1.2 \text{ V}$  $V_{sub} = -1.2 V$  $I_{reset} = 10 \text{ pA}$  $I_{bias} = 100 \text{ nA}$  $I_{biasn} = 10 nA$  $I_{db} = 100 \text{ nA}$  $V_{casn} = 300 \text{ mV}$  $V_{cash} = 250$  mV
- ‣ Looking at tracks without hit in the DPTS, a clear 100% shadow is seen

- The area matches precisely the DPTS
- version: X split: 4 (opt.)  $V_{\text{pwell}} = -1.2 \text{ V}$  $V_{sub} = -1.2 V$  $I_{reset} = 10 \text{ pA}$  $I_{bias} = 100 \text{ nA}$  $I_{biasn} = 10 nA$
- ‣ **166/166** tracks in region of interest
	- similar for second chip **(162/162)**
	- and even for both in coincidence **(83/83)**

### **Figure 10 Sensor** *and* **front-end performance already from** *first* **65 nm prototype and** *first* **65 nm and** *first* **65 nm <b>***nototype*

![](_page_56_Picture_15.jpeg)

![](_page_56_Picture_19.jpeg)

![](_page_57_Picture_138.jpeg)

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![](_page_57_Picture_7.jpeg)

![](_page_57_Picture_11.jpeg)

![](_page_57_Figure_1.jpeg)

**Figure 10 Sensor** *and* **front-end performance already from** *first* **65 nm prototype and** *first* **65 nm and** *first* **65 nm <b>***nototype* 

![](_page_57_Picture_3.jpeg)

![](_page_57_Picture_4.jpeg)

### **Towards a wafer-scale sensor**

‣ Next big milestone in sensor design: **stitching**

![](_page_58_Picture_58.jpeg)

![](_page_58_Picture_6.jpeg)

![](_page_58_Picture_7.jpeg)

![](_page_58_Figure_2.jpeg)

![](_page_58_Picture_3.jpeg)

### **Towards a wafer-scale sensor** ER1 **Design activity at full swing**

![](_page_59_Figure_1.jpeg)

![](_page_59_Picture_3.jpeg)

- 
- 
- 
- 
- 

![](_page_59_Picture_10.jpeg)

# **Summary**

- a deeper sub-micron technology node (**65 nm** vs. 180 nm) allows for larger wafers (300 mm vs. 200 mm) with

- Monolithic CMOS sensors are successfully employed on large scale in HEP
	- latest instalment, **ALICE ITS2** (10 m2, TowerJazz 180 nm), **is taking data at LHC**
- The technology has still much more to offer:
	- at thicknesses of 50 μm the chips are **flexible**
	- the CMOS manufacturing process allows to produce **wafer-scale chips**
	- higher integration density
- ‣ **ALICE** proposes to build the next-generation Inner Tracking System, based on **<sup>300</sup> mm-wafer-scale**, **20-40 μm-thin**, **bent MAPS** 
	- large interest and active contribution of **many institutes** within and outside ALICE
	- physics scope continues to grow, idea is being picked up by other future experiments
- ‣ **R&D** is making rapid progress on all fronts, in particular:
	- **successful in-beam verification of bent MAPS**
	- **full-size mechanical mockups: build and characterised**
	- **65 nm validation: very high detection efficiency proven in beam**
- ‣ **Bent, ultra-light vertex detectors have become a reality!**

![](_page_60_Picture_15.jpeg)

![](_page_60_Picture_24.jpeg)

![](_page_61_Picture_4.jpeg)

![](_page_61_Picture_0.jpeg)

![](_page_61_Picture_1.jpeg)

![](_page_61_Picture_2.jpeg)