17th Trento Workshop on Advanced Radiation Sensors

3D Sensors

Single cell 3D timing: Time resolution assessment and Landau contribution evaluation via test-beam and laboratory measurements

Evangelos – Leonidas Gkougkousis

CERN EP-R&D

Geneve – March 3rd, 2022

•Introduction, EP-R&D W.P. 1.1 – Hybrid Sensors

Planar Sensors (J. Haimberger, V. Gkougkousis)

- ✓ Radiation damage and trapping model validation though TCAD
- ✓ Timing and efficiency at < 1e17 n_{eq}/cm^2 using fast neutrons and ps protons (thicknesses 50, 100, 200, 300 µm)

LGADs (V. Gkougkousis)

- ✓ Radiation damage mechanisms and modeling on different dopant types (TIPP2021, ArXiV Preprint, PicoSecond Workshop 2021)
- ✓ Indium-Lithium gain layer radiation hardness investigations (Trento2021)
- ✓ Process simulations and SiMS – Carbon/Boron (LINK)

Silicon Electron Multiplier (M. Halvorsen, LINK, ArXiV Preprint, IEEE)

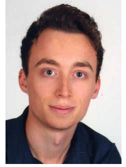
- ✓ Structure optimization and electrostatic simulations
- ✓ Timing and transient Simulations
- ✓ Process iterations (Metal Assisted Etching)

Talks @ Trento 2022

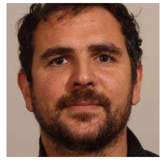
Small Pitch 3Ds for tacking and timing (V. Gkougkousis, LINK)

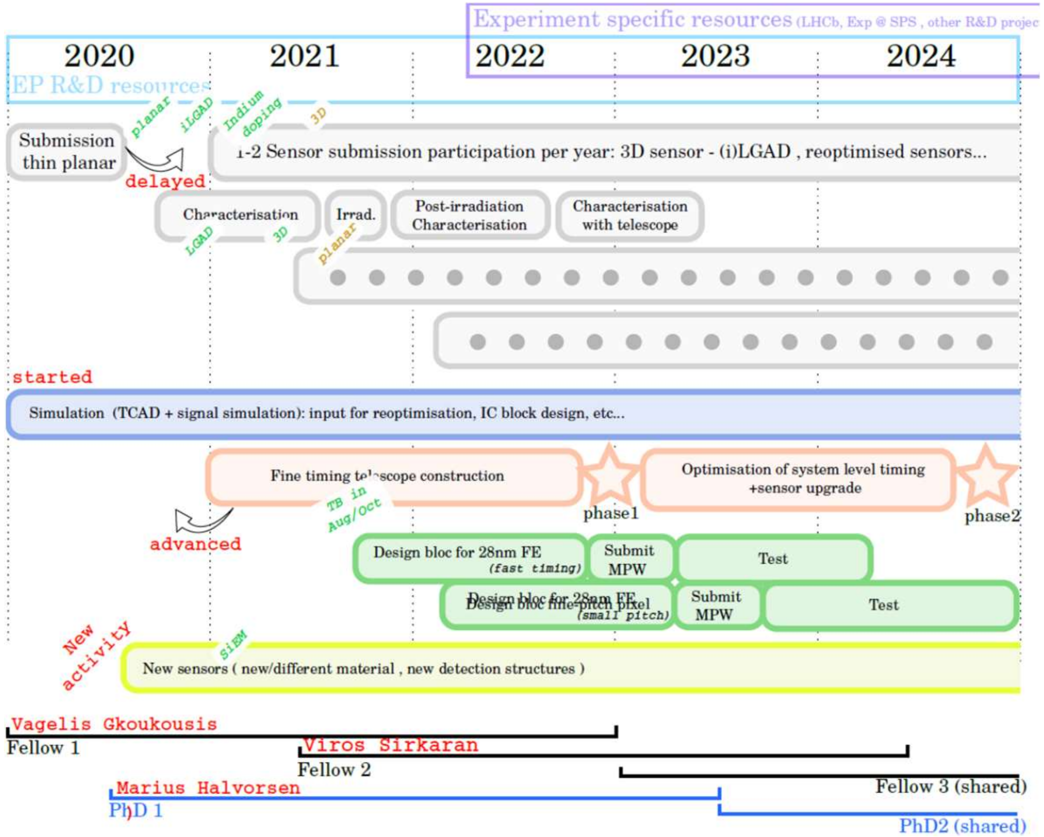
- ✓ **β particles timing studies on irradiated and unirradiated devices**
- ✓ **Test beam with SPS pions (Tracking + Timing)**
- ✓ Proton and neutron irradiations > 1e17 n_{eq}/cm^2
- ✓ New small pitch production optimized for gain at the electrode region


Vagelis Gkougkousis


Jakob Haimberger


Marius Halvorsen


Victor Coco



•3D Sensors for timing

3D Sensors: <u>Decoupling of charge generation and drift volume</u>
(*Standard columns, TimeSpot, Hex geometries* ect.)

Pros

- High radiation tolerance up to several times 10^{16} n_{eq}/cm^2
- Short drift distances with fast rise times
- Reduced Landau fluctuation, practically non-existent for perpendicular tracks

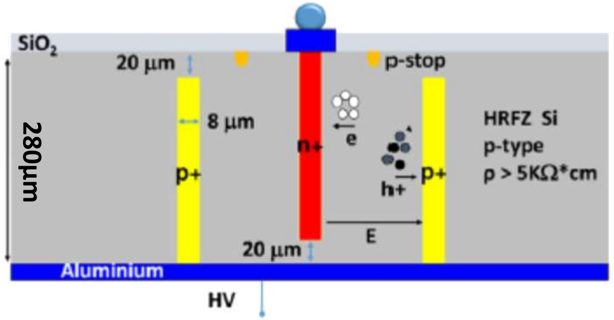
Cons

- Non-uniform field geometry
- High cost
- Increased cell capacitance

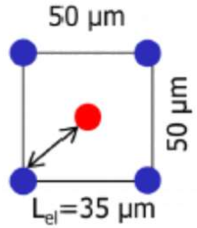
Tested Devices

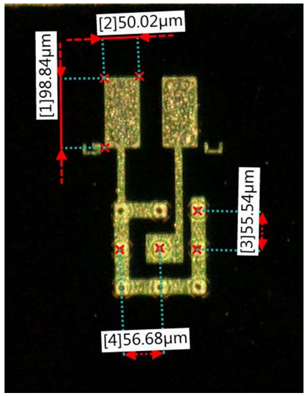
- Process: 2-sided
- Substrate: high Z, p-type FZ Silicon, 4" wafers
- Thickness: ~ 280 um
- Run: CNM 5936-11
- Pixel Geometry: 50 x 50 um, 1E, single cell
- Capacitance: ~80 – 100 pF per cell

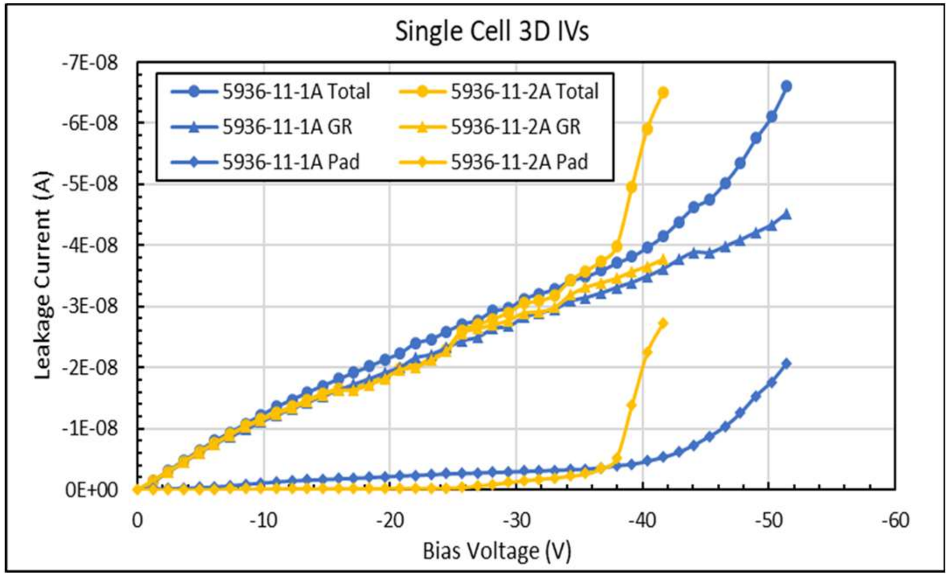
CNM double sided n-on-p, 50 x 50 μm



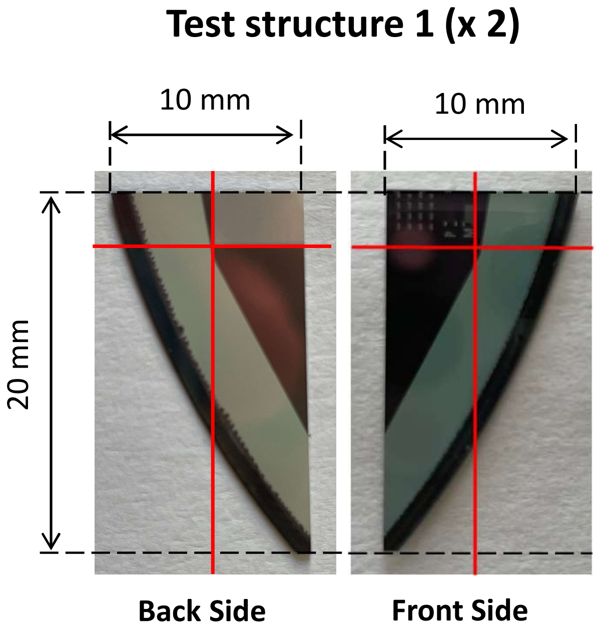
50x50 μm², 1E

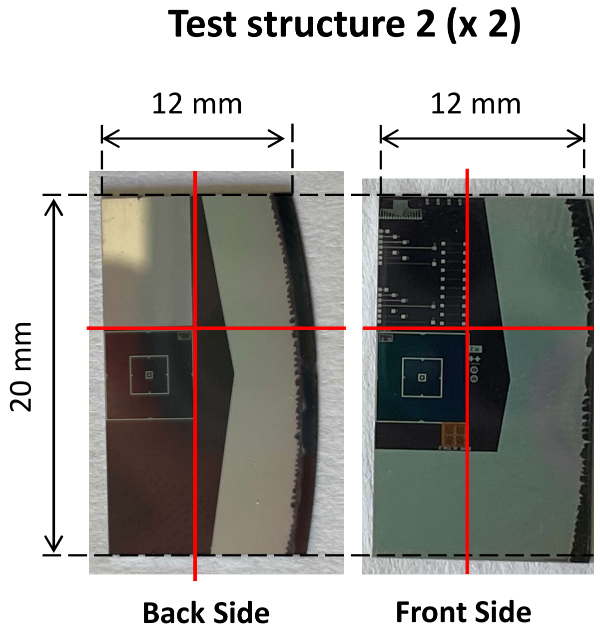


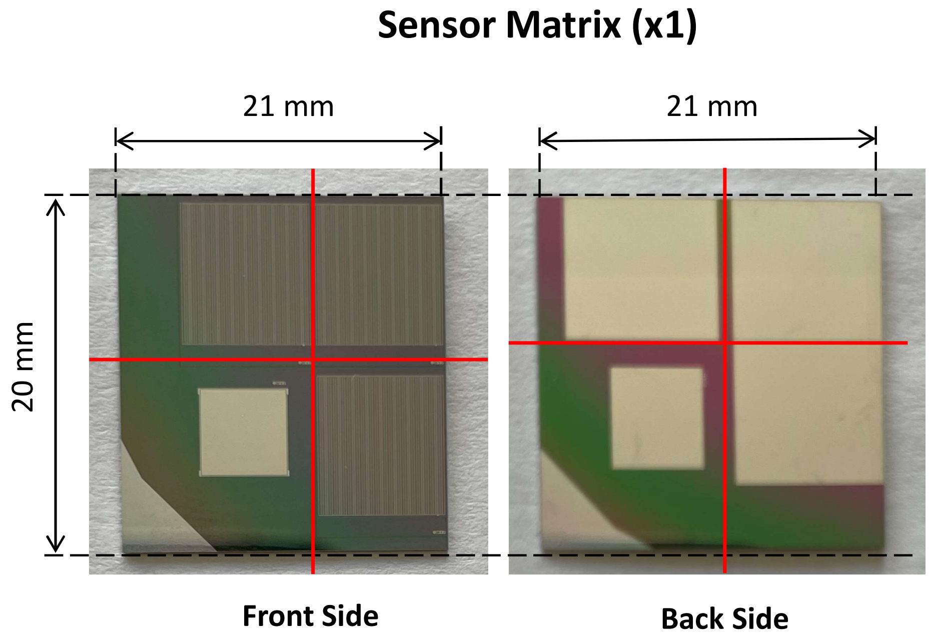




•Sample preparation and dicing



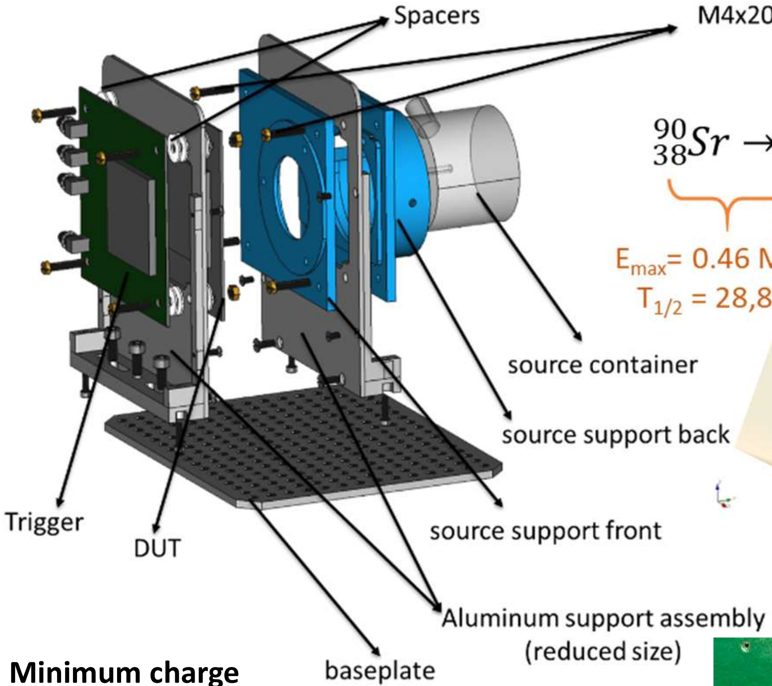




— **Dicing Lines**

Material: Hi Resistivity (>2kOhm×cm), p-type, Fz Silicon
Thickness: ~285 um
Planarity: < 1um
Inter-matrix distance: 200 um
Preparation: Adhesive tape + Photoresist
Dicing at CMi in Lausanne as an external service

•β Source Characterization



$^{90}_{38}Sr \rightarrow^{e^-} {}^{90}_{39}Y \rightarrow^{e^-} {}^{90}_{40}Zr$

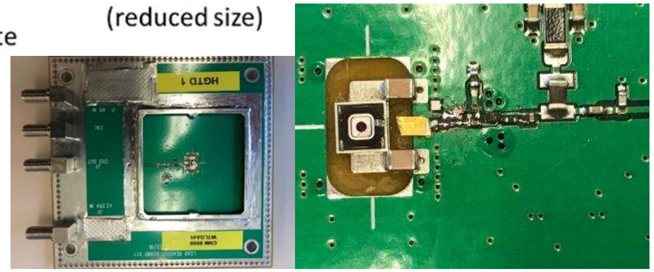
E_{max}= 0.46 MeV, $T_{1/2}$ = 28,8 y

E_{max}= 2.28 MeV, $T_{1/2}$ = 64 h

90 µm Al absorber
+ 500 µm Si

Minimum charge for good timing

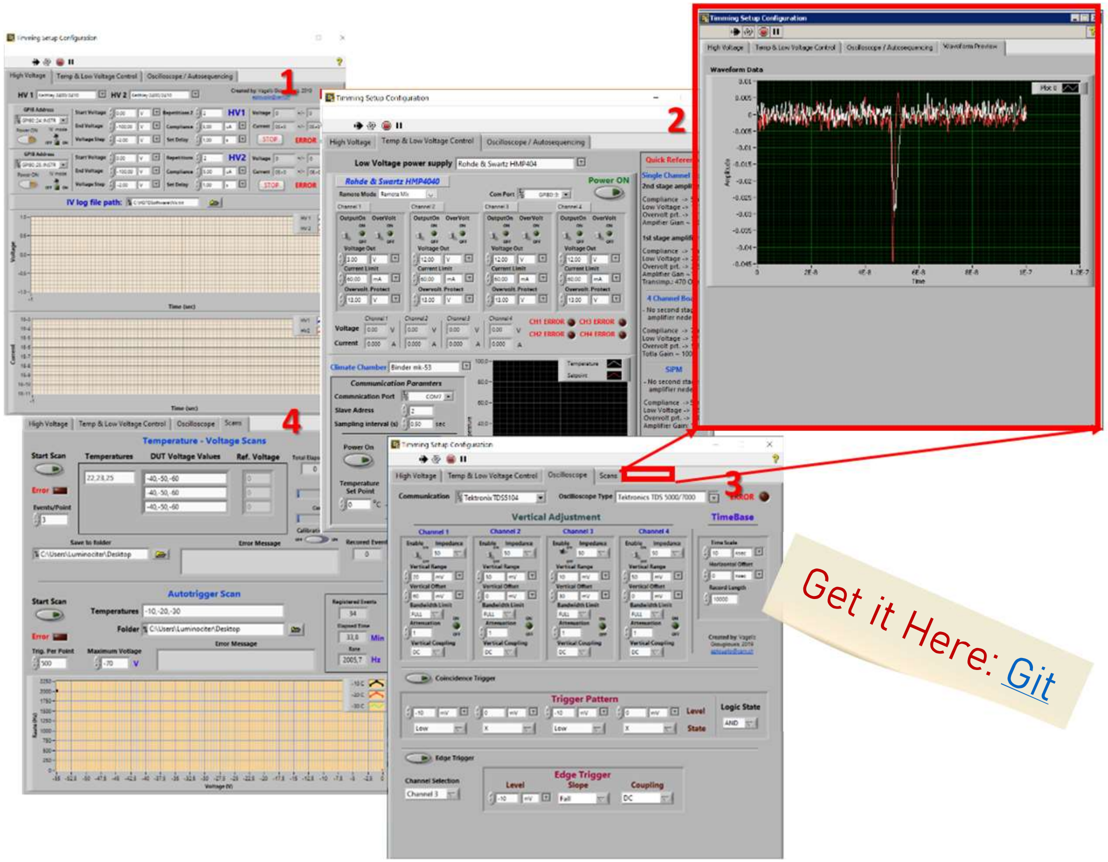
5 σ from noise



- High frequency SiGe (~2GHz) amplifier
- Mean sensor + amplifier noise < 1.5 mV
- 5000 recorded events per point

Timing Configuration & Automation Software (TiCAS)

- Real-time Waveform Visualization
- Dynamic adaptable UI with universal instrument support
- Support for all LeCroy, Tektronix and Agilent oscilloscopes

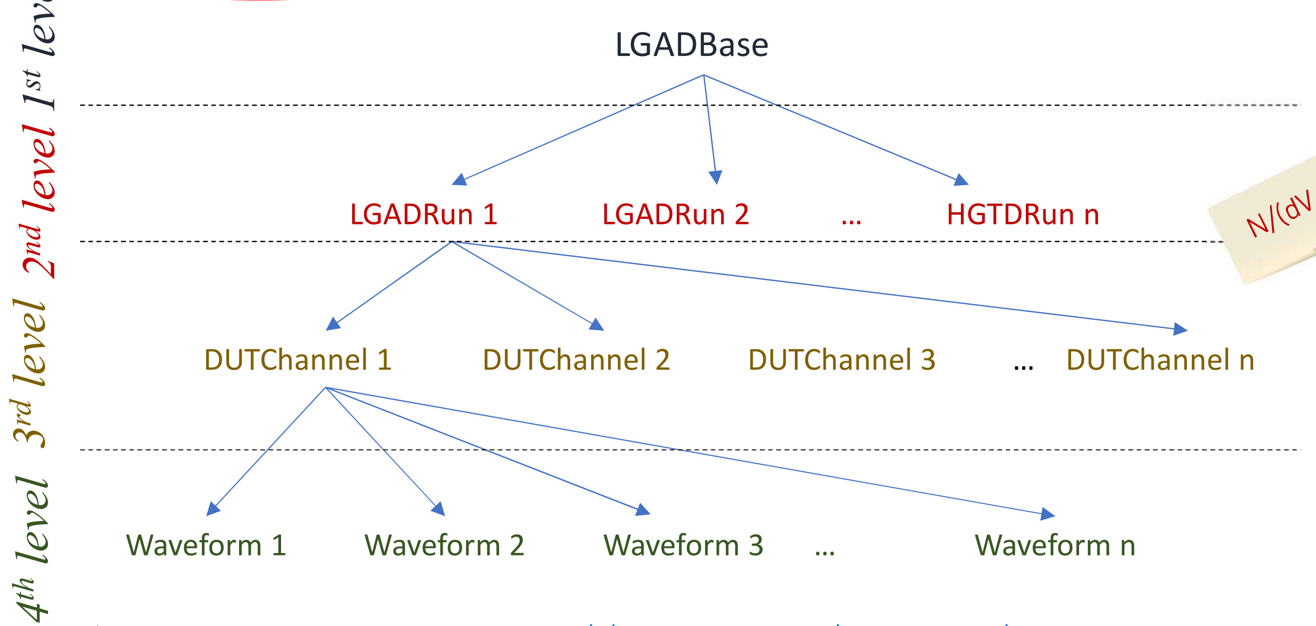


Get it Here: Git

•Analysis Framework

- Four main classes with dedicated header and implementation files, one wrapper class handling user interaction

LGADUtils → Wrapper to handle user I/O and pass arguments
- LGADBase → Basic framework function and infastructure
- LGADRun → Timing resolution, CFD maps, multi DUT operations
- LGADChannel → Mean pulse shape, mean pulse properties form entire run
- WaveForm → Single Waveform properties and time walk corrections
- Bonus: LGADSel → Selector Class with auto-set 64 channel support



- Code available on git: https://gitlab.cern.ch/egkougko/lgadutils

C++ 11

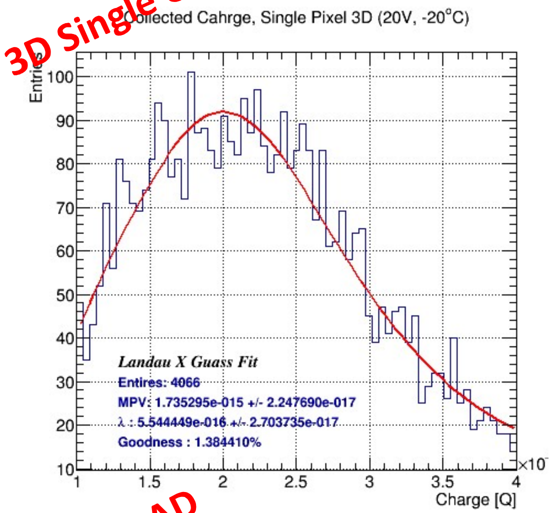
- Iterative re-fitting and re-binning algorithm
- Fitting of discrete and variable binning quantities
- Bayesian uncertainties at efficiency level
- Event by event FFT transimpedance correction

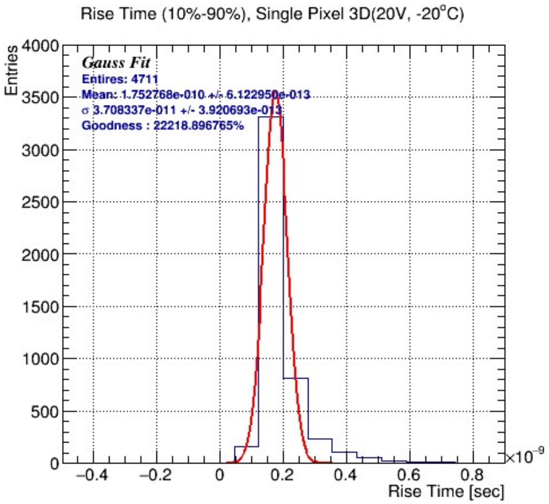
N/(dV/dt) , T_{Rise}/SNR

Quantity	**Applied Fit type**
Min, Max voltage :	Gauss, Gauss x Landau fit
Start, stop, min, max indices :	Gauss, Gaussian fit
Noise / pedestal :	Gaussian fit
Min, Max, Rise, Trigger time :	Gaussian fit
Charge, dV/dT, Jitter, ToT:	Gauss x Landau fit
FFT:	Variable bin Gaussian

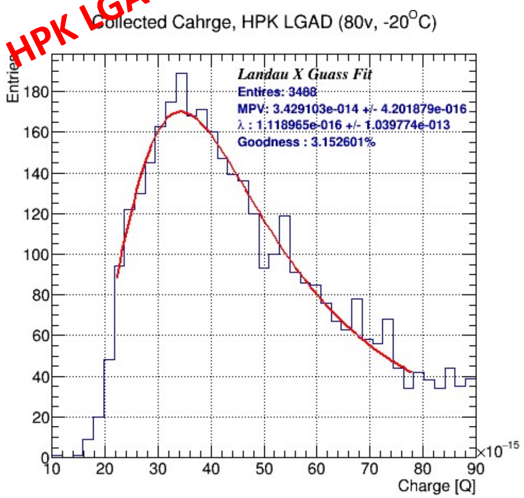
•Laboratory results

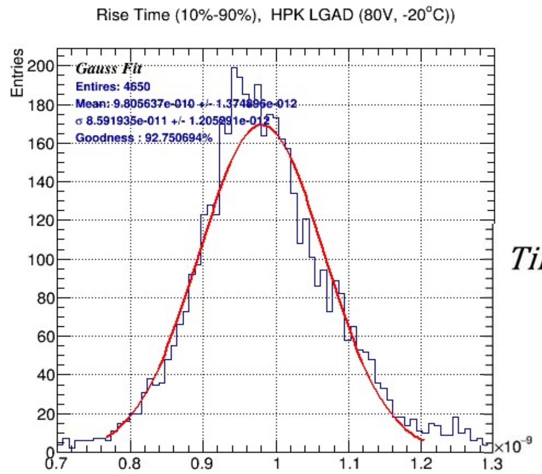
3D Single Cell





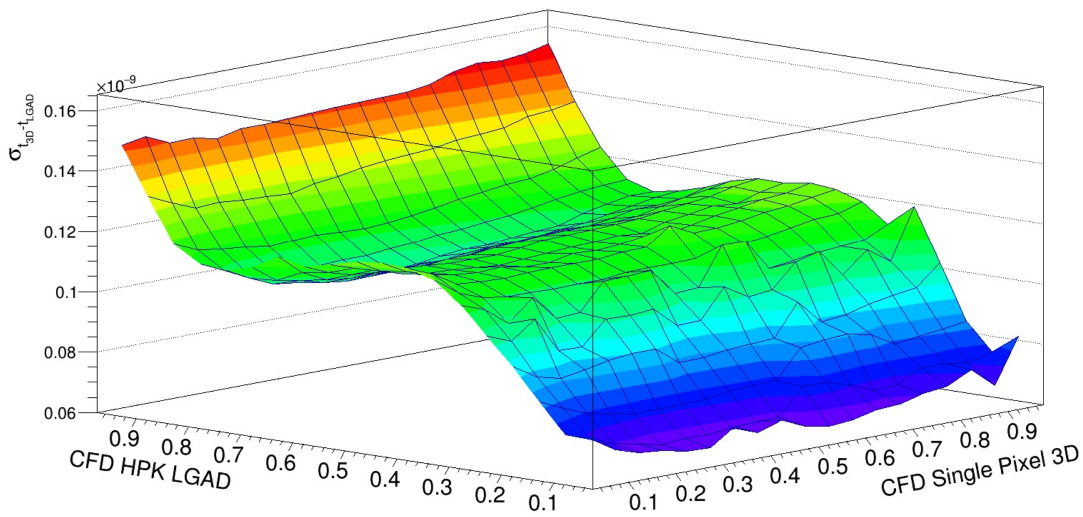
HPK LGAD





$$(\sigma_{\mathrm{Dut}})_{CFD_{ij}} = \sqrt{(\sigma^2_{\mathrm{Tot}})_{CFD_{ij}} - (\sigma^2_{\mathrm{Ref}})_{CFD_i}}$$

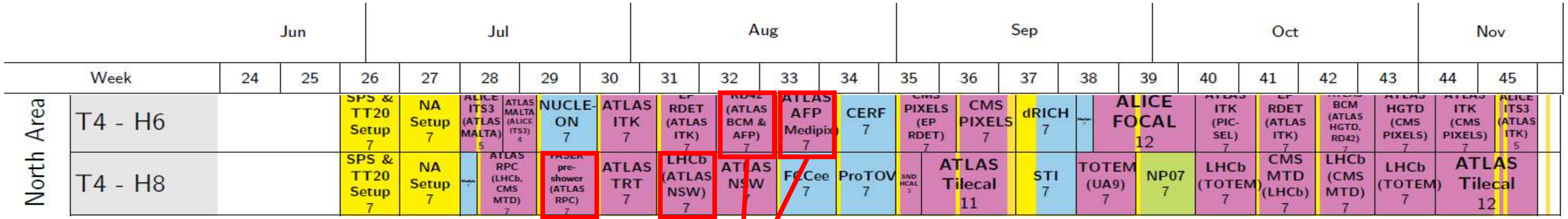
CFD Map, LGAD - Single Pixel 3D (-20°C, 20V)

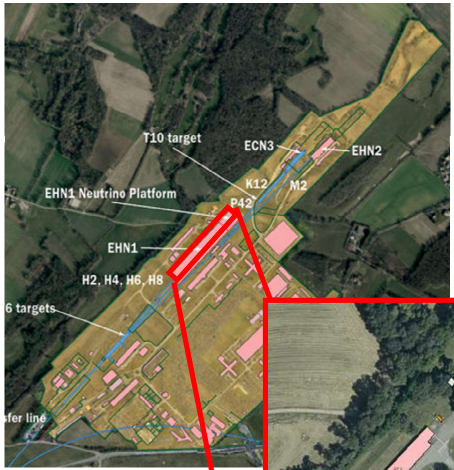


2D optimization plot – 0.5% binning

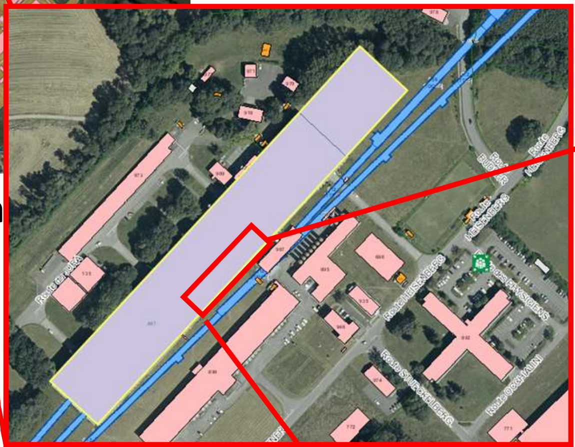
Time Resolution: $$\sigma^2_{tot} = \underbrace{\sigma^2_{timewalk}}_{\sigma^2_{Dist.} + \sigma^2_{Landau}} + \underbrace{\sigma^2_{jitter}}_{\left(\frac{t_{rise}}{S/N}\right)^2} + \underbrace{\sigma^2_{conversion}}_{\left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2} + \underbrace{\sigma^2_{Clock}}_{\text{Fixed Term} \sim 5\text{-}7\,psec}$$

•1st Testbeam – Angle Scan on SPS

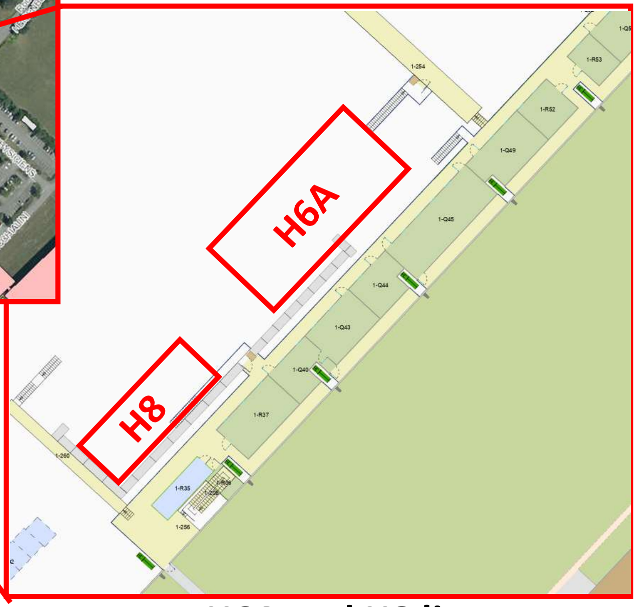




CERN Prevessin



Building 887



H6A and H8 lines

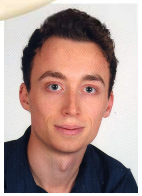
Development phase

- Last minute decision, recovering TimePix 4 slots
- Original plan to test multi-channel boards scrapped due to delays in delivery
- From ground-up development and testing instrumentation, electronics and DAQ software

Data Taking Phase

- Angular incidence scans on single pixel 3D sensors
- +/- 12° range at 1° steps
- Stable operation for the most part

Special thanks to:



Jakob Haimberger

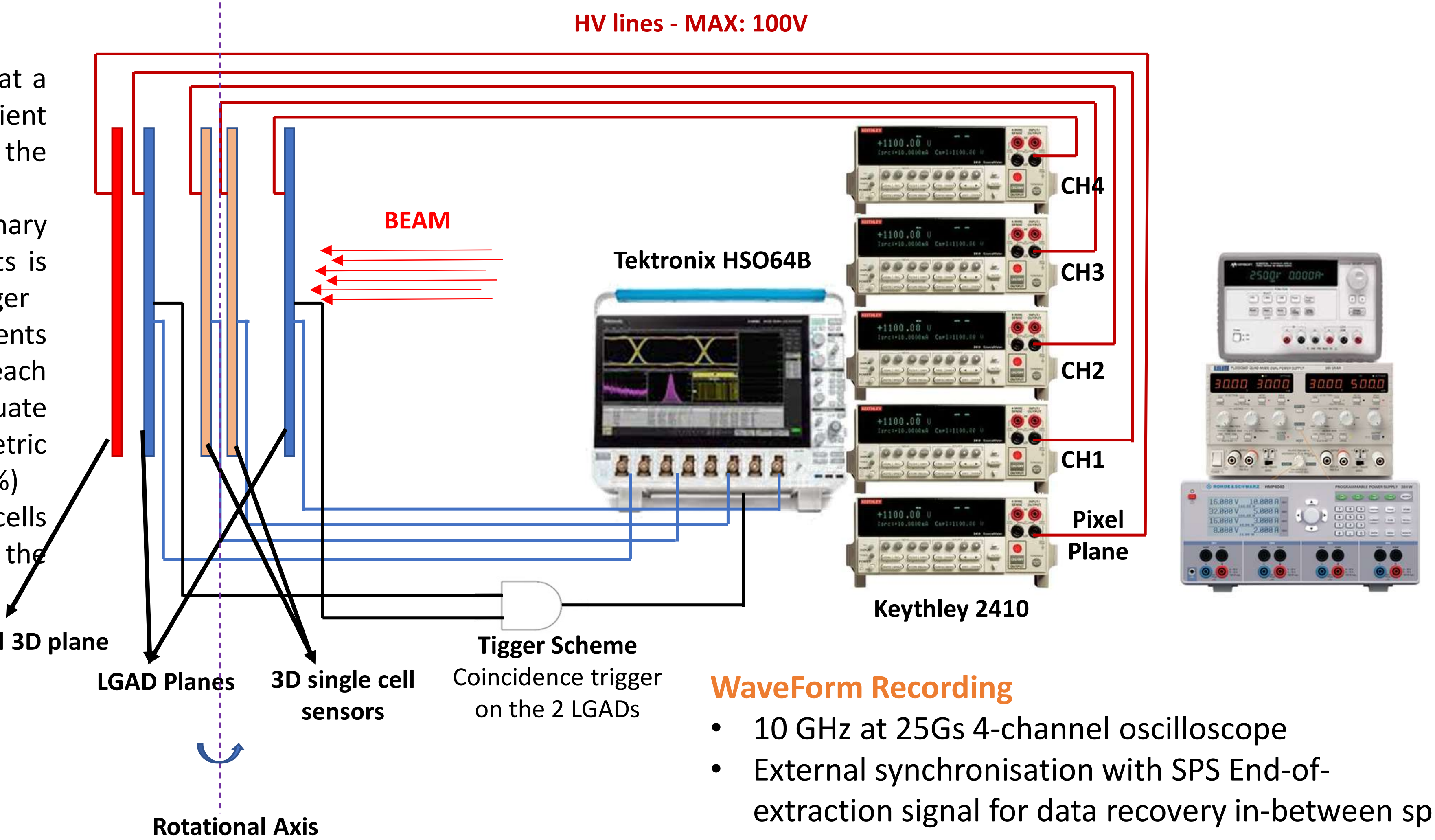
Marius Halvorsen

Daniel Johnson
Laurent Dufour

•1st Testbeam – Setup and Operation

Data Acquisition

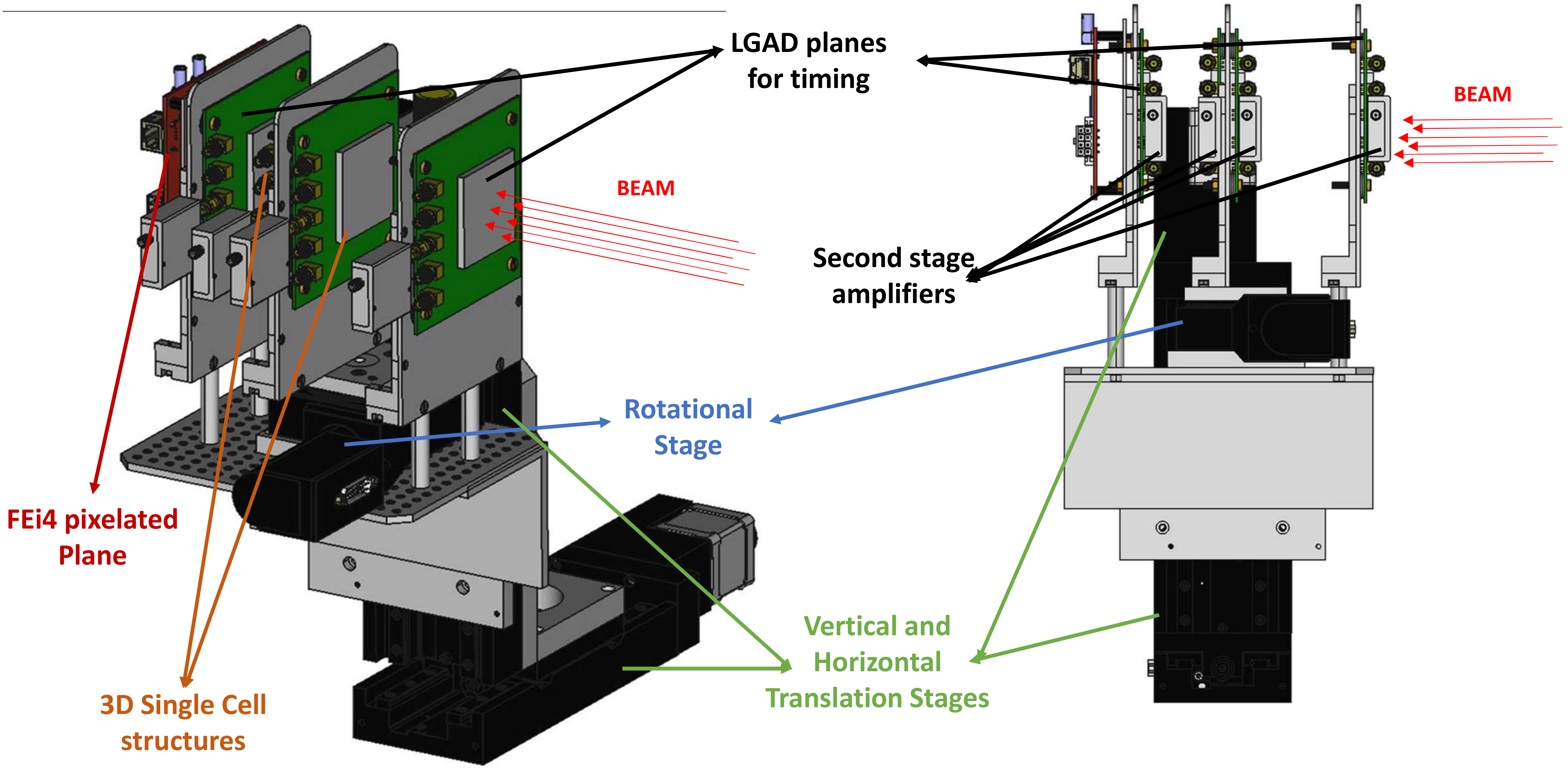
- A coincidence trigger at a known 100% efficient threshold is applied at the 2 LGADs
- RAW waveform binary data of all four objects is recorded for each trigger
- A minimum of 3M events are recorded for each point to ensure adequate statistics (geometric efficiency of 3D ~0.01%)
- Alignment of the 3D cells is verified using the pixelated plane



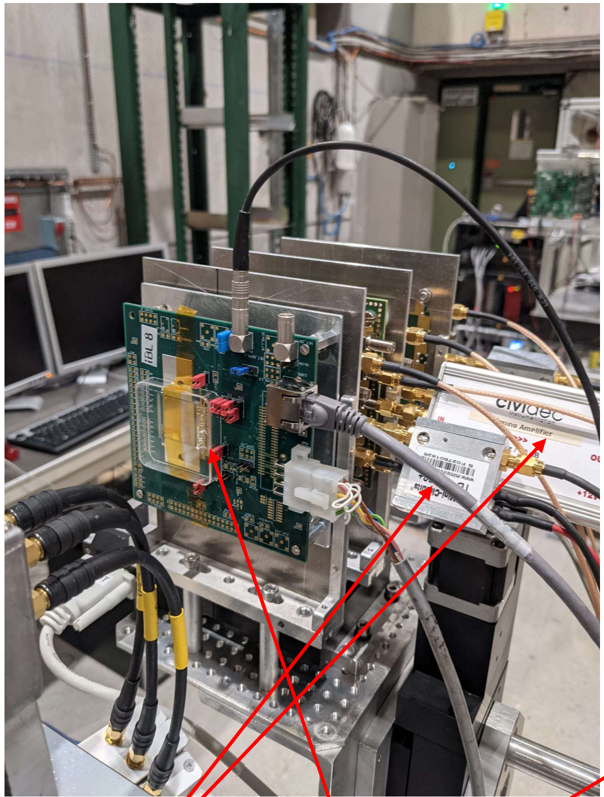
WaveForm Recording

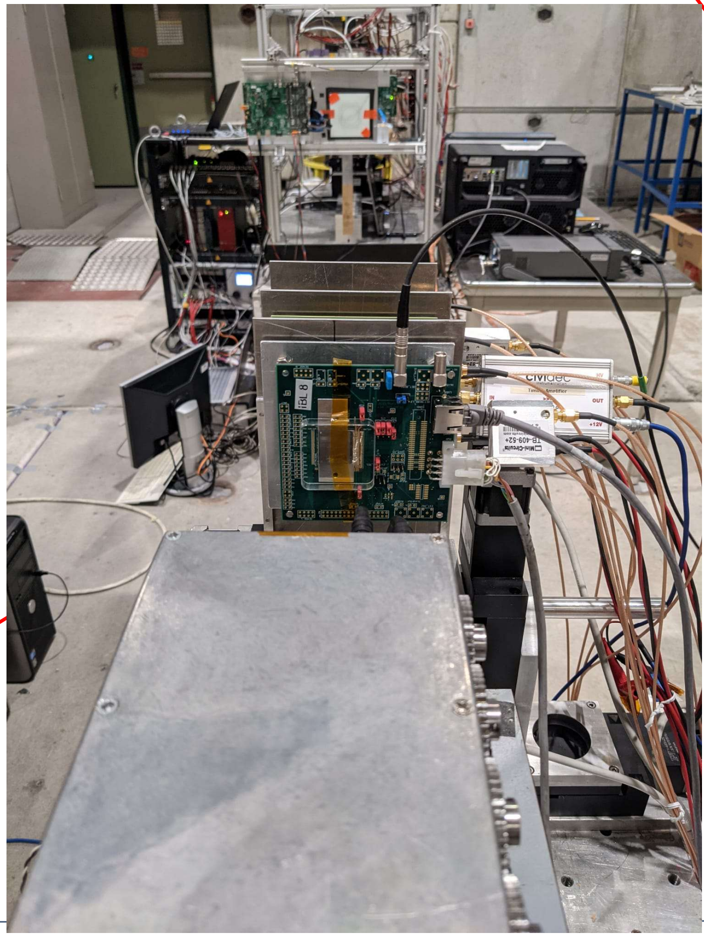
- 10 GHz at 25Gs 4-channel oscilloscope
- External synchronisation with SPS End-of-extraction signal for data recovery in-between spils

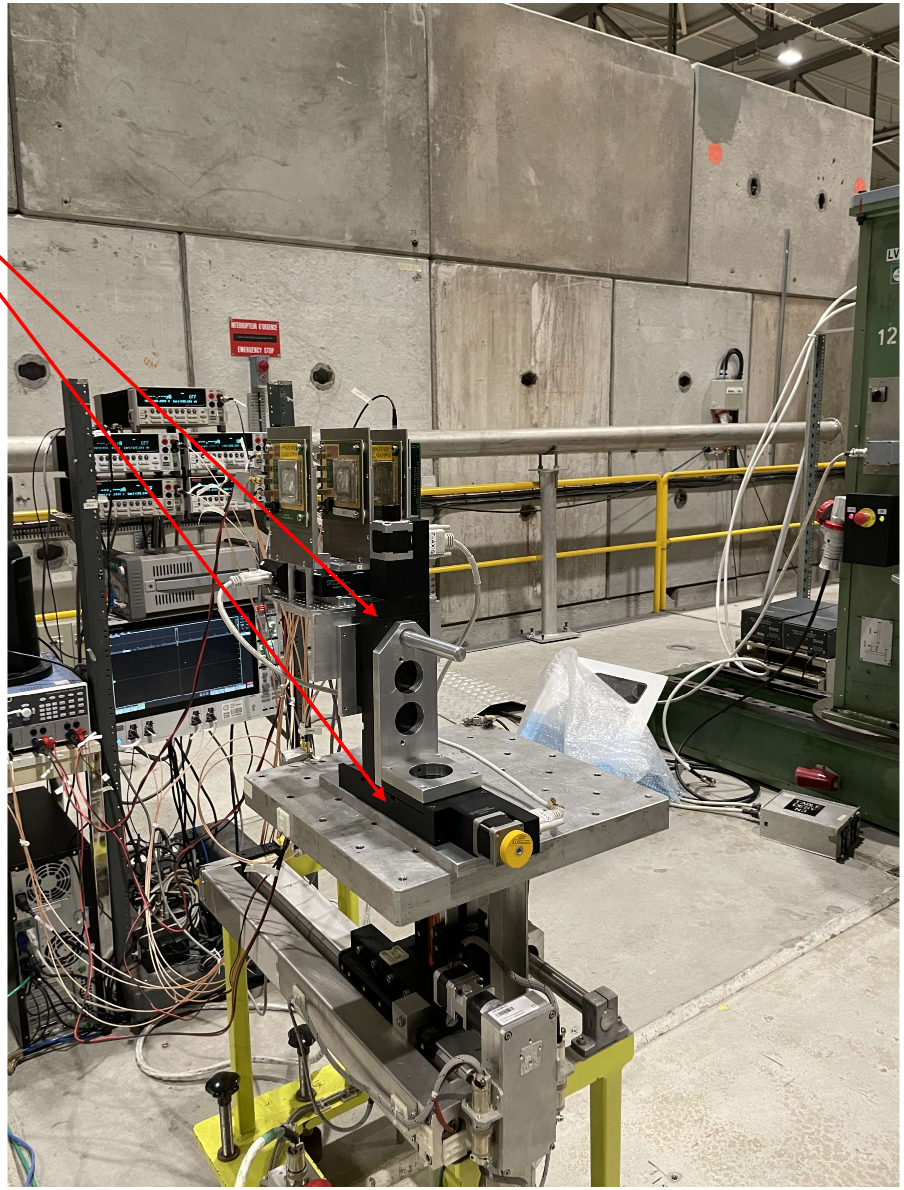
•1st Testbeam – Setup and operation



•1st Testbeam – Setup at H8







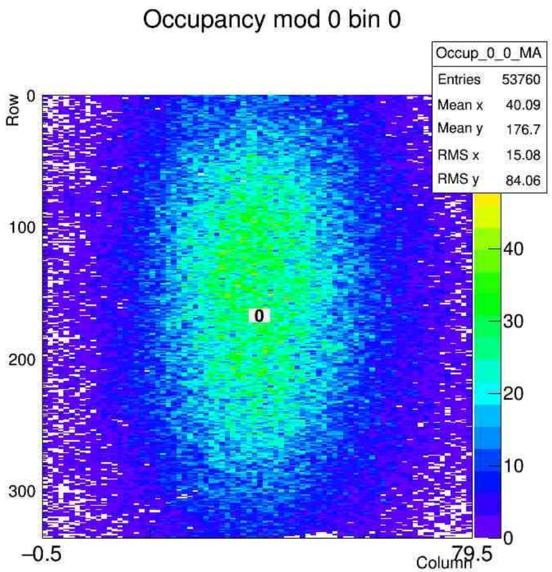
Vertical and Horizontal Stages

Second stage amplifiers

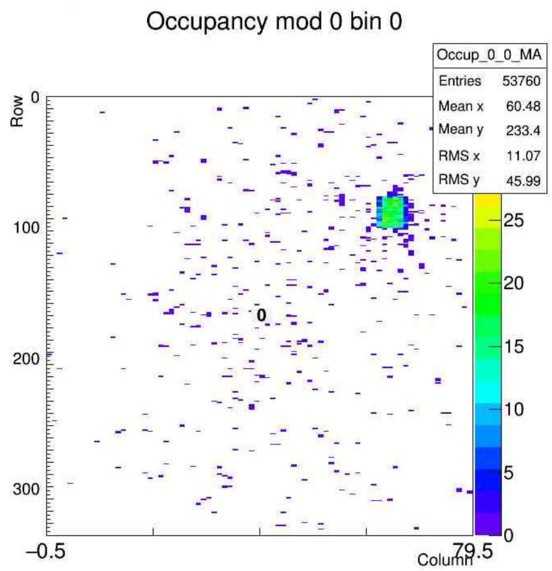
Pixelated plane

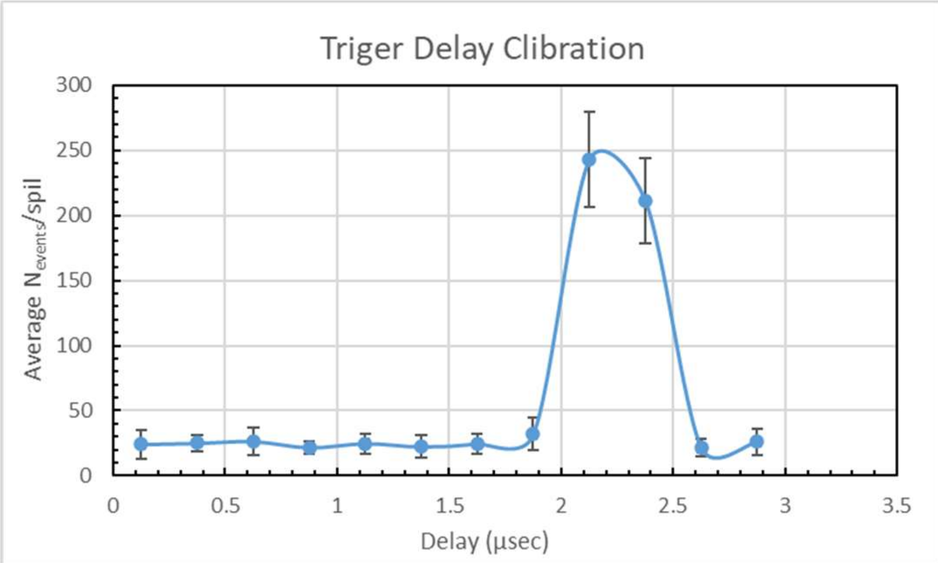
•1st Testbeam – Trigger and ROI calibration

BeamSpot



LGAD 1

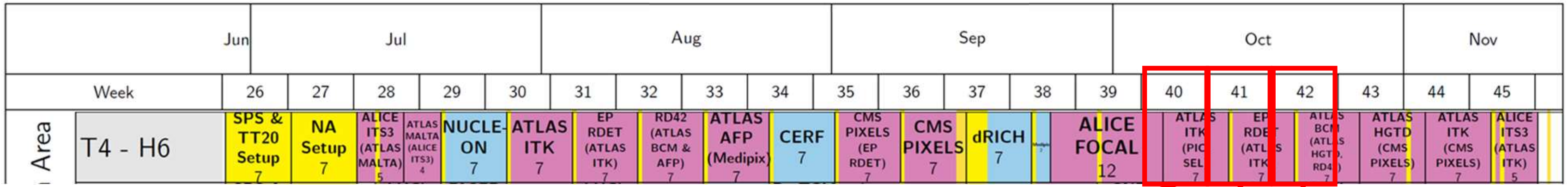




- Trigger delay between FEi4 and Oscilloscope calibrated with an average of 10 spils
- Oscilloscope trigger out used for as HitOr mask fro FEi4
- Average delay ~2.3µsec, FEi4 stores 255 frames with 25nsec distance (40Mhz clock)
- If used as VETO RoI trigger a Gaussian fit can be applied to find the exact frame to read from

•2nd Testbeam – Tracking & Timing

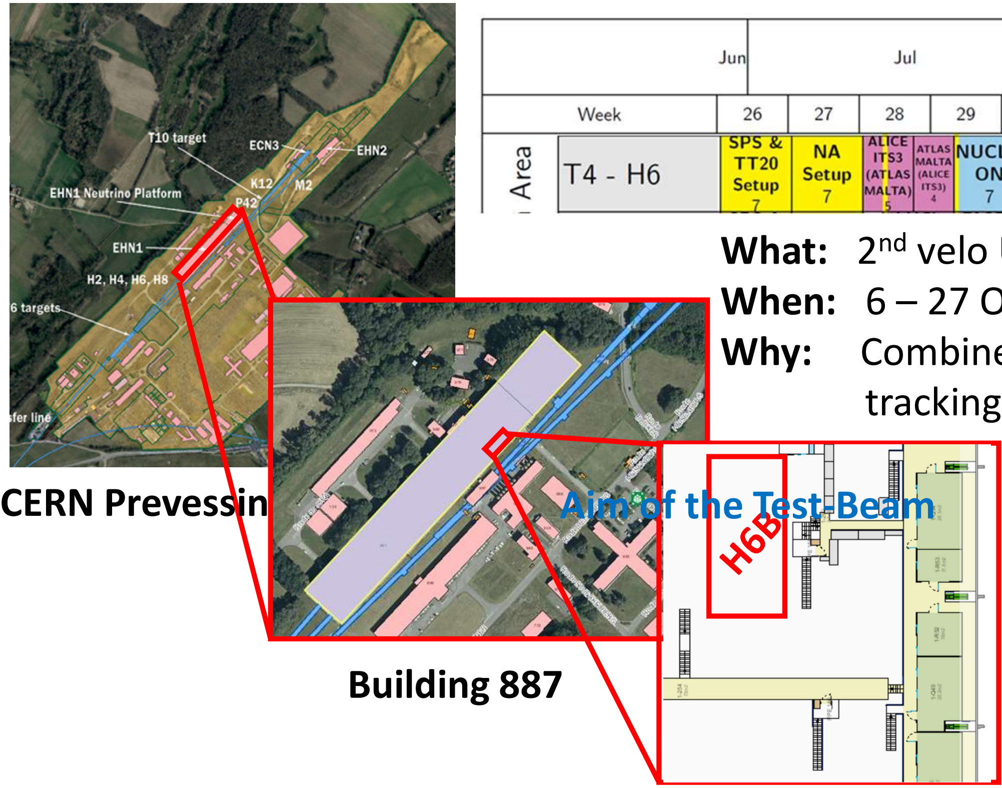
Atlas Forward Proton



What: 2nd velo U2 and EP-R&D test beam

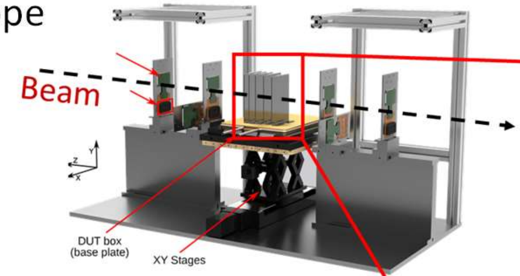
When: 6 – 27 October

Why: Combine picosecond timing with tracking using telescope

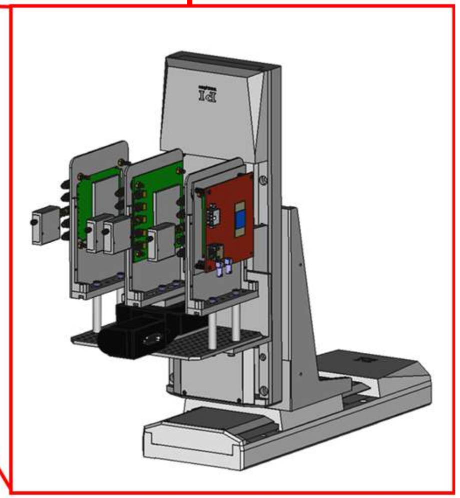


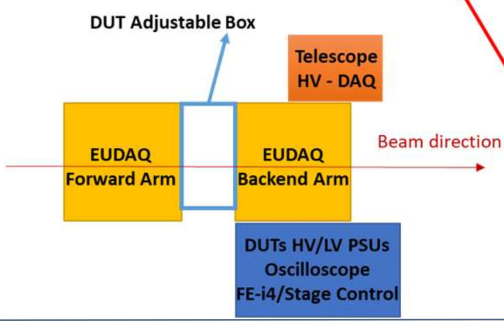
Aim of the Test-Beam

- Single Pixel 50 x 50 µm 3D capable of $< 10^{16} n_{eq}/cm^2$
- Tracking with 7µm position resolution
- Timing with LGAD telescope
- **Study detailed sub-pixel timing map and uniformity**

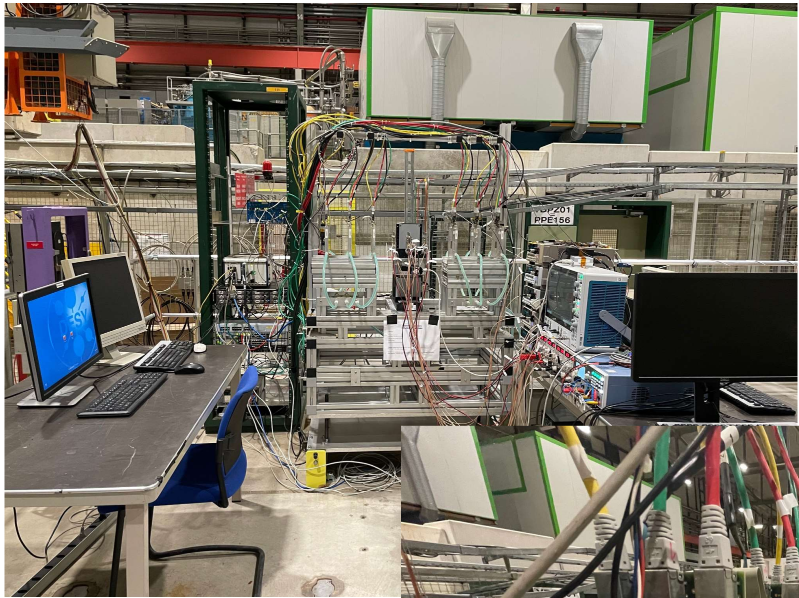


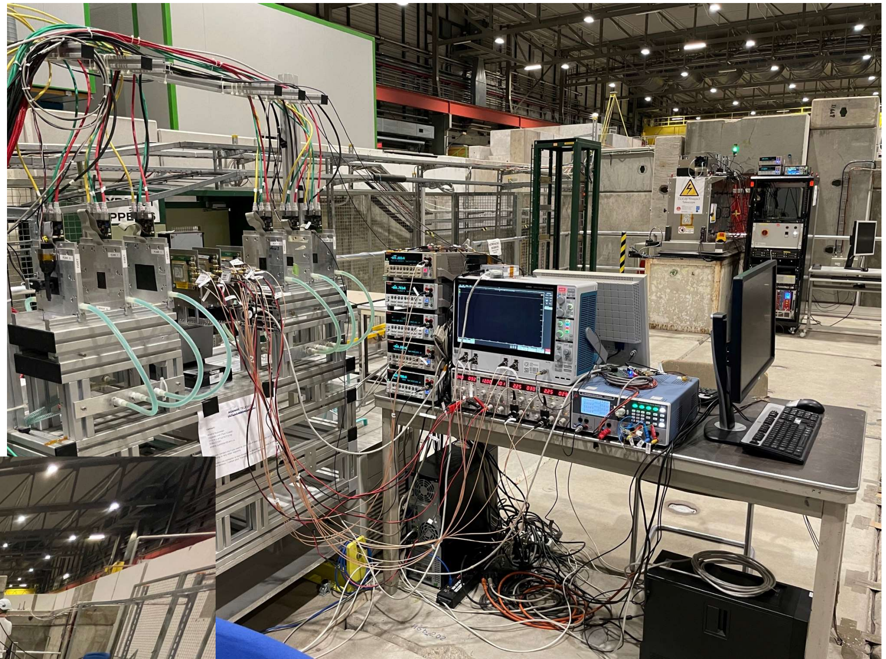
The setup

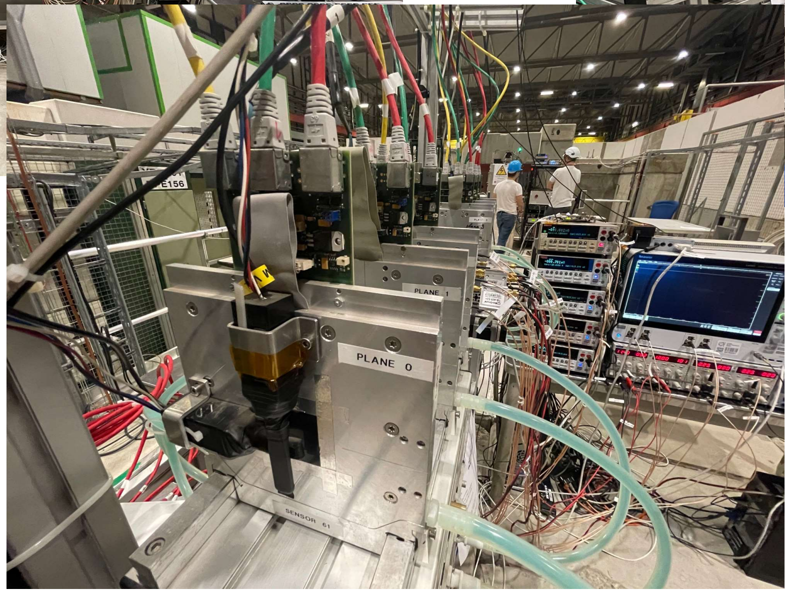




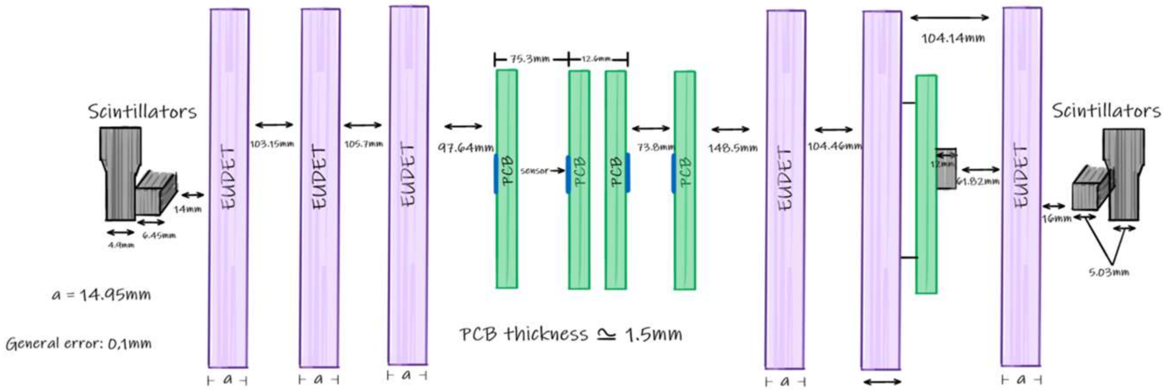
•2nd Testbeam – Tracking & Timing with EUDAQ







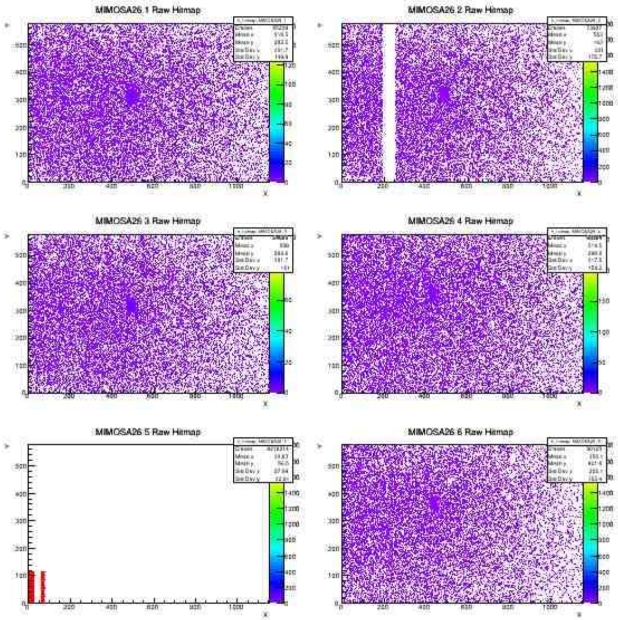
•2nd Testbeam – Tracking & Timing with EUDAQ

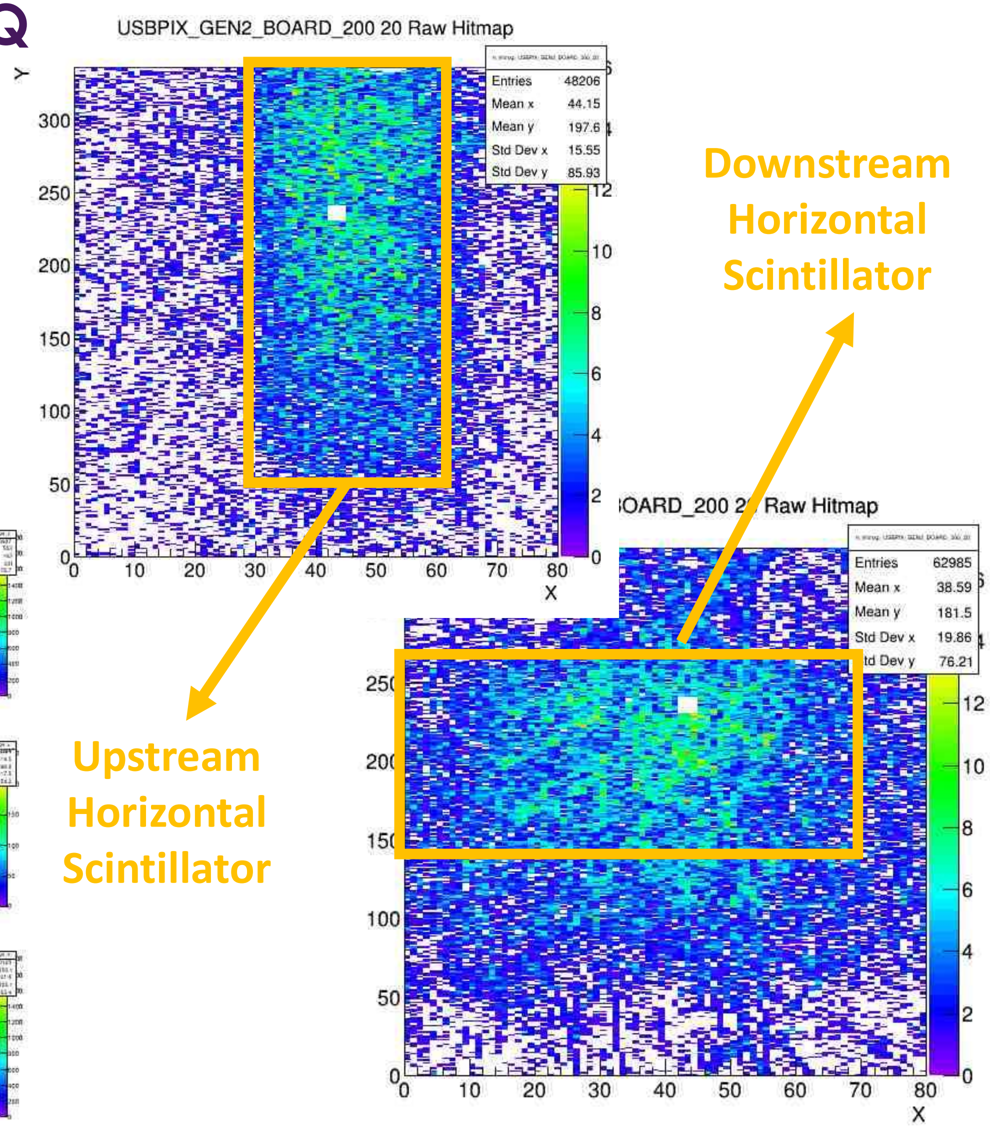


Telescope Planes

- **6 MIMOSA planes for tracking**
- **Plane no. 5 known to be bad**
- **Expected 5μm tracking resolution**
- **Estimated acquired number of events ~1M**

- Limited beam control as parasitic user
- Suffer from low intensity and low data rates of EUDAQ
- Plans to move to TIMEPIX 4

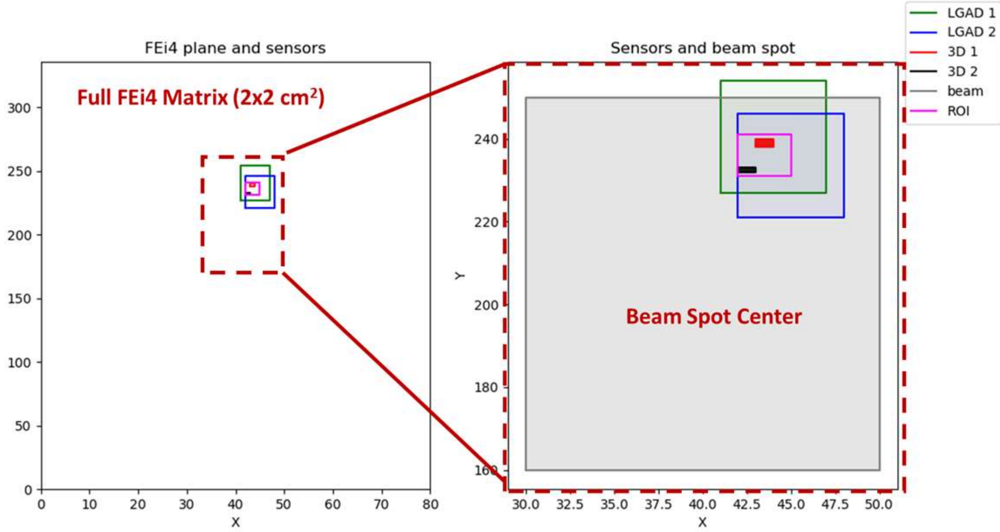




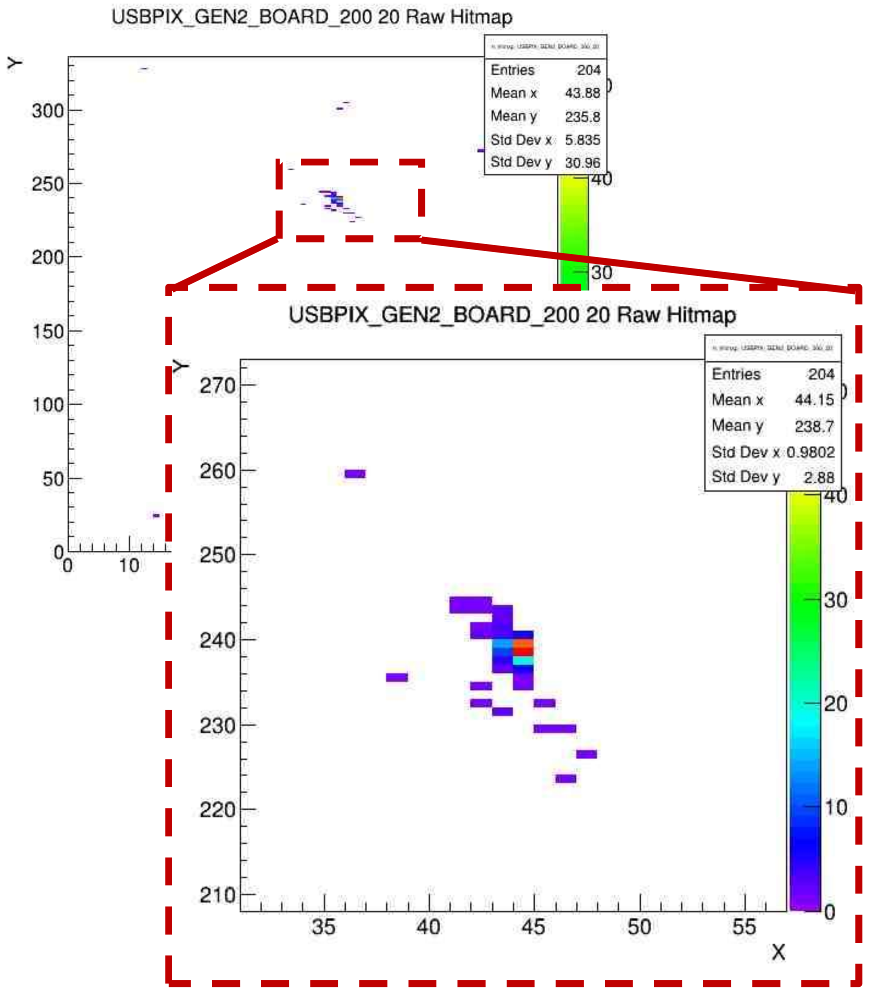
•2nd Testbeam – Tracking & Timing with EUDAQ

LGAD 2 – Downstream (HPK-P2 W25, L17-P12, 1.3 x 1.3mm^2)

LGAD 1 – Upstream (HPK-P2 W25, L17-P11, 1.3 x 1.3mm^2)

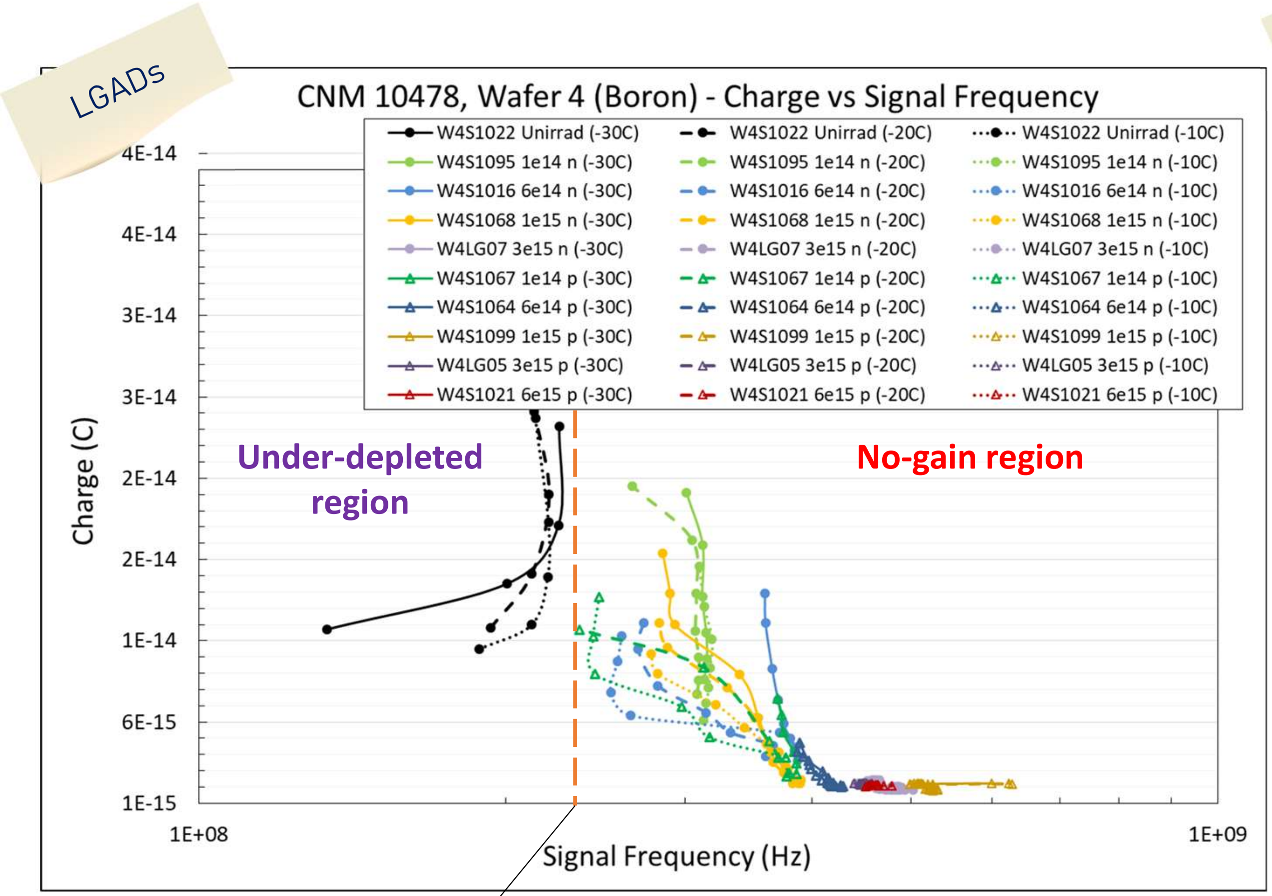


Single pixel 3D (CNM 5936-11, 50 x 50 µm^2)

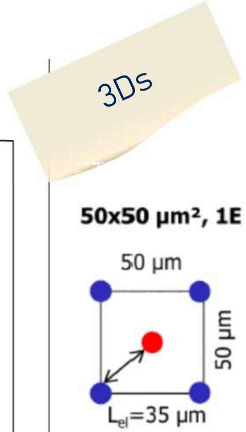


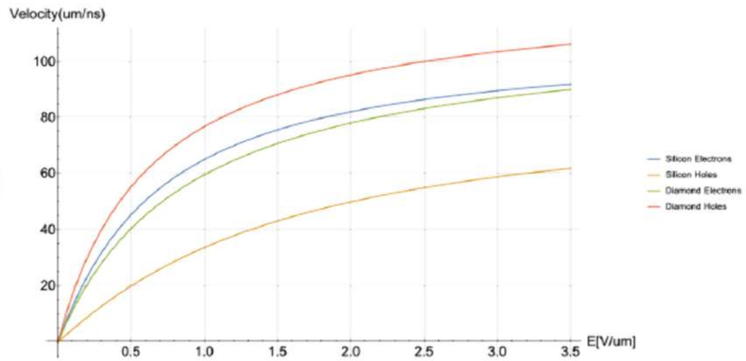
- Extremely small ROI requiring large data taking periods for sufficient statistics
- LGADs used as timing references staggered to limit Active region
- Trigger formation on a coincidence between the scintillators and the ROI
- Efficiency ~20%

•Setup Limitations – UCSC Boards



Asymptotic point ~ 250 MHz





- Assuming a linear filed dependence and a -15 V operation point at 35 µm column distance:
  $$|E| \cong 0.43\ V/\mu m$$
- Estimating drift velocity for electrons:
  $$v^e_{drift} = \frac{\mu_{0,e} \times E}{\left[1 + \left(\frac{\mu_{0,e} \times E}{v^e_{sat.}}\right)^{\beta_e}\right]^{1/\beta_e}}$$
  with $v^e_{sat.} = 107\ \mu m/ns, \mu_{0,e} = 1417 \frac{cm^2}{Vs}, \beta_e = 1.109$
  $$\boldsymbol{v^e_{drift} \approx 41.4\ \mu m/ns}$$
- Extrapolated Rise time and Frequency:
  $$t_{Rise} \approx \frac{1}{3} \times t_s = \frac{1}{3} \times \frac{d/_2}{v^e_{drift}} \approx 140\ psec \Rightarrow \mathbf{2.3\ GHz}$$

•Multi-channel timing Board

Gkougkousis V., Lemos Cid E., EP-R&D meeting July 2021: link

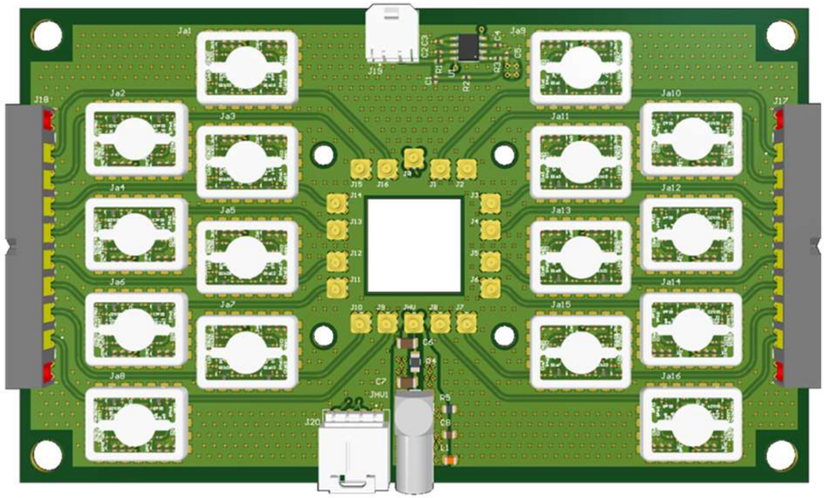
Common emitter single transistor first and second stage charge amplifier

Total Gain: 100 – 40dB

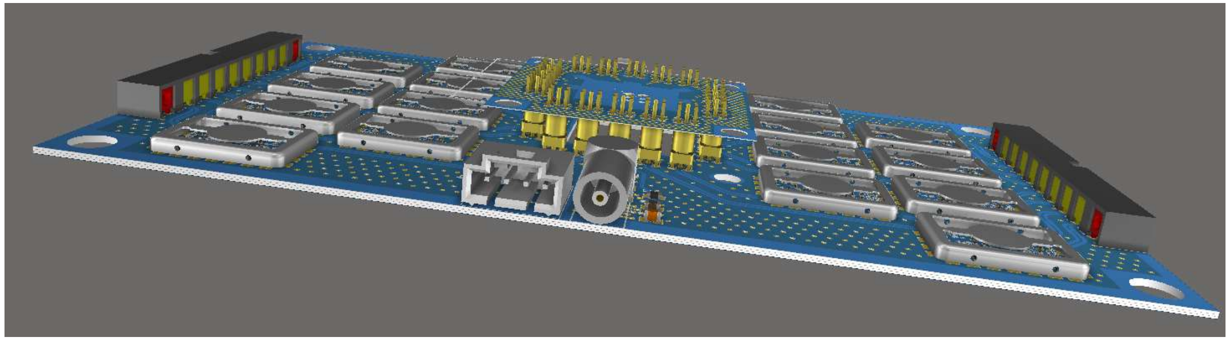
First stage Single Transistor	
Infineon	BFR840L3RHESD
G_{max}	26.5 dB
I_C max	35.0 mA
NF	0.5 dB
OIP3	17.0 dBm
OP1dB	4.0 dBm
V_{CEO} max	2.25 V
Frq. Range	Up to 12 GHz

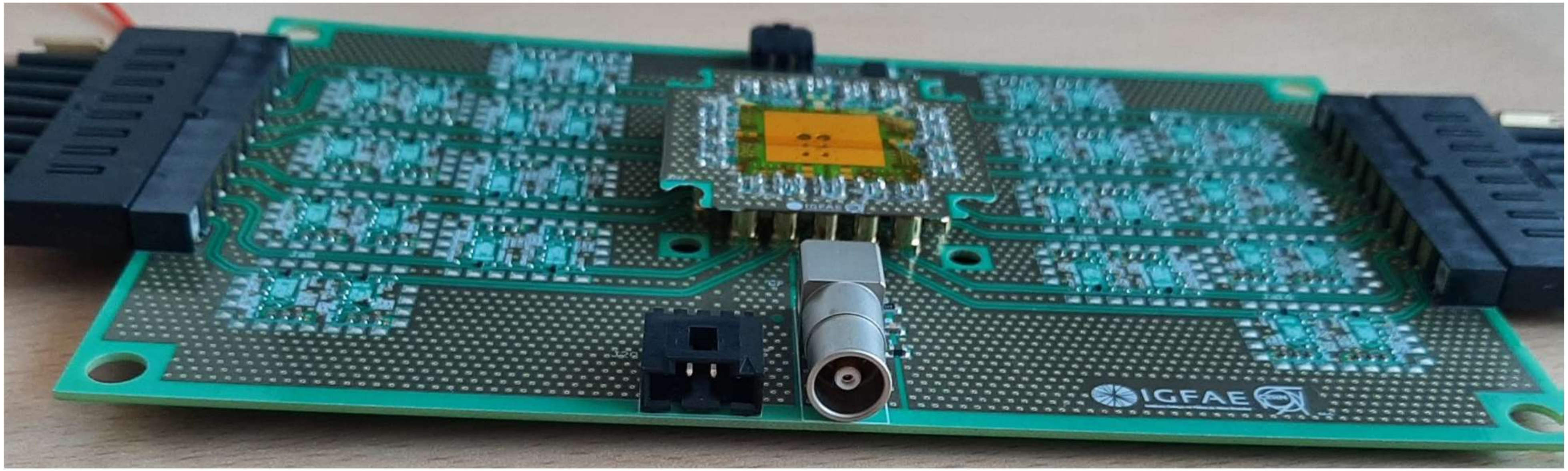
- High Frequency SiGe technology with 75GHz switching frequency
- High frequency design with up to 12GHz
- Low max current (~10mA)
- Well behaved gain linearity vs V_{DD}
- Small packaging with 201-size components for multichannel integration
- Independent Shielding per channel

- 16-channel readout board with integrated first and second stage amplifiers
- Regulated Voltage input
- 15 mm x 15 mm central opening
- 140 mm x 140 mm outer dimensions
- Pre-assembled miniaturized coaxial edge connectors with panel-mounted SMA plugs (1m cable length)
- Vertical miniaturized coaxial plug connectors for sensor board (16 channels + HV/RTD)
- Keyed connectors with high life cycle



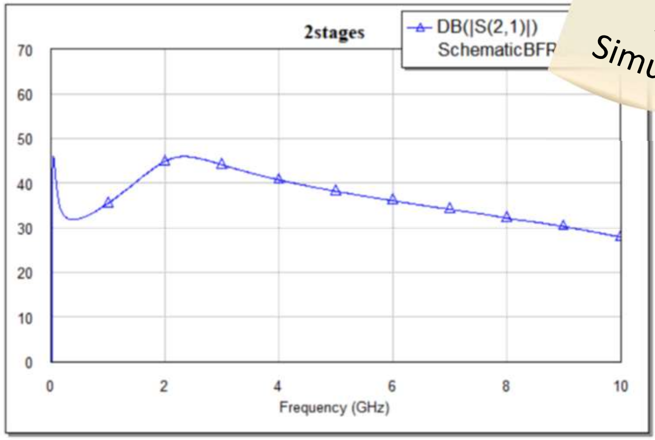
•Multi-channel timing Board – First Prototype





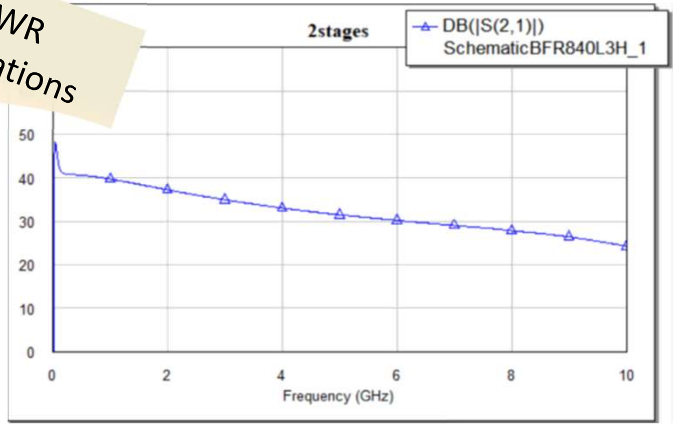
•Multi-channel timing Board – Characterization

Initial design



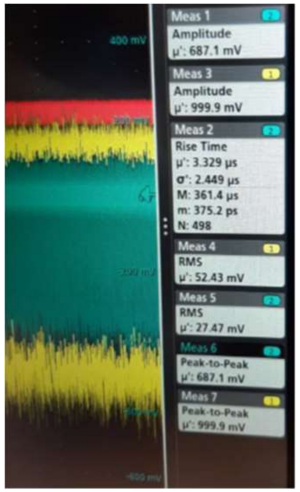
AWR Simulations

Modified –Uniform design

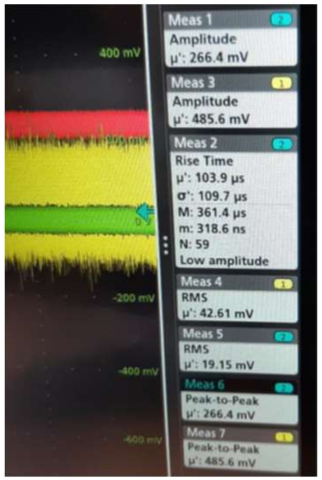


- Optimized design for uniform response with frequency
- No sharp gain change discontinuities
- No undershoot/overshoot observed
- Gain moderated to ~70 for a two-stage configuration
- 20% Higher SNR than UCSC board (with both stages)
- 2 x SNR with respect to UCSC board + niniCircuits second stage amplifier
- On going energy and transimpedance simulation

With signal injection

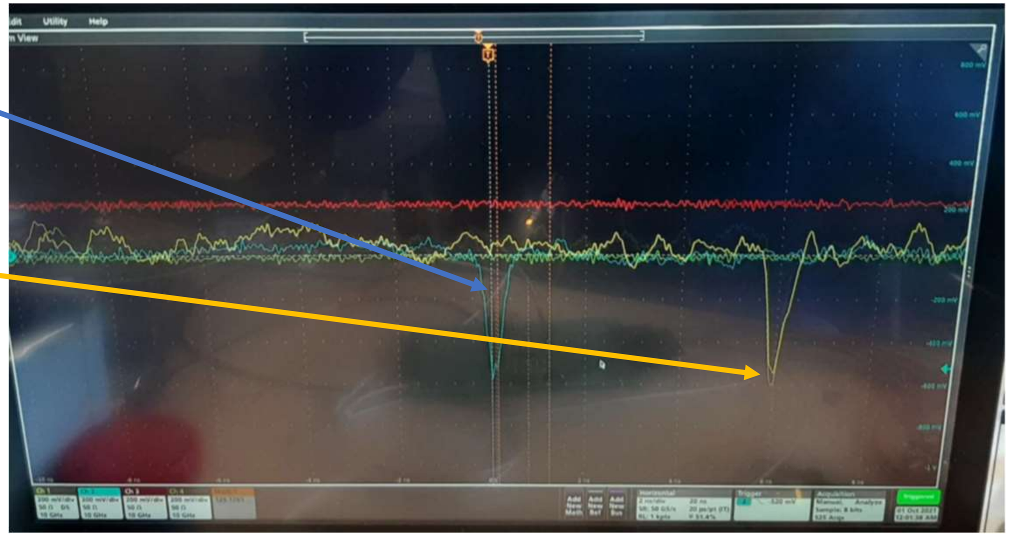


Without signal injection



Blue: 16 channel board

Yellow: UCSC board (only one stage)



•Multi-channel timing Board- Carrier Board

Gkougkousis V., Lemos Cid E., EP-R&D meeting July 2021: link

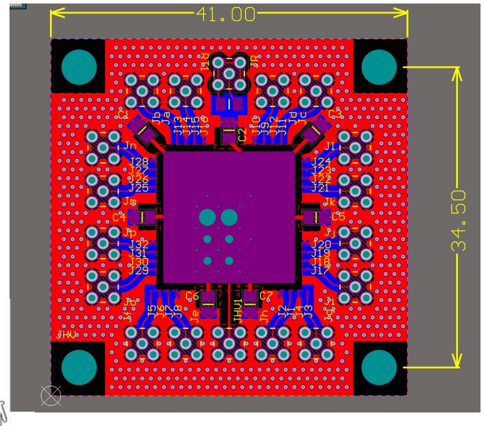
- Quick sensor test turnaround → Group wire-bonding into large batches
- Simplify probing and reduce sensor damage → Needle-less probing
- Batch testing with better control → Unify electrical, timing, laser and charge characterization

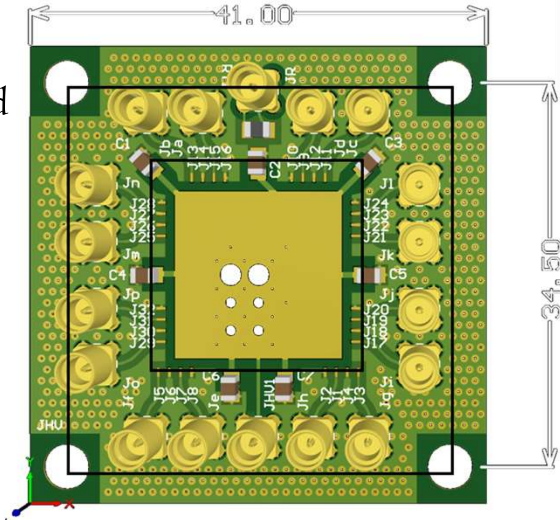
Solution: Develop single sensor carrier board and make all testing structures compatible with it

Requirements

- Simple – cheap design
- Electrically neutral – low noise
- Temperature monitoring
- Compatibility with variety of sensor sizes
- Low material budget
- Easy alignment

✓ 32 x 37 mm rectangular shape
✓ 0.508 mm board thickness
✓ 15 x 15 mm gold plated sensor pad
✓ 2 mm diameter central via
✓ Rogers 4003C HF laminate
✓ 6 passive components per board
✓ 18 mini coaxial connectors (16 channels + HV+ sens)
✓ Integrated RTD





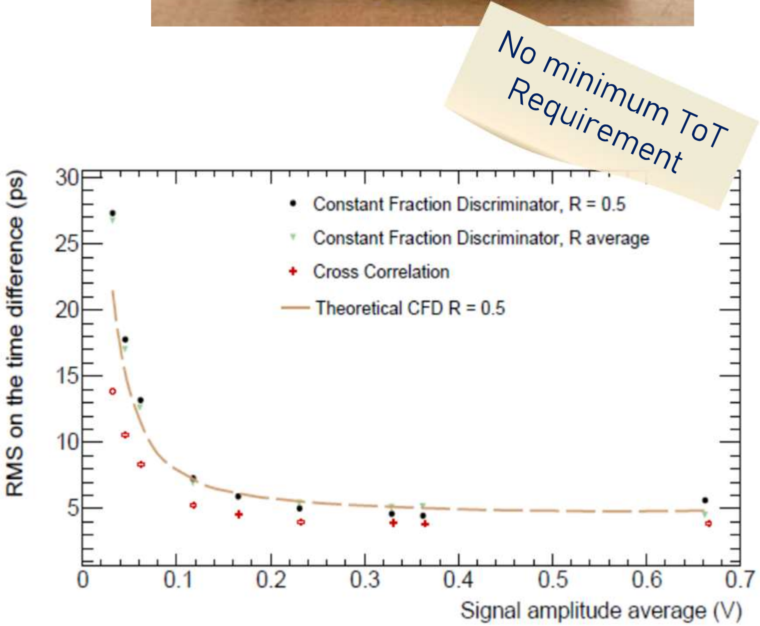
•Multi-Channel DAQ - Sampic

The ASIC (SAMPIC)

- Technology: AMS 0.18µm
- Sampling: between 3 and 8.4 GS/sec on 16 channels (depends on DAC setting)
- 16 channels per chip
- Signal Bandwidth of 1.6GHz
- Discrimination noise 2 mV, chip noise < 1.3 mV RMS
- Max input Signal: 1V unipolar (0.1V to 1.1V)

ADC

- 8 to 11 bit Wilkinson ADC at 1.3GHz
- Upon triggering 64 samples digitalized in parallel per channel
- Resolution adjustment possible to improve timing by reducing bit count
- Time resolution between 5 ps (calibrated) and 15ps (uncalibrated)



Calibration

- Calibration files provided for all operational points of the ADC
- Channel by channel calibration to be performed by user
- 64 channels x 4 operation points = 256 calibration runs

Connectivity

- USB2.0 + LabWindows based software (provided)
- UDP Based Ethernet, direct PC connection – no router support

•Sampic Test Runs

Time Resolution

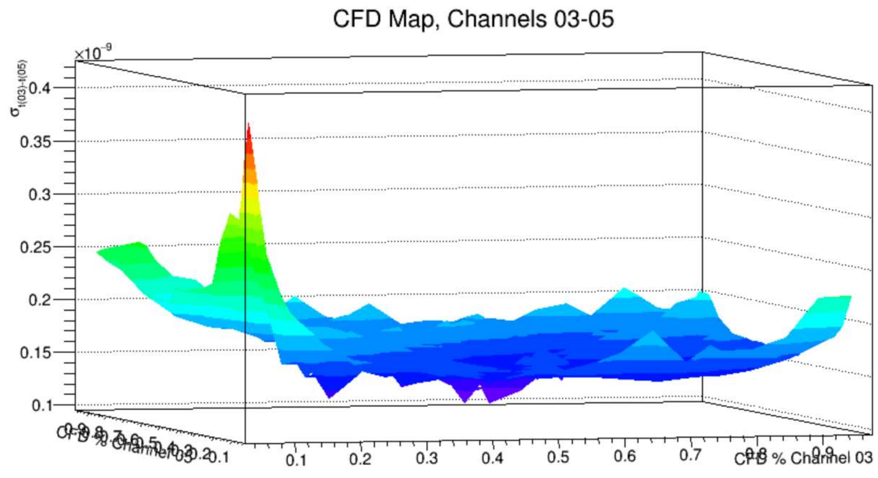
Obtained with: LGADUtils
https://gitlab.cern.ch/egkougko/lgadutils

Both methods give similar results:

- Linear fit 5% - 95% analysis on rising edge
- Results may be improved by global fit on pulse shape
- Not more than 10 % - 20 % expected improvement

Trigger:

- Self trigger on either channels
- No coincidence implementation
- No internal buffer, no opportunity for combined trigger with tracker
- Only independent operation possible



2 LGAD Run	
Time resolution	78 psec (60 psec with oscilloscope)
Sampling Frequency	6.2 Gs/s

2 LGAD Run	
Registered Events	2698
Coincidences	2967
Efficiency	99.98 %
Thresholds	10 mV
Trigger Mode	Self Trigger

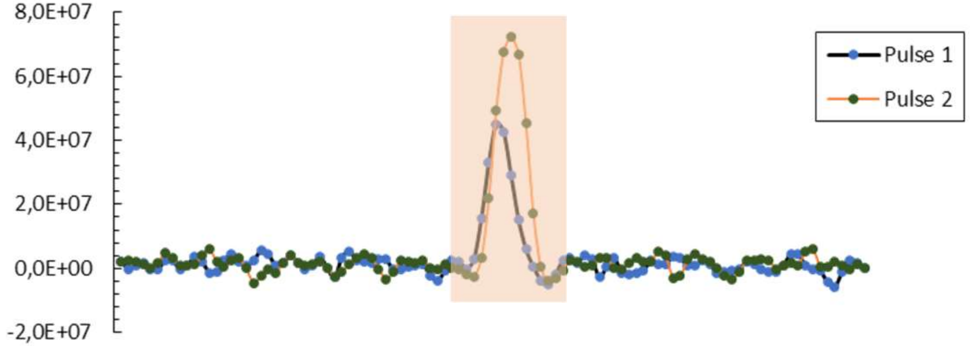
•Conclusions

Outlook and Plans

- 1st Lab timing measurements presented and look extremely promising
- 2 Testbeam campaigns completed with tracking and results soon to be published
- **A new multi-channel (x16) versatile board has been developed and is at the final stages of testing, suitable for 3D and planar timing applications**
- 3 more test beam campaigns planned for 2022 with EUDAQ – **We are open to partnerships!!**
- **Non-irradiated 3D studies are completed, sensors are being currently irradiated up to 1e17 with protons and neutrons**
- New production planned for mid-2022, tender will be out soon and we invite ALL producer to participate

•Backup

•Backup – FFT analysis



Discrete FFT Resolution

$FFT_{Res} = {F_s}/{N}$

Sampling Frequency

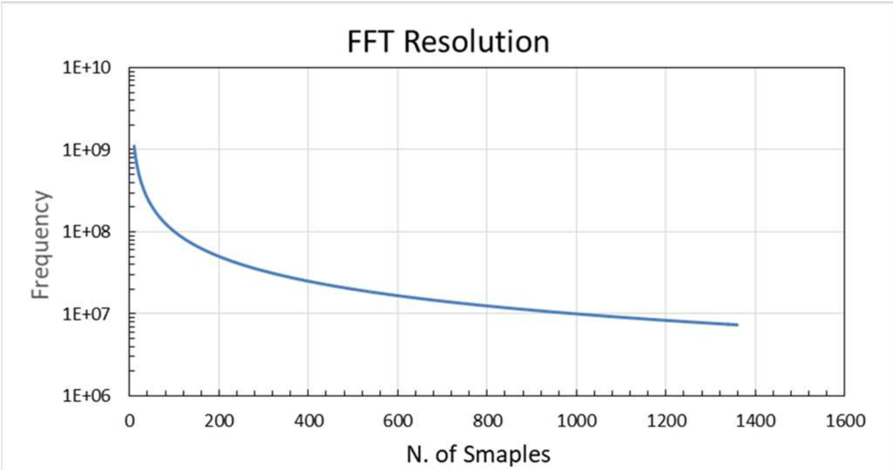
Number of Samples

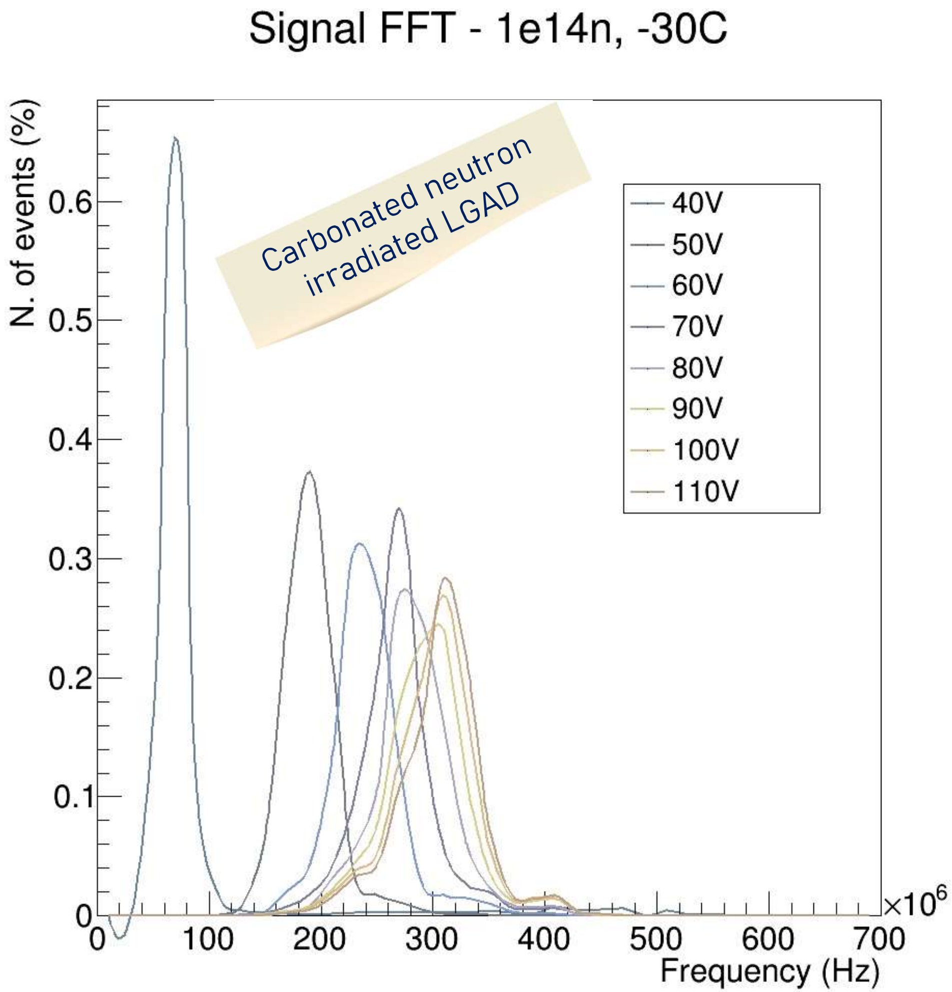
Fixed sampling rate

but

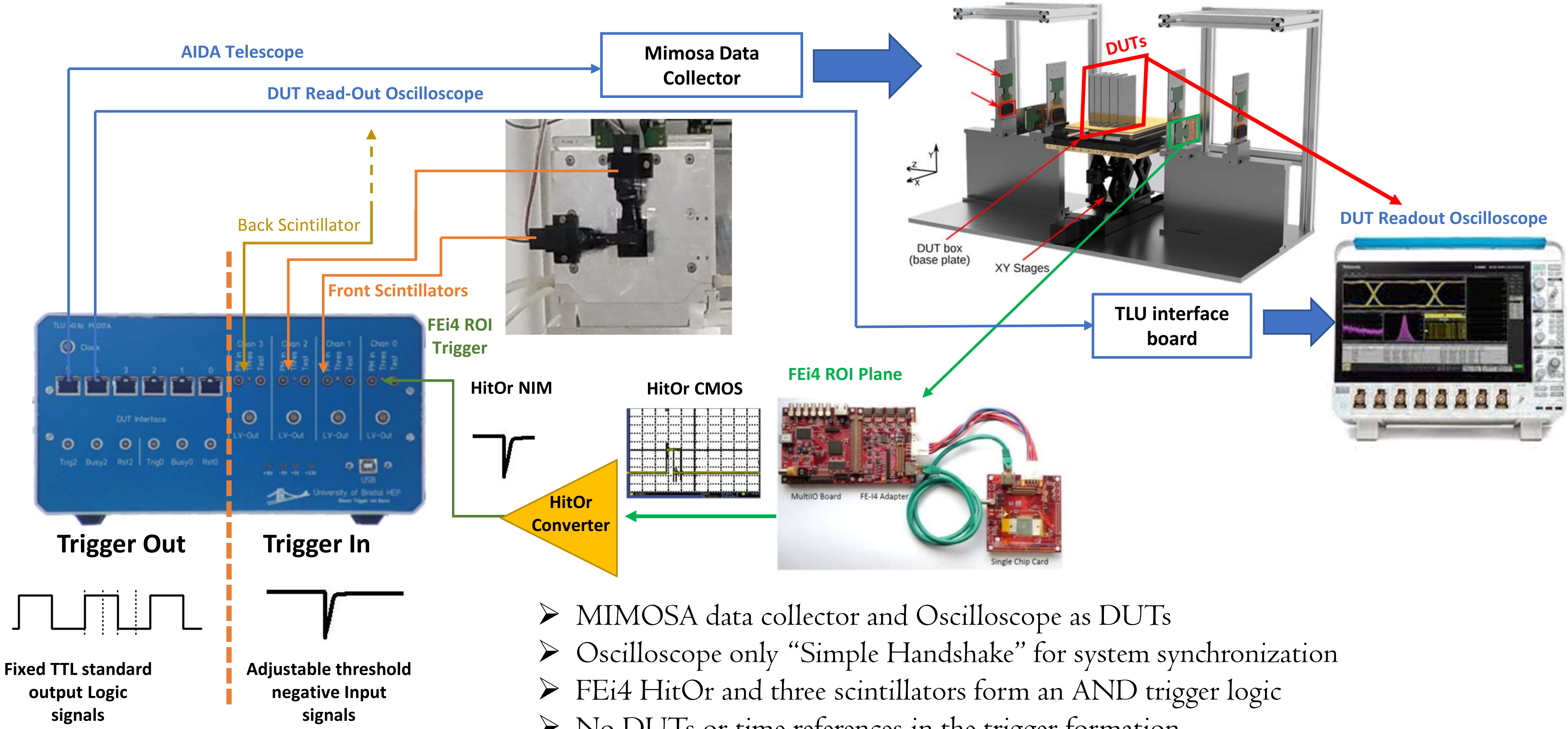
Variable sample size

Variable resolution → Non – standard bin size - Renormalization





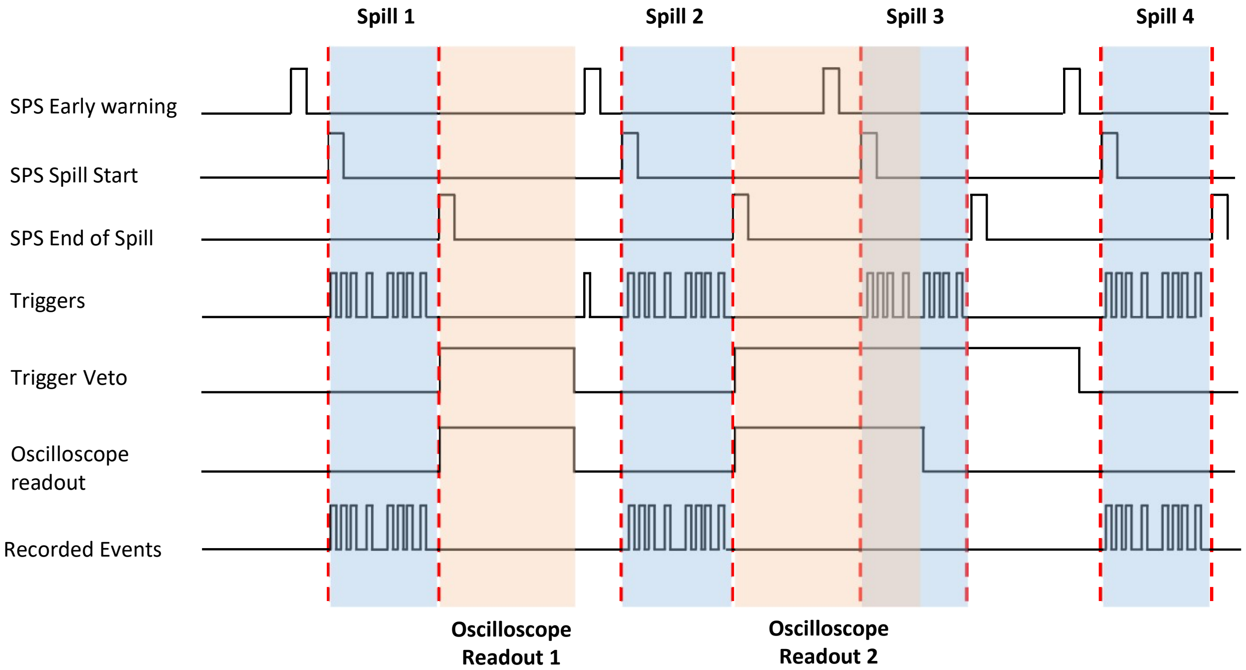
•Backup - Trigger Scheme

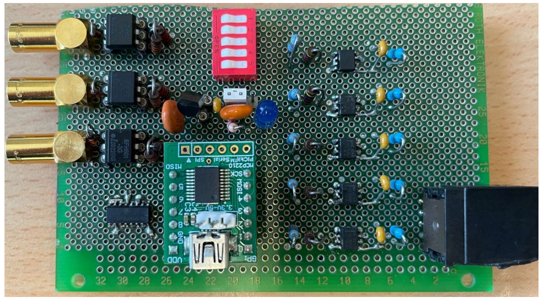


- MIMOSA data collector and Oscilloscope as DUTs
- Oscilloscope only "Simple Handshake" for system synchronization
- FEi4 HitOr and three scintillators form an AND trigger logic
- No DUTs or time references in the trigger formation

•Backup - Interface board

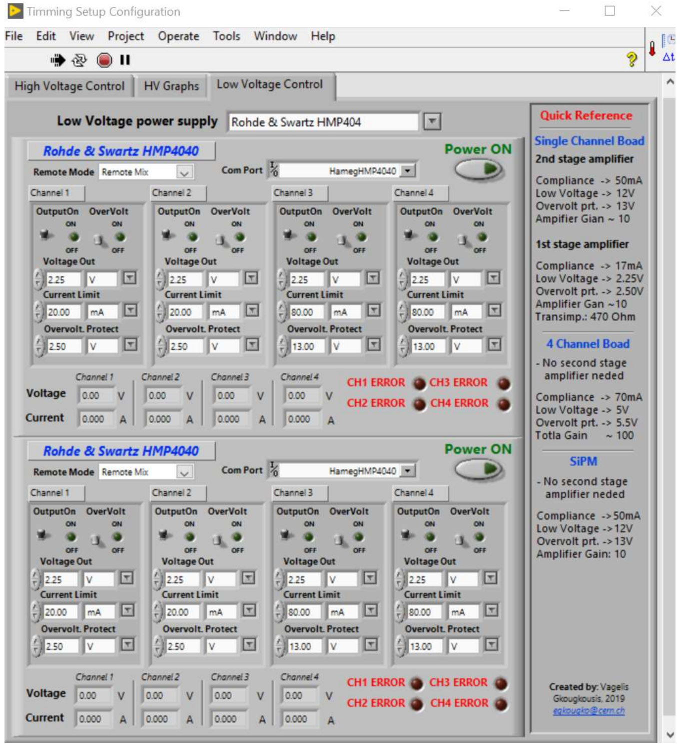
Trigger Interface Board



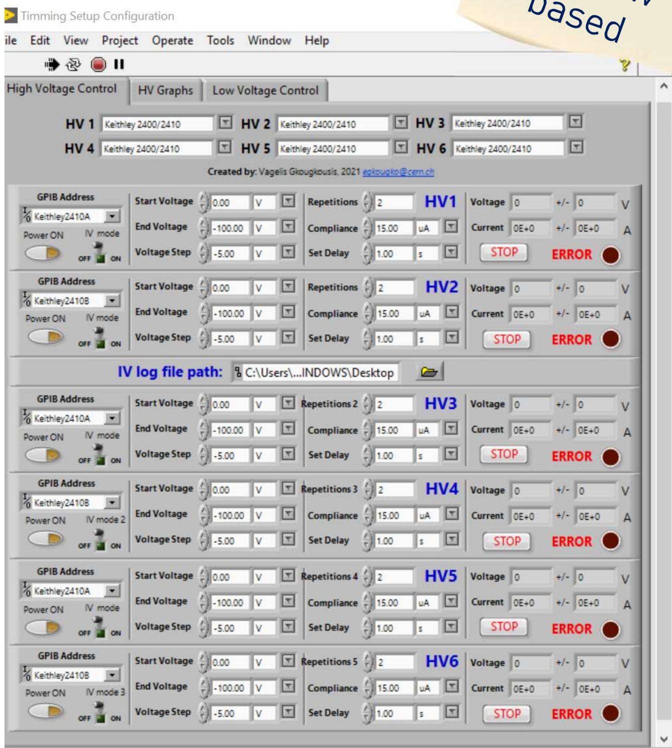


- ➢ Monitor SPS end of spill and SPS early wanting
- ➢ Only readout Oscilloscope between spills
- ➢ Use LVDS to TTL EUDAQ interface board
- ➢ Controlled via USB though character device drivers on oscilloscope DAQ PC

•Backup - HV & LV slow control

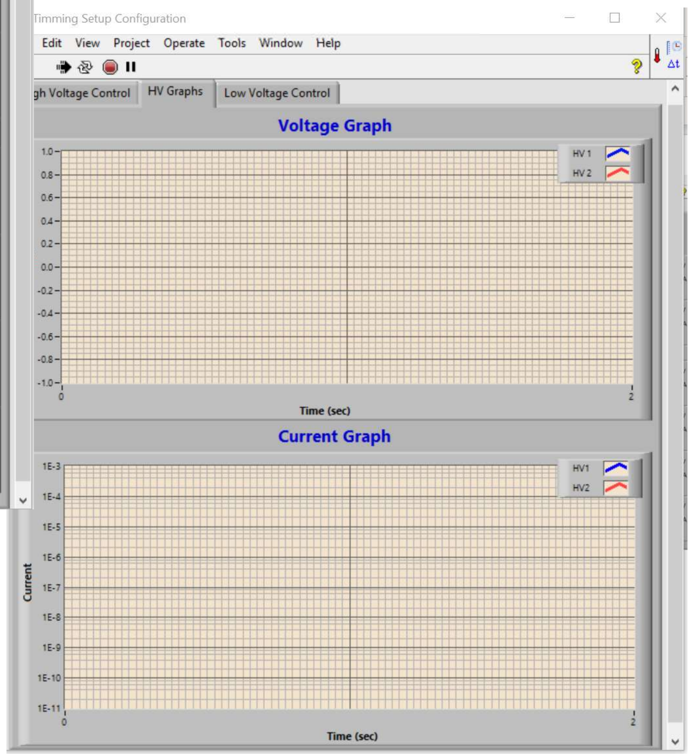


Labview based



High voltage

2400/2410 series



Supported Low Voltage Power supplies

363X series | 364X series | HMP4040 | PL330DP | PL303QMD

- 8x HV channels
- 8x LV channels
- Constant monitoring & logging
- Live protection