SINTEF

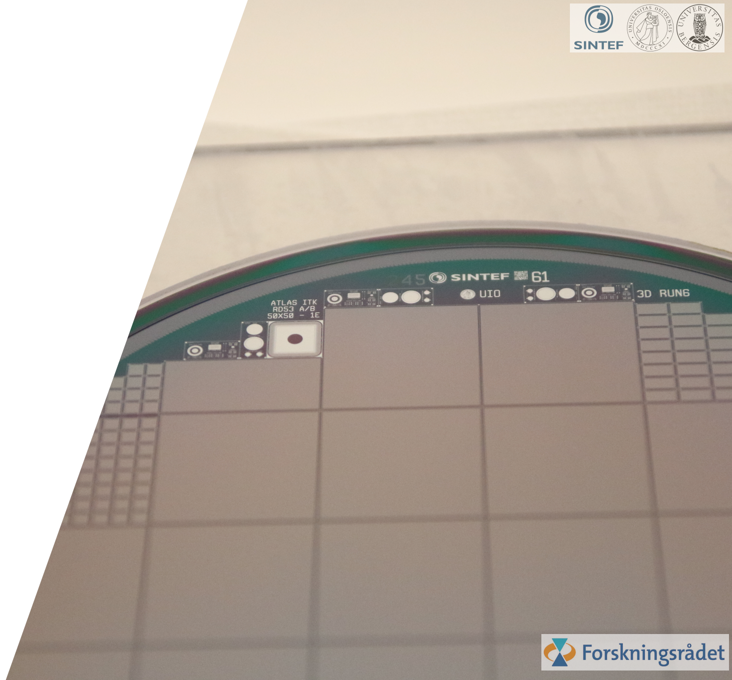
SINTEF 3D pixel sensor pre-production for the ATLAS ITk

Marco Povoli [1] O. Koybasi [1] A. Kok [1]
A. Summanwar [1] O. Rohne [2]
O. Dorholt [2] A. L. Read [2]
H. Sandaker [2] A. L. Heggelund [2]
B. Stugu [3] S. K. Huiberts [3]
M. E. Lauritzen [3] A. Traeet [3]

[1]SINTEF MiNaLab, Oslo, Norway
[2]University of Oslo, Norway
[3]University of Bergen, Norway

17th (Virtual) "Trento" Workshop on Advanced Silicon Radiation Detectors

University of Freiburg, 2-4 March 2022.



SINTEF

Outline

1. Introduction
2. Electrical tests results on temporary metal
   - Full batch yield
   - Planar test structures
   - 3D test structures
   - 3D pixel detectors
   - Effect of sintering - estimation
3. Lessons learned
   - Deep Reactive Ion Etching - DRIE
   - Wafer bowing/warping
4. Conclusion and future plans

SINTEF

Forskningsrådet

Recent history of 3D technology at SINTEF

YEAR	Project	Wafer type	Active thickness [µm]	Electrode diameter [µm]	Remarks
2006	Run-1	4" SOI	230	15	N-type, low mechanical yield
2008	Run-2	4" SOI	230	15	50% yield (roughly)
2010	Run-3	4" SOI	230	15	Low yield (2 out of 24 wafer ok)
2018	Run-4*	6" Si-Si	50 & 100	4	Very good yield (FE-I4 layout)
2019	Run-5*	6" Si-Si	150	6	OK yield (RD53 A/B with active edge)
2021	**Run-6***	**6" Si-Si**	**150**	**6**	**Completed Feb. 2021. ATLAS pre-production. (RD53 A/B with common layout with FBK, slim-edge termination)**

*funded by Norwegian ATLAS R&D

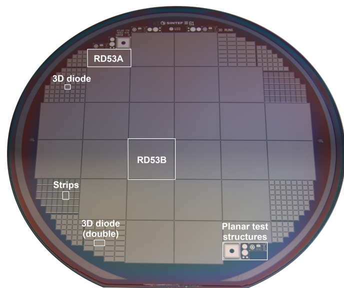
SINTEF

Forskningsrådet

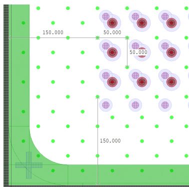
SINTEF

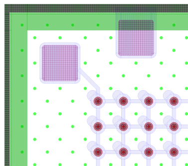
Fabricated wafers

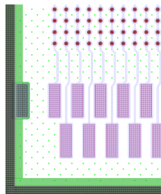
Pixel layout - $50\mu m \times 50\mu m$ - 1E configuration

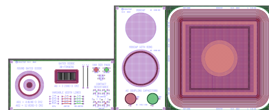


- 24 wafers, 6” Si-Si p-type (ICEMOS **150μm active**)
- 2 test wafers, 6” Si-Si p-type (PiKEM/INSETO (UK) **150μm active**)
- **Slim-edge** (ohmic column ’fence’), **3D electrodes** (6μm diameter)
- **Depth:** N-type electrodes **115μm**, P-type electrode **150μm**
- All processing steps in-house except the **p-spray** implant
- P-spray dose **increased** in this run
- Layout performed at SINTEF in collaboration with FBK and CNM
- Common layout with FBK (6” wafers)





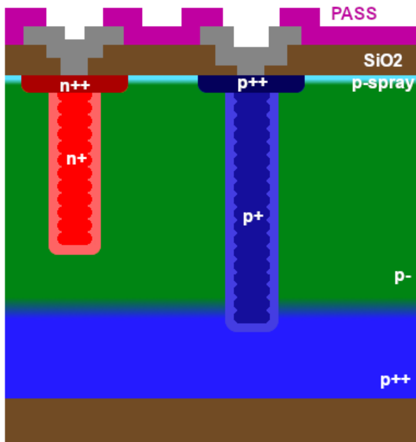




Forskningsrådet

SINTEF

3D RUN6 - Fabrication process

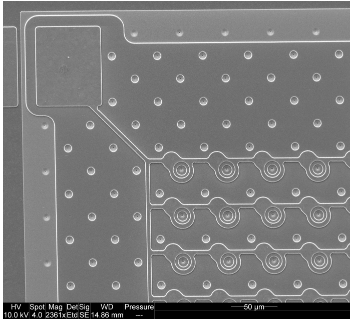


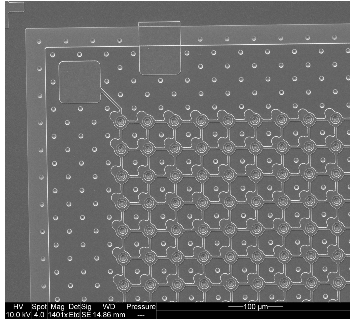
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling
5. Planar n+ doping
6. Repeat steps **'2-5'** for p+ columns (Boron)
7. Contact opening
8. Temporary metal deposition and patterning
9. **TEMP METAL MEASUREMENTS**
10. Temporary metal removal and cleaning
11. Final metal deposition, patterning and **sintering**
12. **Passivation** deposition and patterning
13. Final baking if necessary

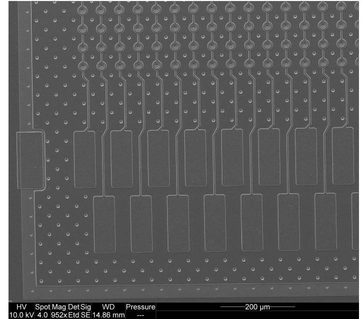
→ **60 main steps! 10 months of net processing**

SINTEF
Forskningsrådet

Temporary metal test results

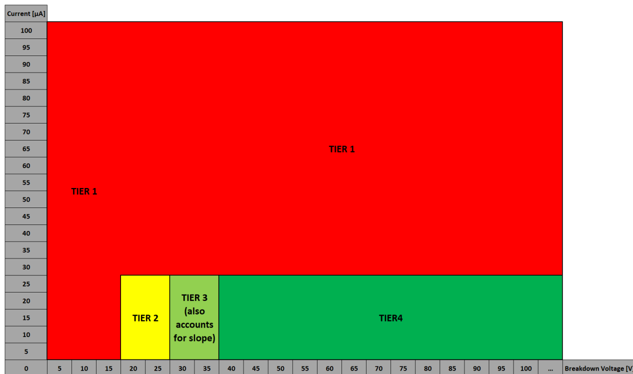






TEMP METAL deposited on thermal oxide, biasing both N+ and P+ from the front!

Selection criteria for yield calculation



Specifications given in the tender:

- $C_{pix} < 100pF$ (from C-V of 3D diode) ✓
- $V_{depl} < 10V$ (from C-V of 3D diode) ✓
- $V_{BD} > V_{depl} + 20V$ ✓
- SLOPE: $\frac{I_{LK}(V_{depl}+10V)}{I_{LK}(V_{depl}+5V)} < 2$ ✓
- $I_{LK}(20^\circ C) < 2.5\mu A/cm^2$
- Chuck temperature on automatic prober is $24^\circ C$ (current increase of a factor ∼1.5)
- Measurements performed before SINTERING and PASSIVATION!
- The distance between the metal and the SiO_2/Si interface is smaller and the surface is not fully terminated ⇒ expected higher current

Forskningsrådet

SINTEF

3D RUN6 - Fabrication YIELD

RD53B pixel detectors MEASURED BEFORE SINTERING

				TIER1	TIER2	TIER3	TIER4	TIER4	TIER4+3	TIER4+3+2
WAFER #	Thickness [µm]	SENSOR TYPE	# of sensors	BAD	MARGINAL	GOOD	BEST	YIELD STRICT	YIELD SOFT	YIELD VERY SOFT
G17	150 + 500	RD53B	24	1	0	2	21	87.50 %	95.83 %	95.83 %
G15	150 + 500	RD53B	24	3	0	1	20	83.33 %	87.50 %	87.50 %
G11	150 + 500	RD53B	24	4	0	1	19	79.17 %	83.33 %	83.33 %
G14	150 + 500	RD53B	24	3	1	1	19	79.17 %	83.33 %	87.50 %
G7	150 + 500	RD53B	24	3	0	3	18	75.00 %	87.50 %	87.50 %
G18	150 + 500	RD53B	24	3	0	3	18	75.00 %	87.50 %	87.50 %
G1	150 + 500	RD53B	24	2	1	4	17	70.83 %	87.50 %	91.67 %
G12	150 + 500	RD53B	24	6	0	1	17	70.83 %	75.00 %	75.00 %
G16	150 + 500	RD53B	24	4	2	1	17	70.83 %	75.00 %	83.33 %
G20	150 + 500	RD53B	24	6	1	0	17	70.83 %	70.83 %	75.00 %
G21	150 + 500	RD53B	24	3	0	4	17	70.83 %	87.50 %	87.50 %
T2-2	150 + 500	RD53B	24	6	0	1	17	70.83 %	75.00 %	75.00 %
G5	150 + 500	RD53B	24	7	0	1	16	66.67 %	70.83 %	70.83 %
G19	150 + 500	RD53B	24	6	0	2	16	66.67 %	75.00 %	75.00 %
G22	150 + 500	RD53B	24	8	0	0	16	66.67 %	66.67 %	66.67 %
G2	150 + 500	RD53B	24	5	2	2	15	62.50 %	70.83 %	79.17 %
G24	150 + 500	RD53B	24	9	0	0	15	62.50 %	62.50 %	62.50 %
G4	150 + 500	RD53B	24	3	1	6	14	58.33 %	83.33 %	87.50 %
T2-1	150 + 400	RD53B	24	6	1	3	14	58.33 %	70.83 %	75.00 %
G3	150 + 500	RD53B	24	6	0	5	13	54.17 %	75.00 %	75.00 %
G6	150 + 500	RD53B	24	7	1	3	13	54.17 %	66.67 %	70.83 %
G8	150 + 500	RD53B	24	7	2	3	12	50.00 %	62.50 %	70.83 %
G9	150 + 500	RD53B	24	7	2	3	12	50.00 %	62.50 %	70.83 %
G13	150 + 500	RD53B	24	10	0	2	12	50.00 %	58.33 %	58.33 %
G10	150 + 500	RD53B	24	9	0	4	11	45.83 %	62.50 %	62.50 %
G23	150 + 500	RD53B	24	21	3	0	0	0.00 %	0.00 %	12.50 %
		RD53B TOT.	624				TOT.	63.46 %	72.44 %	75.16 %

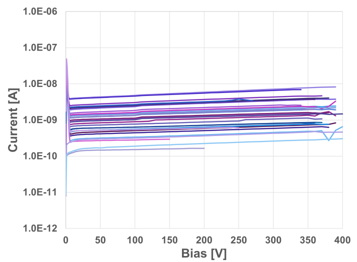
- Better yield than previous run
- **T2-1** and **T2-2** comparable or better than the rest
- Other interesting wafer are **G23** and **G24** (more on this later…)
- Leakage current still a bit high (more on this later…)
- Yield calculated with a relaxed spec on leakage current for now…

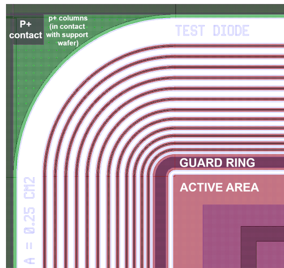
Forskningsrådet

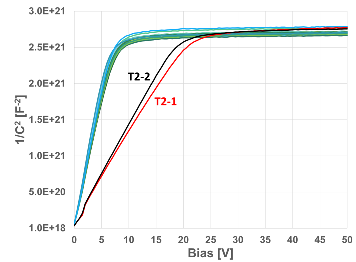
SINTEF

I-V of planar test diodes

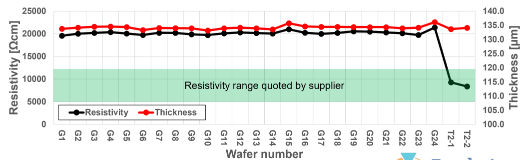
Measured before sintering







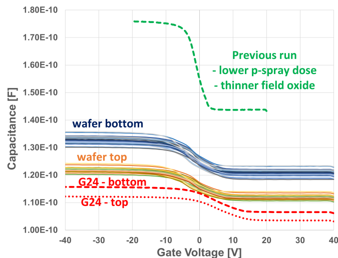
- Breakdown voltages around **350 V**, (p-spray dose increased in RUN6)
- Average current value **before sintering** equal to **1 nA** (corresponding to life times of roughly **6 ms**)
- C-V measurements show saturation at **10 V** (ICEMOS) and **20 V** (PiKEM, INSETO) (difference in resistivity)
- Saturation value of the C-V curves suggests an **effective active volume thickness** of $135 \mu m$
- Boron diffusion from the support wafer results in a loss of active volume (doping profile measured on RUN5 wafers)

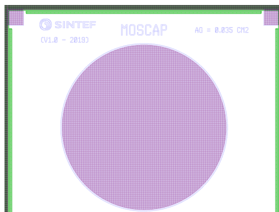


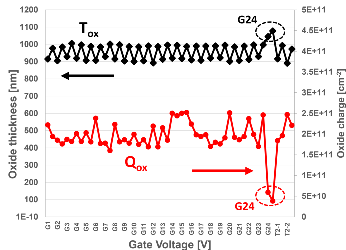
Forskningsrådet

MOS Capacitor C-V

Measured before sintering





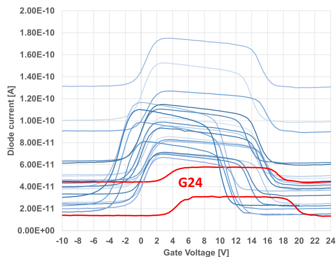


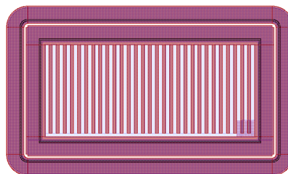
- Loss of **oxide thickness** during processing was greatly reduced (compared to RUN5)
- Slight **difference** in T_{ox} between **top** and **bottom** part of the wafer (not critical)
- Extracted values:
  - $T_{ox} = 950\ nm$
  - $Q_{ox} = 2 \times 10^{11}\ cm^{-2}$
- Higher p-spray dose results in 'stretching' of the C-V curves
- Expected decrease in oxide charge after sintering
- Wafer **G24 lower oxide charge**

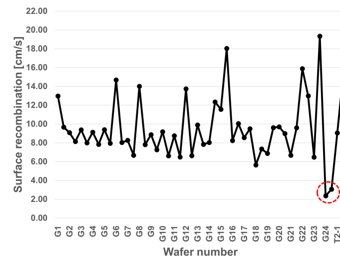
Forskningsrådet

Gated Diode

Measured before sintering



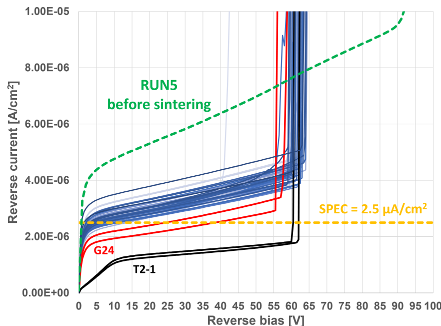




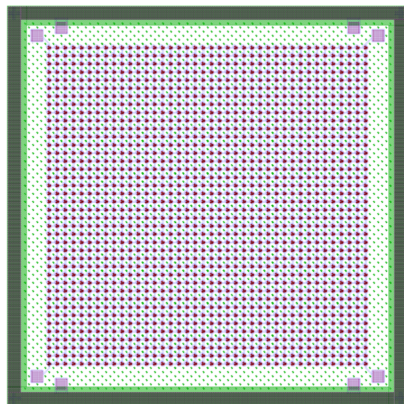
- Surface recombination velocity is **LOW**
- This value is expected to drop drastically after sintering
- Mesurements performed at $V_{p+} = -15V$
- **G24 shows the lowest values at this stage**

3D DIODES (50x50 - 1E)

Measured before sintering on the manual prober ($T =\sim 21^{\circ}C$)



40x40 cells + slim-edge



- **Clear current reduction** when comparing to the previous run
- Reduction in breakdown (**p-spray doping higher** by a factor $\sim$ 10)
- **G24** and **T2-1** are lower than the spec even before sintering
- **T2-1** seems to require slightly higher voltage to deplete ($\sim 9V$)

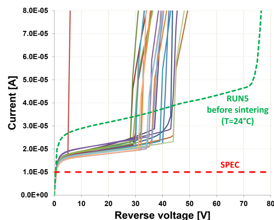
Forskningsrådet

SINTEF

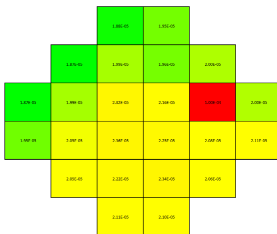
RD53B pixel detectors - WAFER G17 (GOOD)

Measured before sintering ($T_{chuck} = 24°C$)

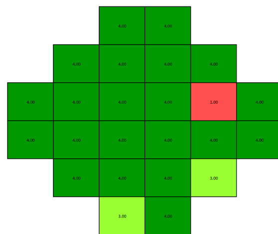
Measured currents



Current at 25V



YIELD (tier map)



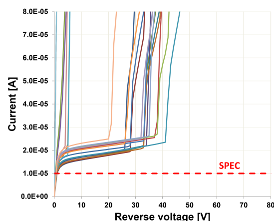
- **RD53B: Yield 87.50%**
- Current specification relaxed in the calculation for now (missing sintering and passivation)
- Current level fairly uniform
- A bit more spreading on the breakdown (sintering and passivation should help)
- **Current reduction with respect to the previous run**

Forskningsrådet

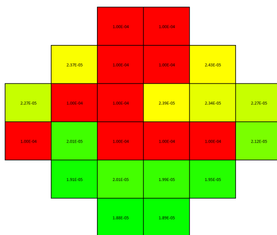
RD53B pixel detectors - WAFER G10 (POOR)

Measured before sintering ($T_{chuck} = 24°C$)

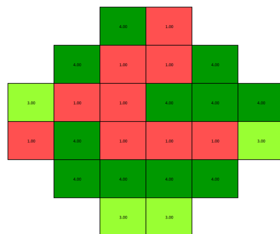
Measure currents



Current at 25V



YIELD (tier map)

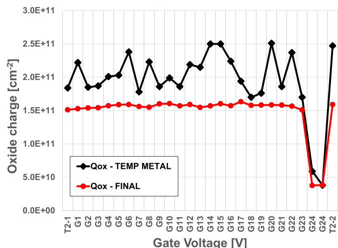


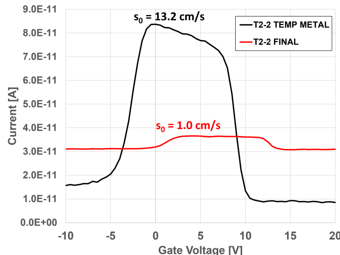
- **RD53B: Yield 45.83%**
- More detectors breaking down before 10V (defective)
- More spreading in current value
- Slightly lower breakdown with some 'marginal' detectors

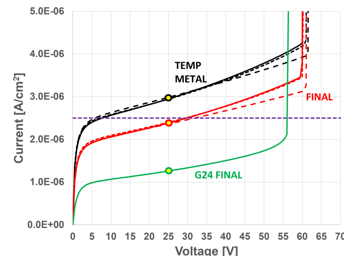
SINTEF

Effect of Sintering and Passivation

MOS capacitor, Gated diode, 3D diodes (manual prober)







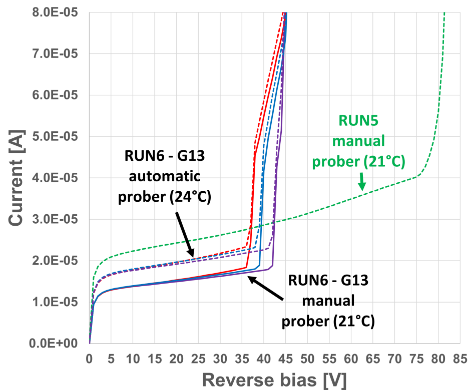
- **MOSCAP:** reduction and stabilization of the oxide charge
- **GATED DIODE:** considerable reduction in surface recombiantion velocity
- **3D DIODES:** reduction in reverse current, goes below the spec at 25V
- Post sintering current reduction by a factor between **1.2** and **1.4** on **3D diodes**

Forskningsrådet

Effect of temperature on the current measurements

RD53B - Manual prober (21°C) vs. Automatic prober (24°C)

- The automatic prober is a fairly 'enclosed' system with little air circulation
- The **temperature on the chuck** is 24°C
- Leakage current **doubles** every 7°C
- The **specification** is given at 20°C
- The measurements can be scaled to the desired temperature using the following approach…

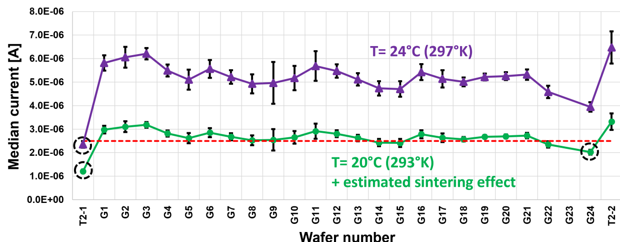


SINTEF
Forskningsrådet

SINTEF

Scaling of reverse current to 20°C

Median current value at 25V of bias for all wafers



Scaling formula

$$I(T_2) = I(T_1)\left(\frac{T_2}{T_1}\right)^2 \exp\left[-\frac{E_g}{2k}\left(\frac{T_1 - T_2}{T_1 T_2}\right)\right]$$

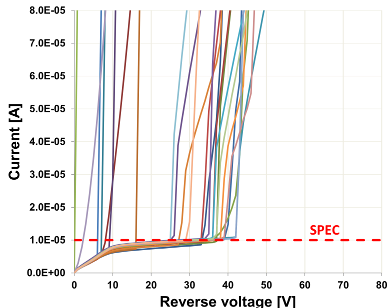
$$T_1 = 297^\circ K; T_2 = 293^\circ K$$

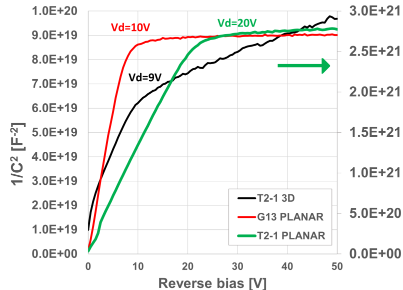
- Wafer **T2-1** was already under the spec at $24^\circ C$
- Scaling and **accounting for sintering** (factor 1.3) wafer **G24** is under the specification
- The rest of the wafers sit more or less **ON** the specification

Forskningsrådet

Why does T2-1 stand out?

PiKEM (UK) - substrate material from Silicon Valley Microelectronics (US)

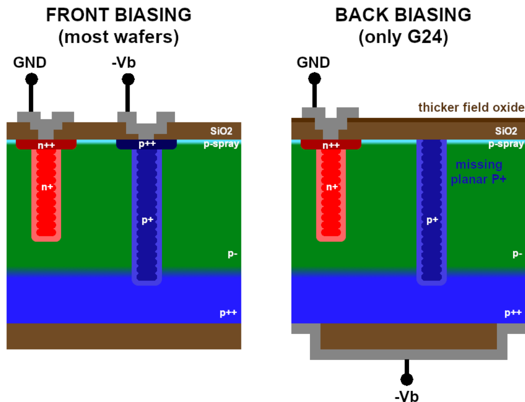




- **T2-1** went through **all the processing steps** together with the rest of the wafers
- The **current** on the **pixel detectors** is considerably lower
- The only other difference is the **higher depletion voltage**
- The **substrate resistivity** seems to be lower than for ICEMOS (Topsil) wafers [8 $k\Omega cm$ vs. 20 $k\Omega cm$]
- Is the quality of the starting material different? Difficult to tell…
- **Additional investigation only possible with destructive testing after bump bonding**

Why does G24 stand out?

- This wafer had to **skip the last two thermal steps** (planar Boron doping and final anneal)
- The 3D part of the process was completed so it was decided to try **biasing from the support wafer** (extra processing)
- This resulted in lower Q_{ox} and s_0 ($\sim 5 \times 10^{10}\ cm^{-2}$ and $2\ cm/s$ respectively)
- Skipping the Boron doping saves roughly $200nm$ of thermal oxide
- The **TEMP METAL** is deposited on the **oxide** (not on the passivation) $\Rightarrow$ surface depletion at lower bias
- A **thicker oxide** can delay the surface inversion under the TEMP METAL grid $\Rightarrow$ **less surface current**
- **We are currently testing the deposition of the TEMP METAL on top of the passivation (results next week)**

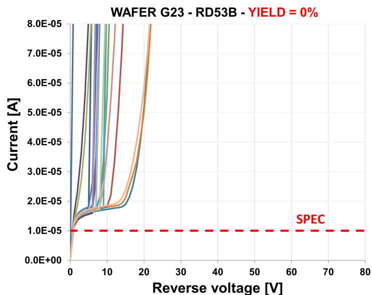


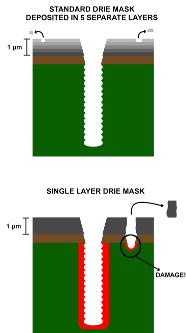
SINTEF
Forskningsrådet

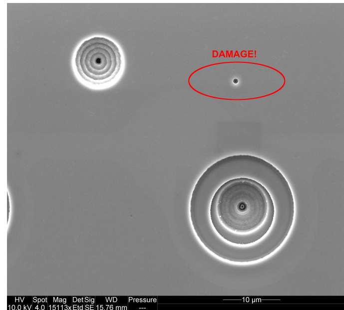
Lessons learned in RUN 6

Deep Reactive Ion Etching - DRIE

Integrity of the masking layer







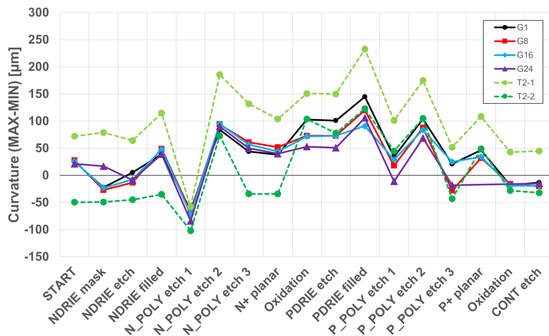
- The DRIE process is masked using an **Aluminium mask** deposited in **5 steps** of $0.2\mu m$ ($1.0\mu m$ in total)
- During DRIE **aluminium grains can detach** leaving a void, the multi-layer mask ensures full coverage at all times
- Depositing the mask in **one step** would **reduce process complexity and duration (higher risk!)**
- This was tested on wafer **G23**
- This gave confirmation that a **single layer mask is not sufficiently reliable**
- The detectors breakdown before full depletion or slightly after

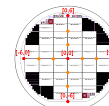
Forskningsrådet

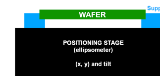
SINTEF

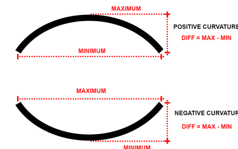
Wafer bowing and warping (1)

Tracking during the process









- Measured using the **ellipsometer** (10 points take roughly 3-4min per wafer)
- Dedicated wafer support holding the wafers only at the exclusion zone
- The weight of the wafer will have an effect on the measurement
- Considerably **easier to control bowing/warping with thicker support wafers**
- Wafer **warping** ⇒ higher resolution measurements (30 min/wafer) (only done at critical steps in the process)

SINTEF
Forskningsrådet

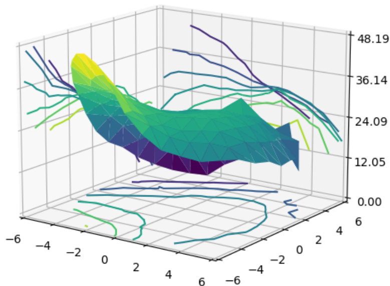
SINTEF

Wafer bowing and warping (2)

Higher resolution measurements (examples)

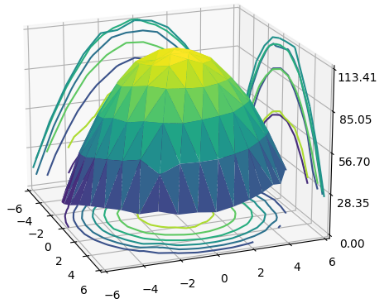
After complation of N+ columns and planar doping

WAFER ID = T2-2 - Support + Device =650 μm - Curvature = 48.19 μm



After etching of the P+ polysilicon from the wafer backside

WAFER ID = G1 - Support + Device =650 μm - Curvature = 113.41 μm



SINTEF

Forskningsrådet

SINTEF

Conclusions and future plans

- We have completed the 6th run of 3D detectors at SINTEF MiNaLab
- Replacing the ACTIVE-EDGE with the SLIM-EDGE termination contributed to much easier processing
- Temporary metal measurements before sintering are promising but will require verification after bump bonding
- Measurements on test structures after completion of the processing seems to further improve the results
- We are currently completing the patterning of the TEMP METAL on top of the PASSIVATION
- It should be possible to start electrical characterization soon
- Final wafer inspection and curvature measurements will be performed before shipment
- Functional characterization should follow shortly after

Technology for a better society

SINTEF