A monolithic ASIC for the very high precision pre-shower detector of the FASER experiment at the LHC

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- System design

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- Sensor design
- Analog electronics
- Laboratory test

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- System design
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- Board design
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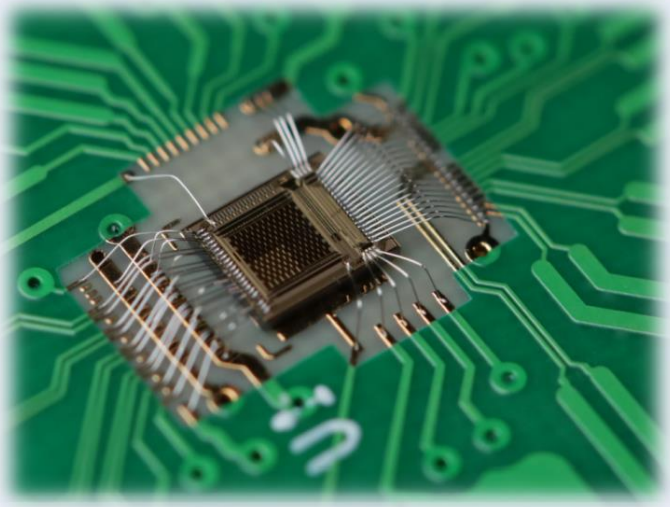
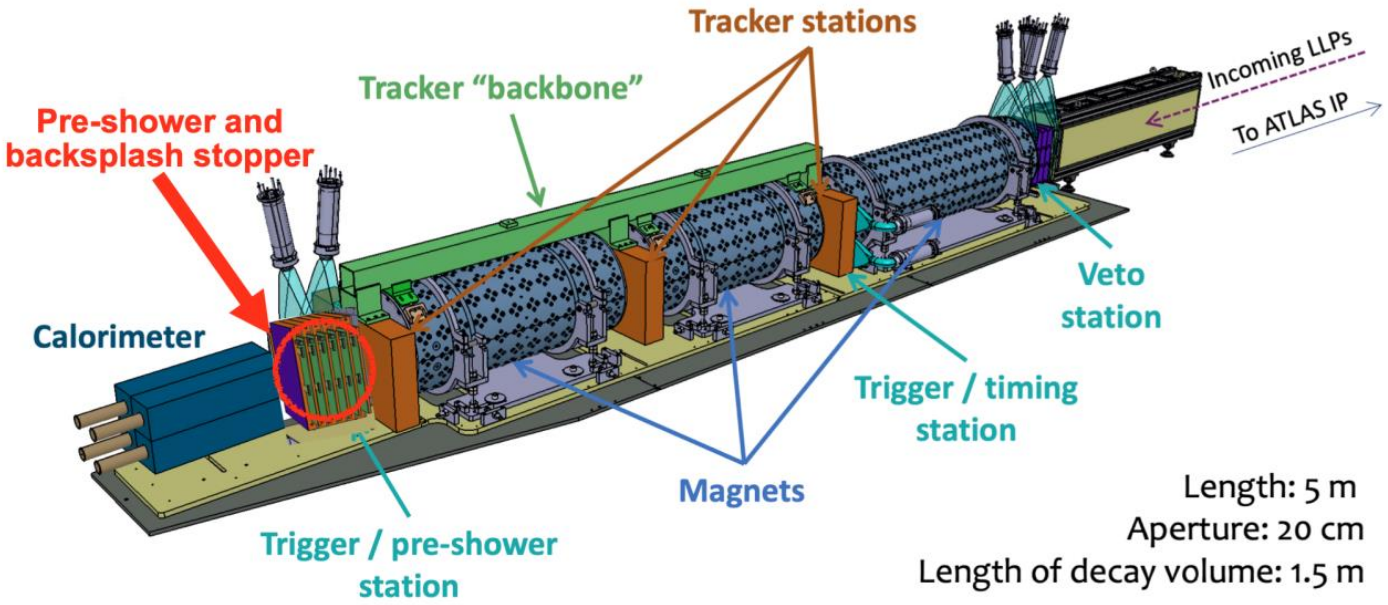


Proposal for a new pre-shower detector

Current preshower:
2 layers of tungsten (1X0) + scintillating detectors ⟹ No XY granularity.

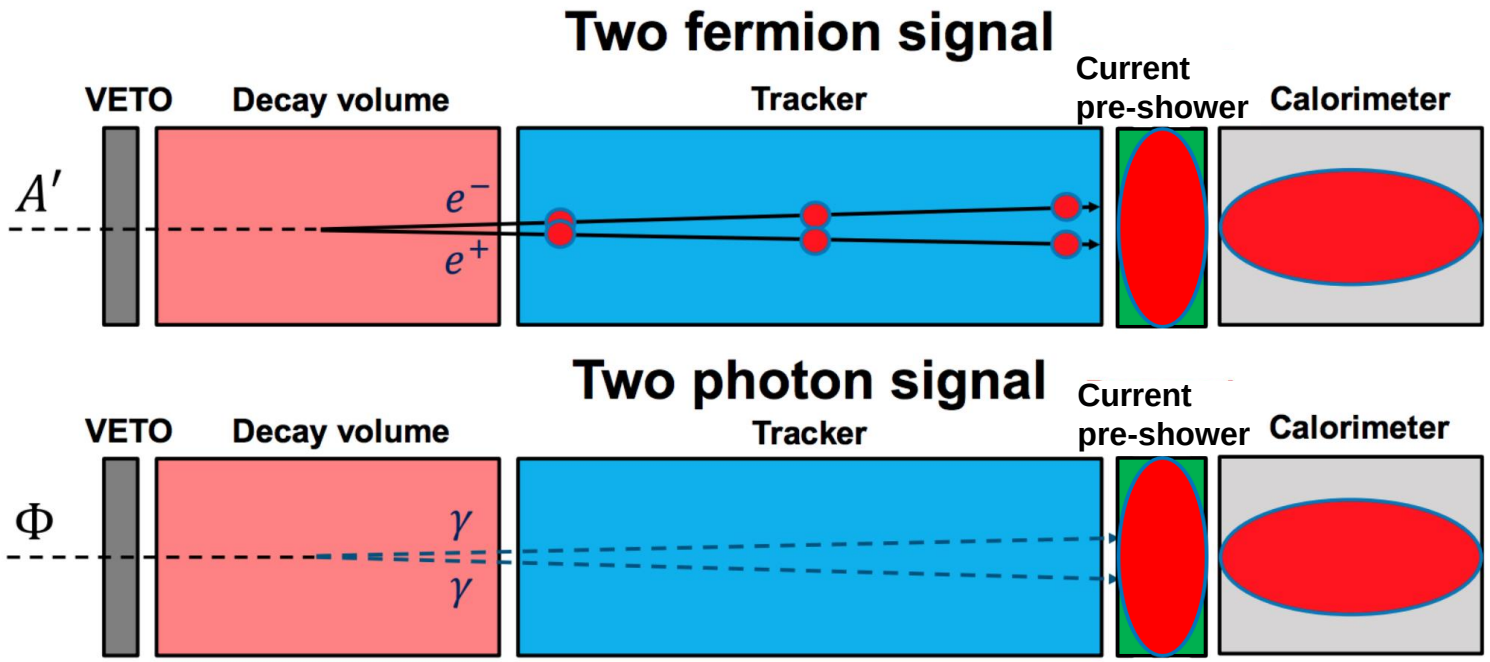


The project:

- **A high-granularity/high dynamic range pre-shower** based on monolithic silicon pixel sensors.
- Discriminate **TeV scale electromagnetic showers**.
- Targeting data taking in 2024/25, during LHC run 3 and during HL-LHC.

The goal of the new pre-shower

- The goal is to have independent measurement of two very collimated photons.



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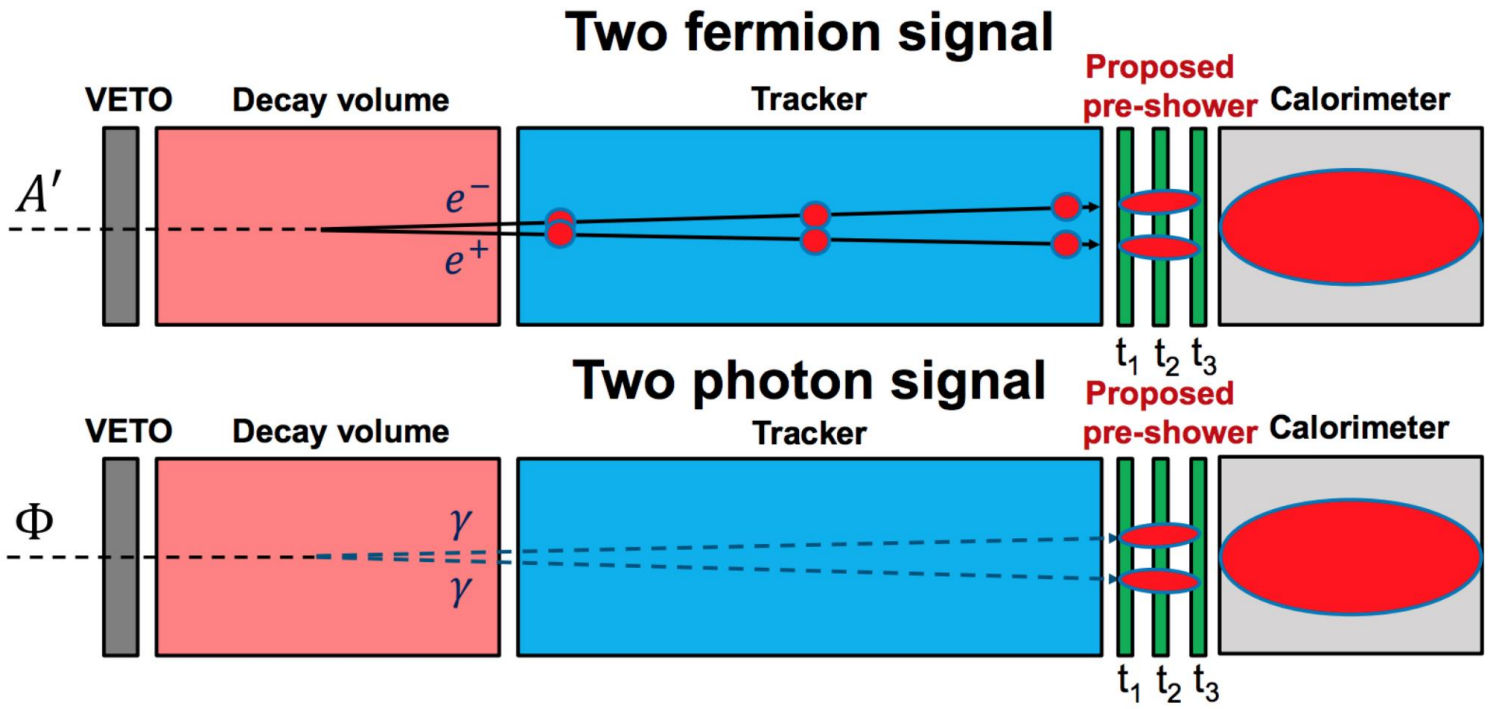
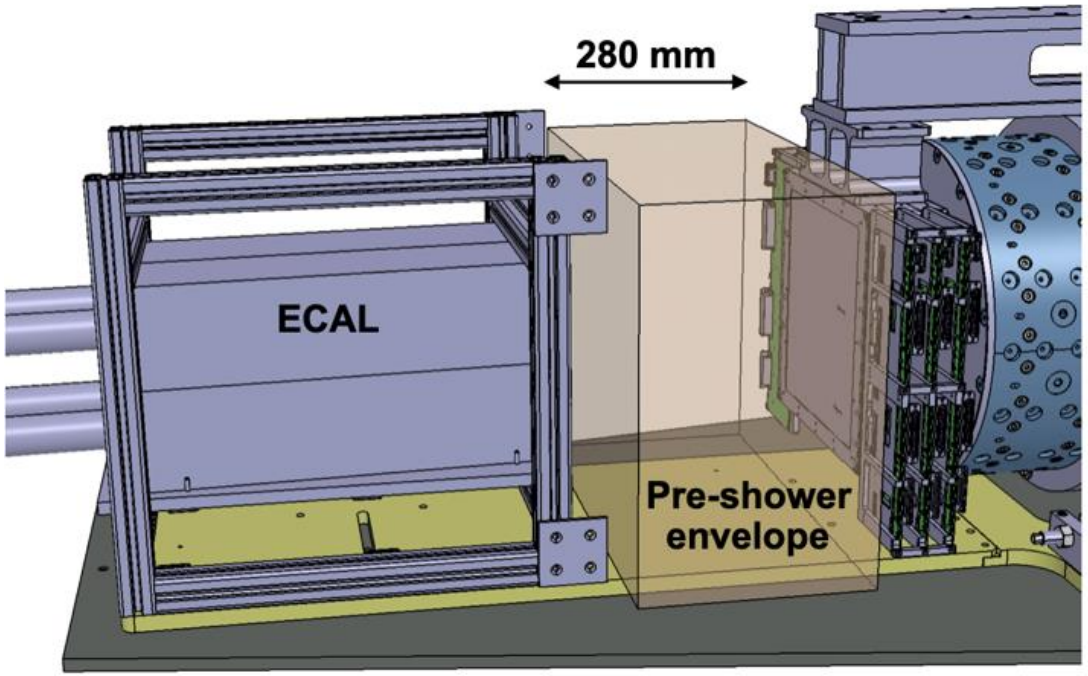


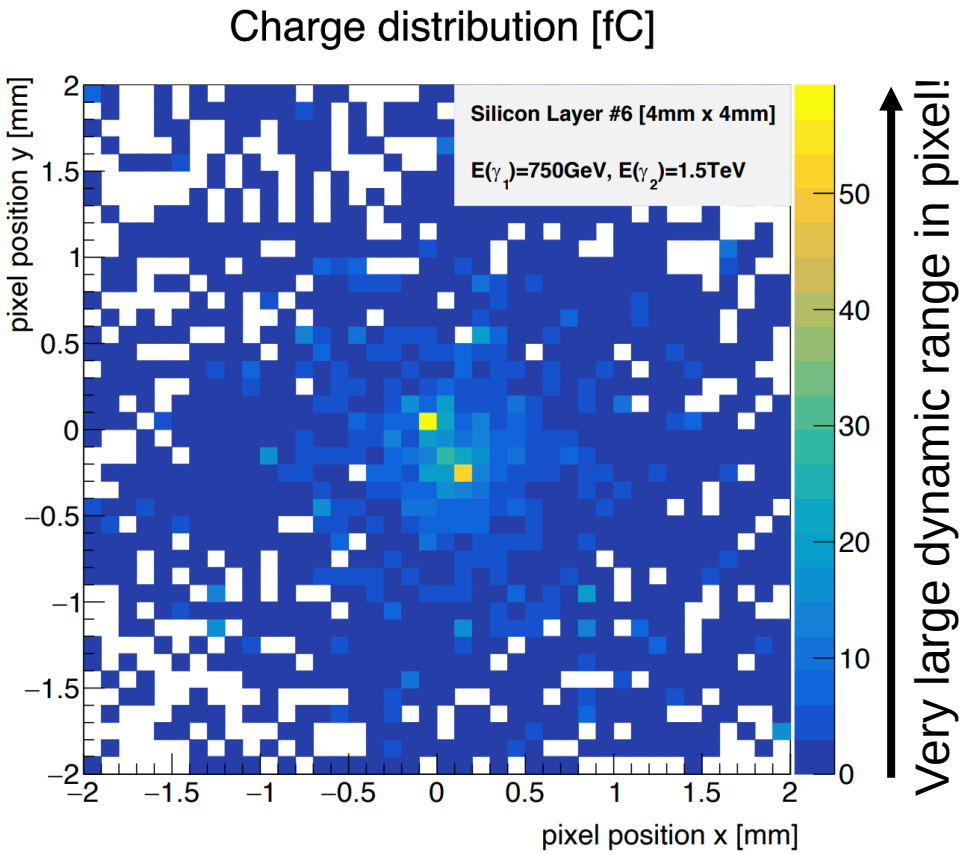
Pre-shower design

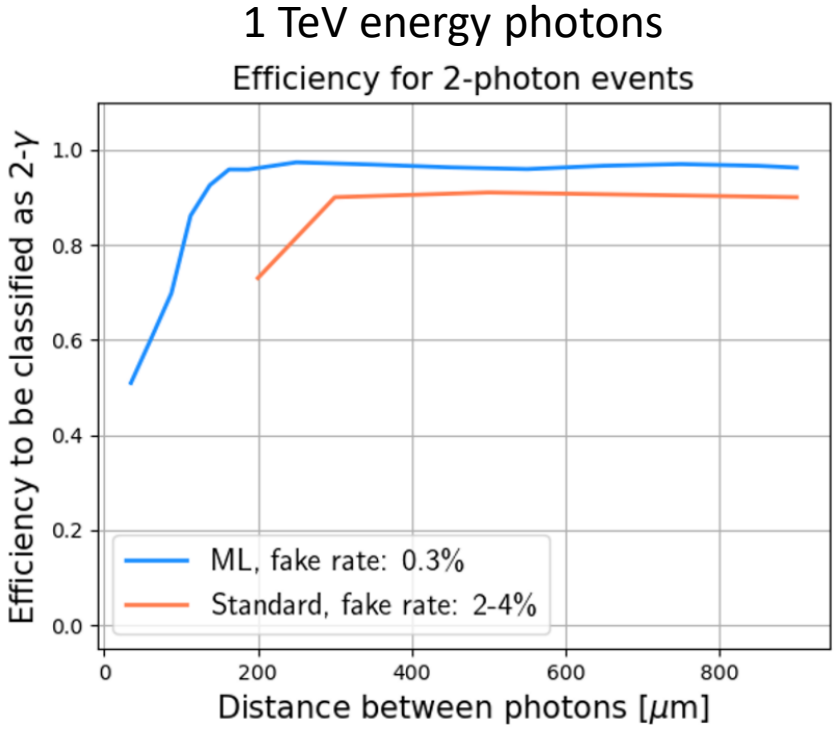


6 detector planes + 2 plastic scintillators:

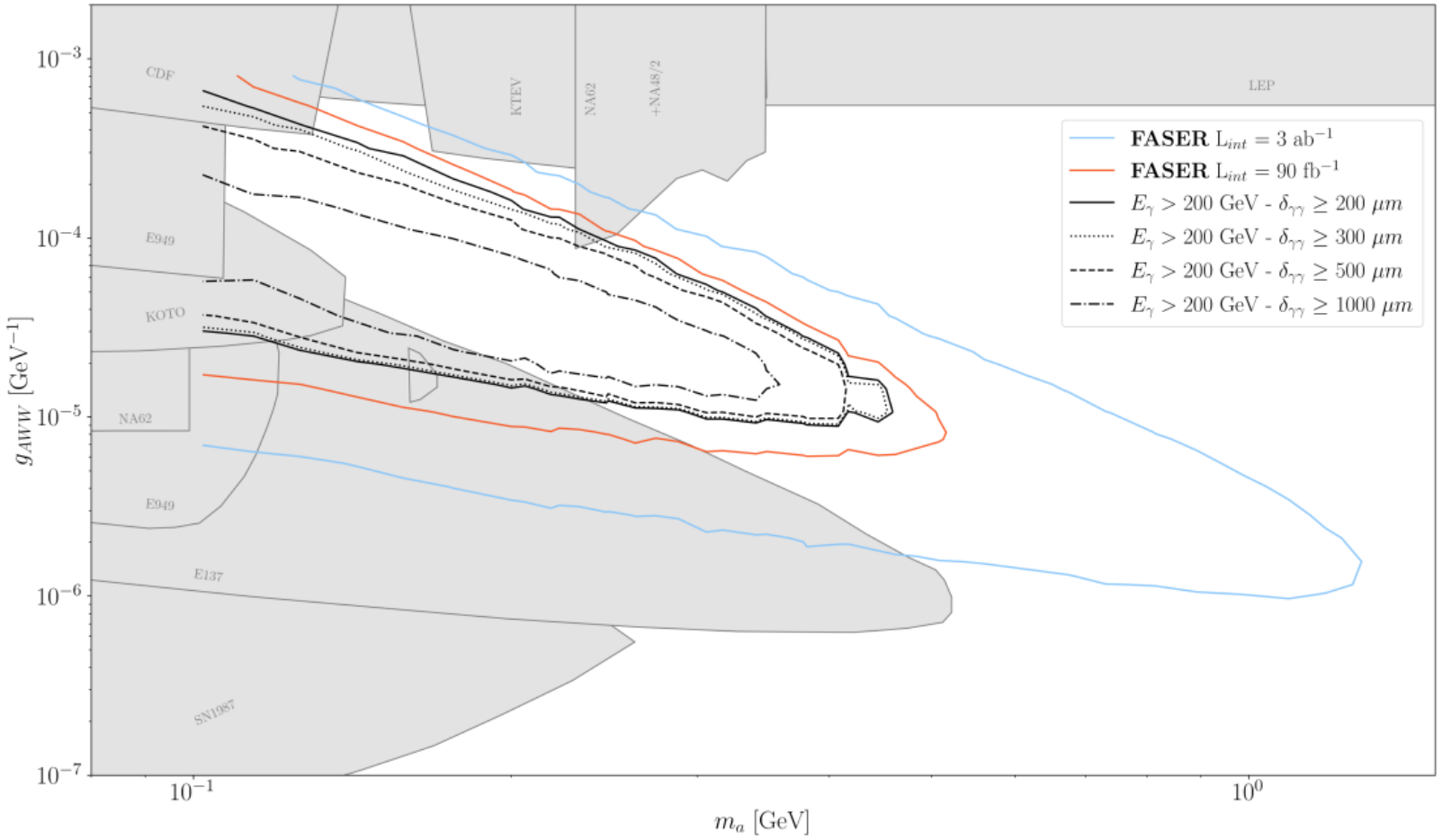
Each plane: 1 X0 of tungsten + 1 plane of monolithic Si-pixel detectors

Event on a pre-shower plane





Search for ALP: Expected performance



0 photon background assumption:

- High rejection probability of single photon events.
- Rare TeV-scale single photon events pointing to ATLAS IP.

Main background source:

- Neutrino background

Monolithic ASIC specifications

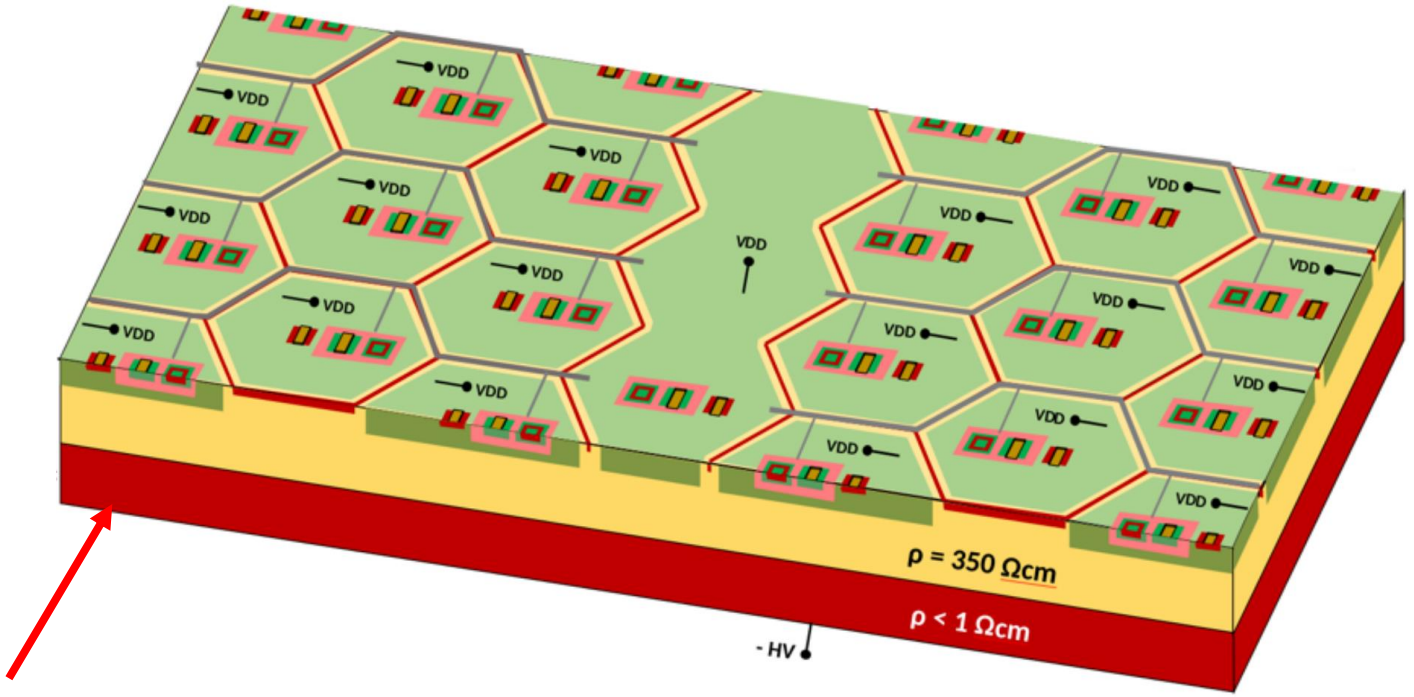
Main specifications	
Pixel size	65 µm side (hexagonal)
Pixel dynamic range	0.5 ÷ 65 fC
Cluster size	O(1000) pixels
Redout time	<200 µs
Power consumption	< 150 mW/cm^2
Time resolution	< 300 ps

Selected technology: SG13G2, by IHP microelectronics.

- Monolithic ASIC in **130nm SiGe BiCMOS.**
- Chip size: 1.5 x 2.5 cm^2.
- Pixel size: hexagonal pixels, 65 µm side.
- Local analog memories to store the charge.
- Ultra fast readout with no digital memory on-chip to minimize the dead area.
- **In between an imaging chip and a HEP detector.**

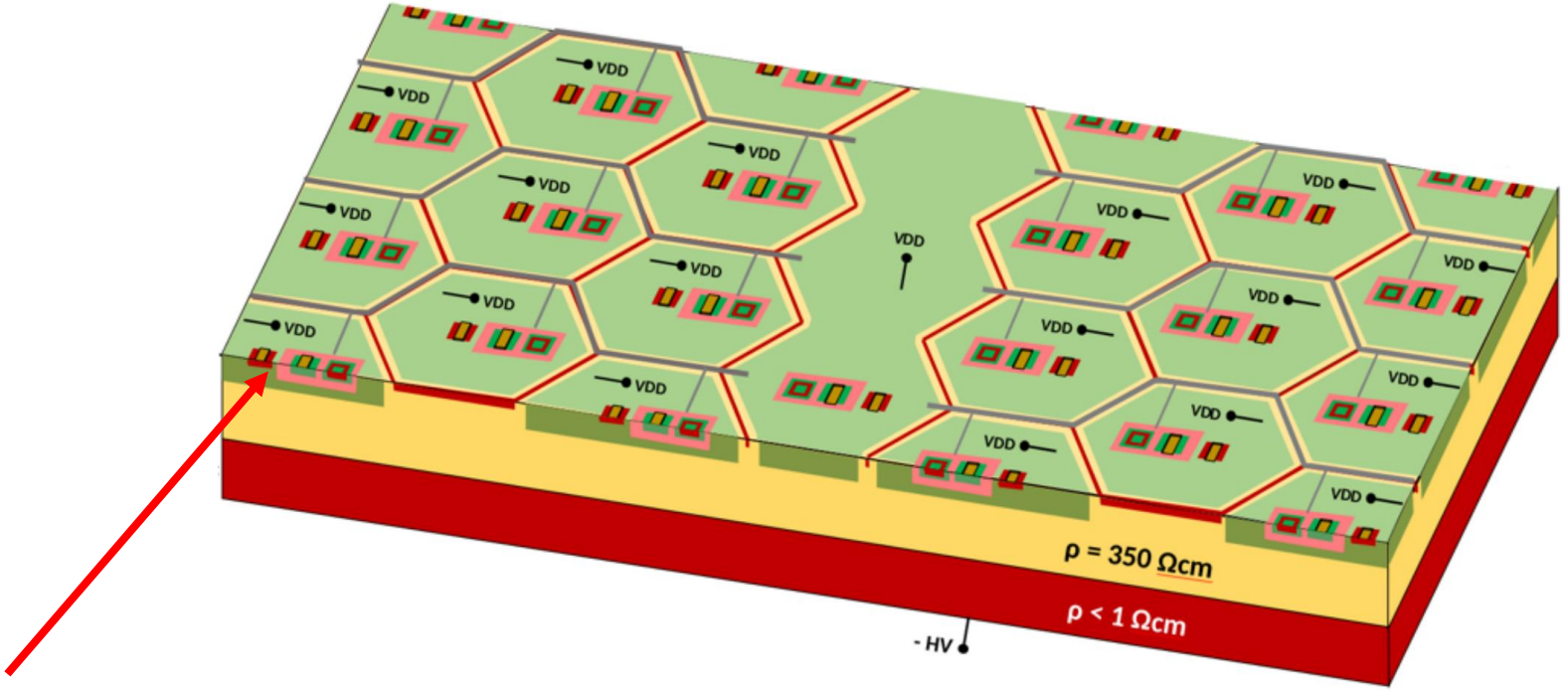
ASIC design in collaboration between CERN, University of Geneva and KIT

Sensor cross section



- <1 Ωcm, heavily P-doped substrate.
- Negative High Voltage applied to the substrate.

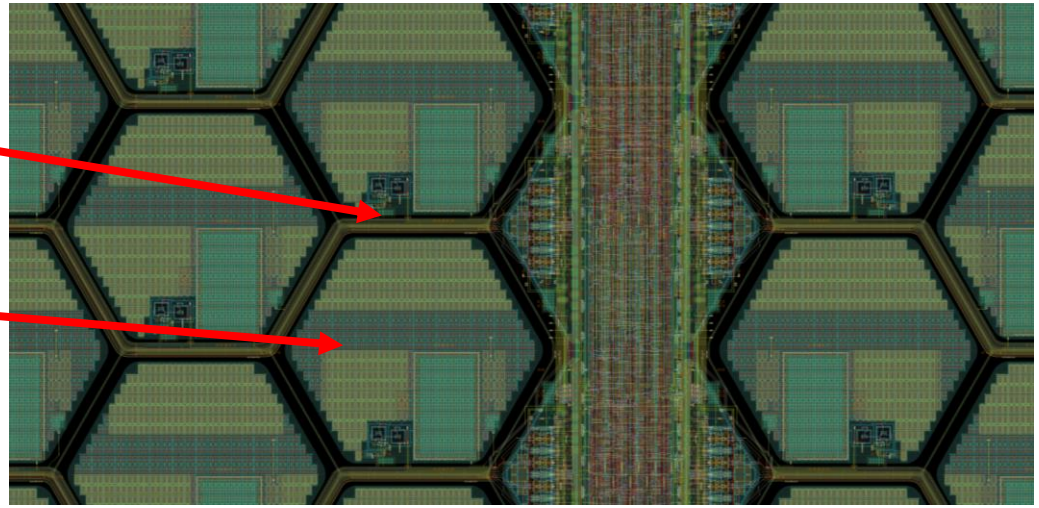
Sensor cross section

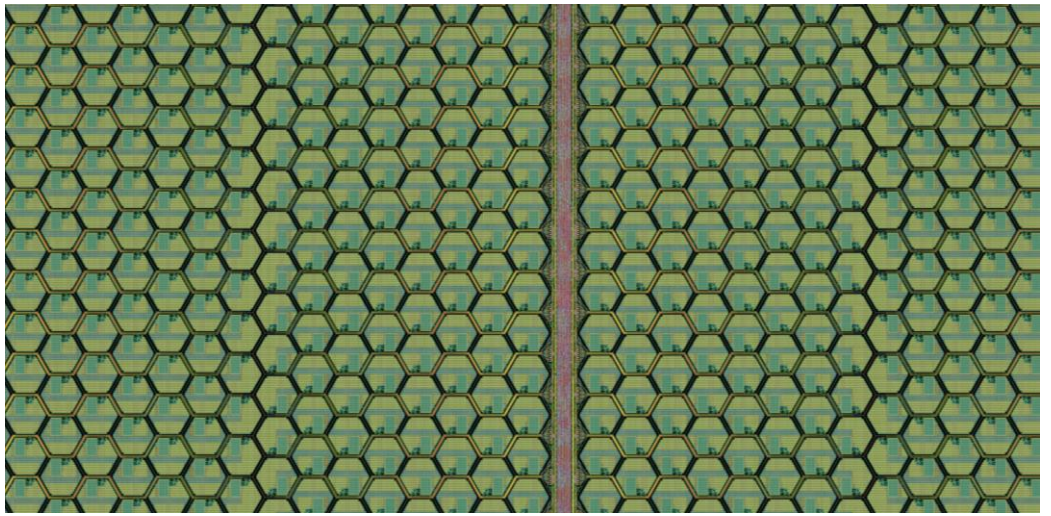


- Electronics inside the guard-ring, isolated from substrate using deep n-well.
- Triple well design: polysilicon, nmos and HBTs in an isolated pwell, pmos directly in the pixel nwell.
- Pixel and electronic deep n-wells are kept at positive low voltage.

Monolithic layout

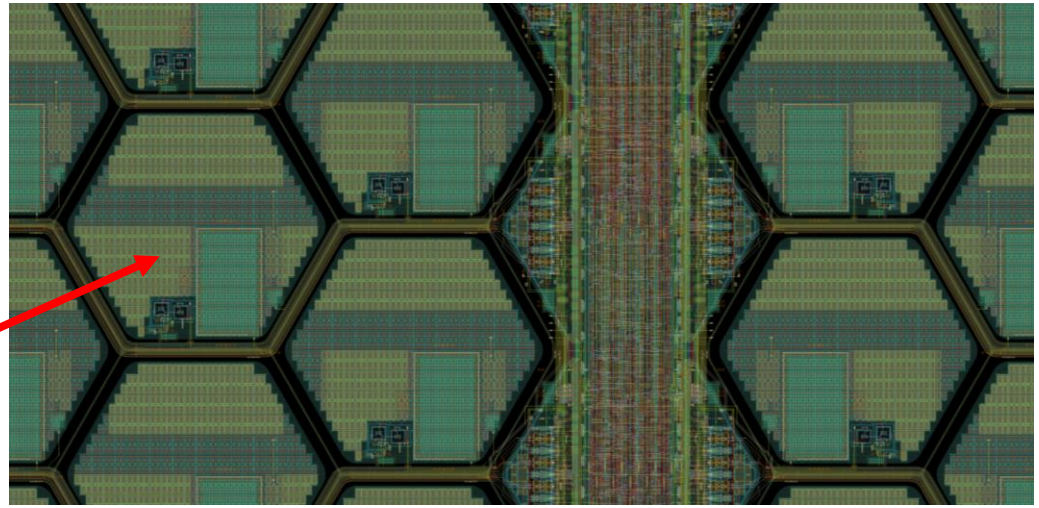
- Polysilicon resistor parasitic capacitance to nwell is too large to realize a proper biasing: pmos bias is necessary.
- Pixel bias at Vcc to avoid body effect on pmos.

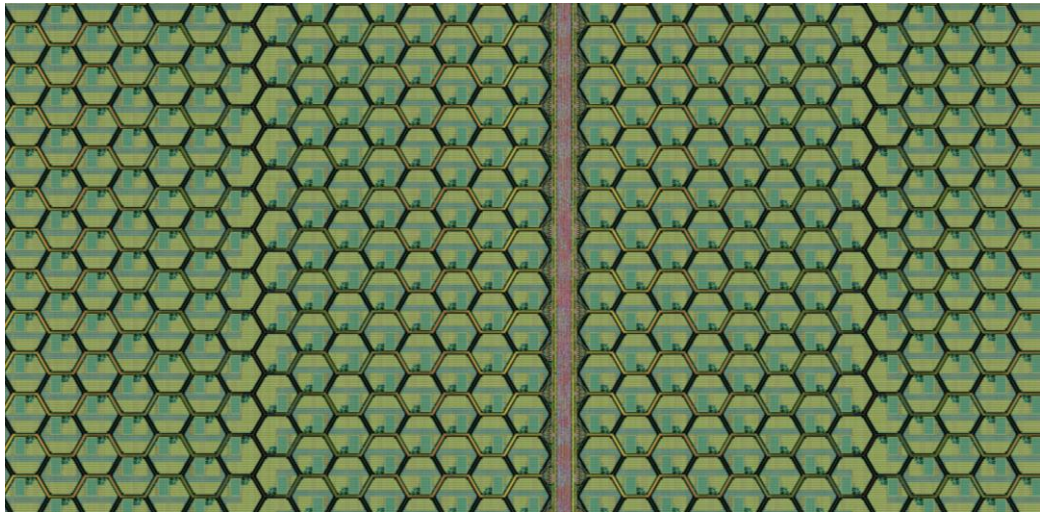




Monolithic layout

- Polysilicon resistor parasitic capacitance to nwell is too large to realize a proper biasing: pmos bias is necessary.
- Pixel bias at Vcc to avoid body effect on pmos.
- Capacitive coupling using a matrix of large area pmos distributed in the pixel.





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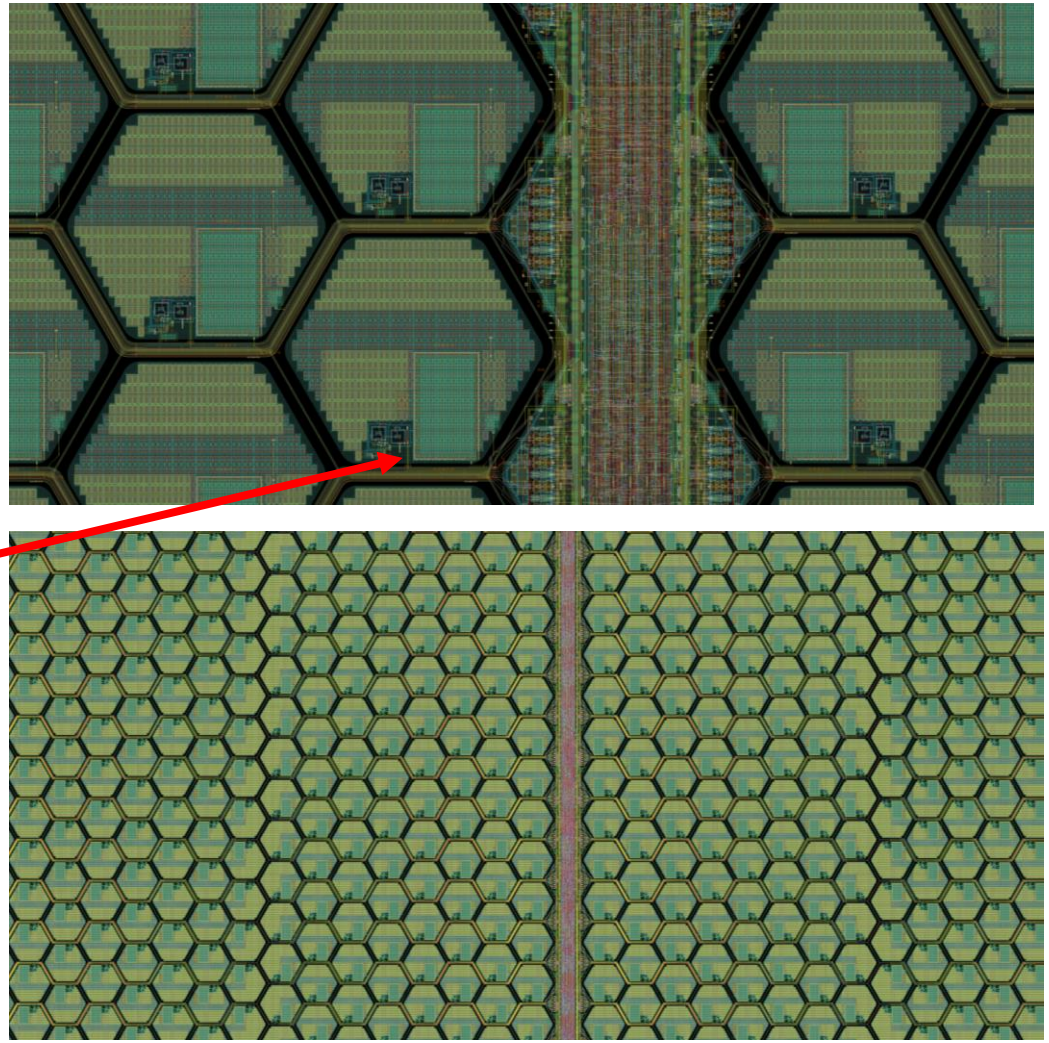
- Nmos are preferred in sensitive nodes, to avoid unnecessary parasitic capacitance towards the input.



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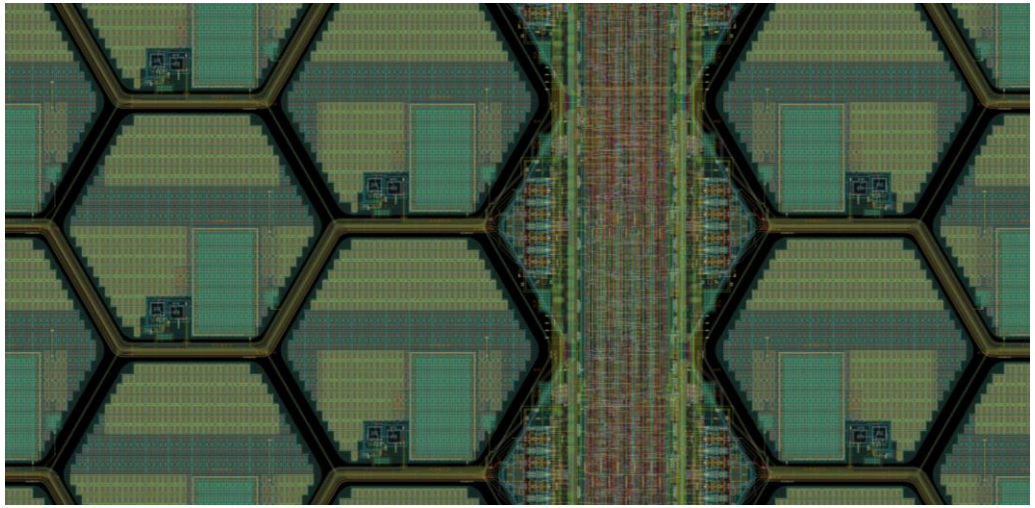
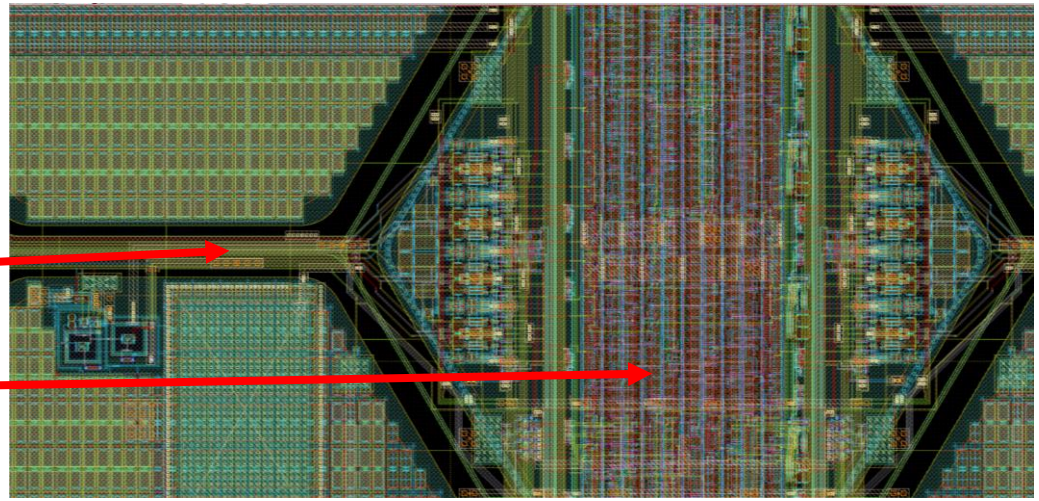
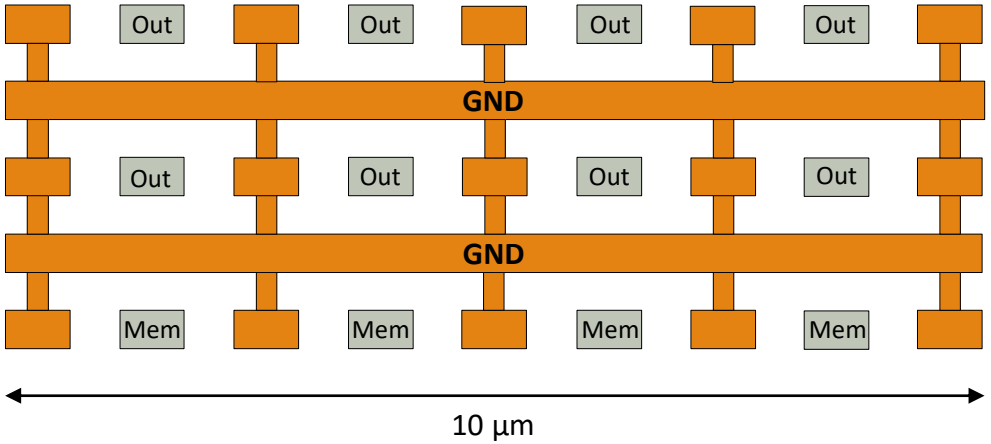
- Polysilicon resistor parasitic capacitance to nwell is too large to realize a proper biasing: pmos bias is necessary.
- Pixel bias at Vcc to avoid body effect on pmos.
- Capacitive coupling using a matrix of large area pmos distributed in the pixel.
- Nmos are preferred in sensitive nodes, to avoid unnecessary parasitic capacitance towards the input.
- Signal routing after amplification stage requires shielded bus to avoid cross-talk to pixels.
- Digital electronics in separate well.



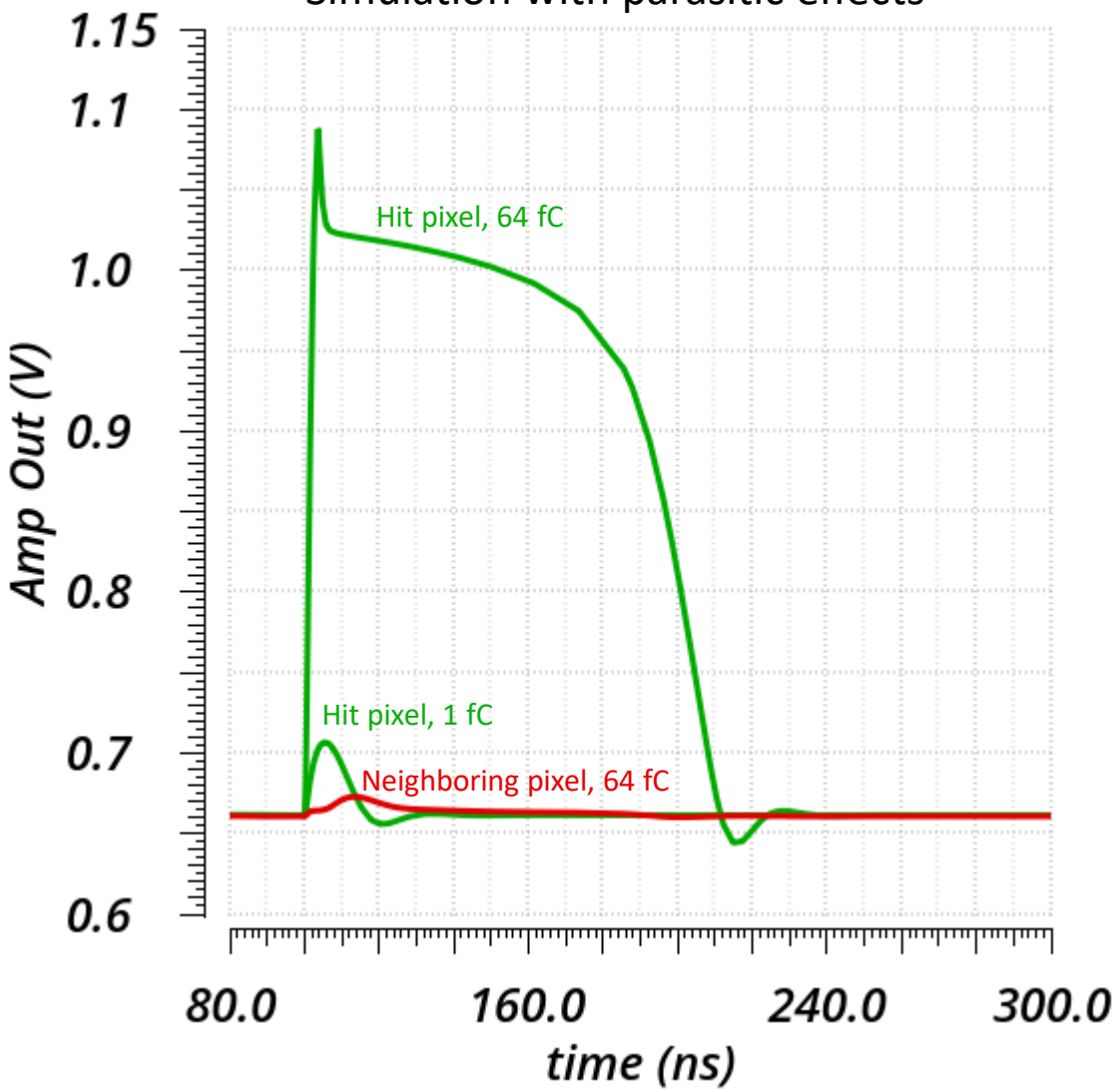


Signal routing

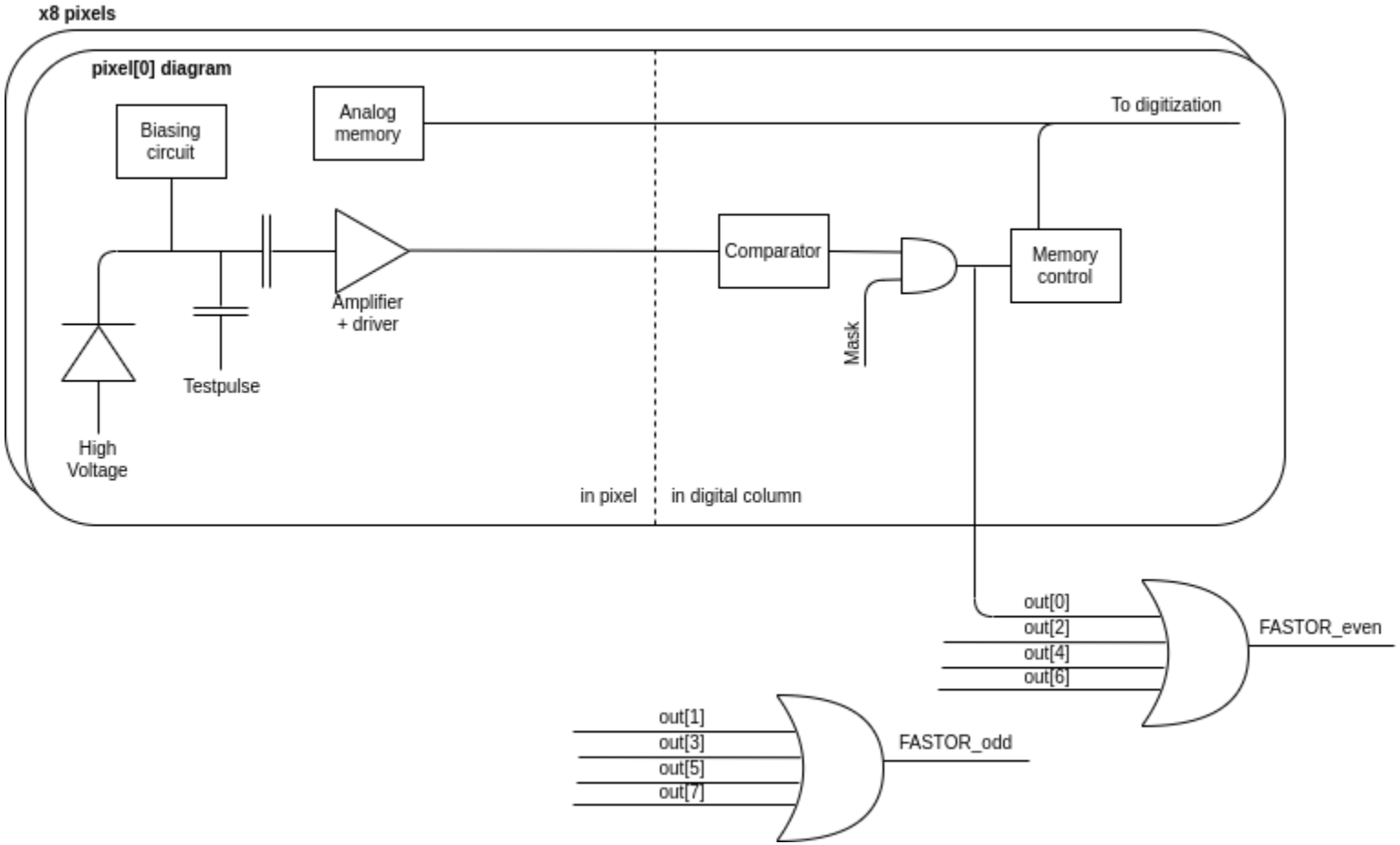


- Extra output capacitance ~20 fF.

Simulation with parasitic effects

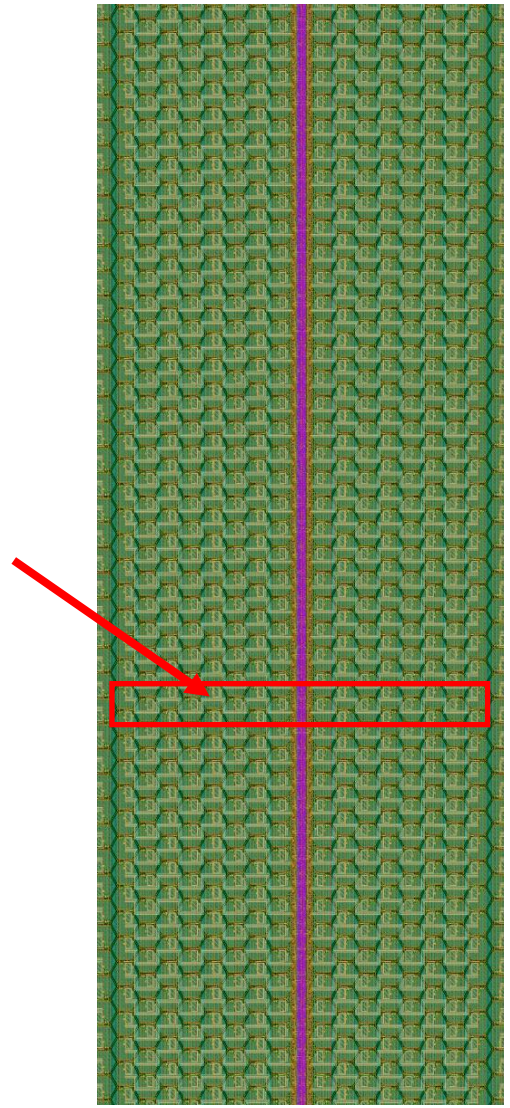


Pixel row structure

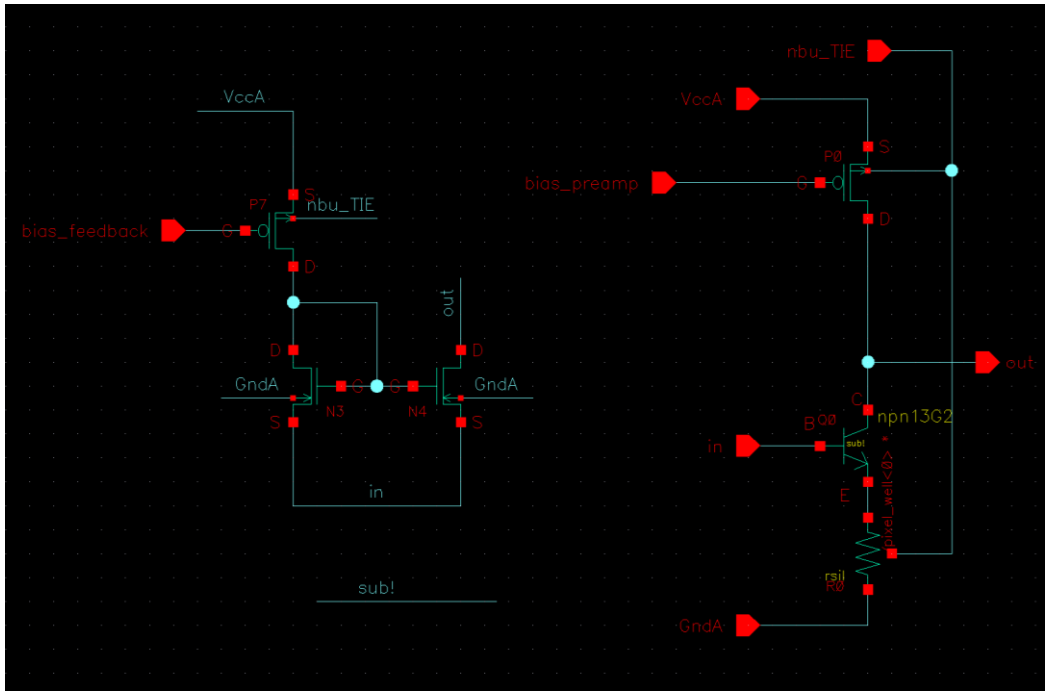


Supercolumn

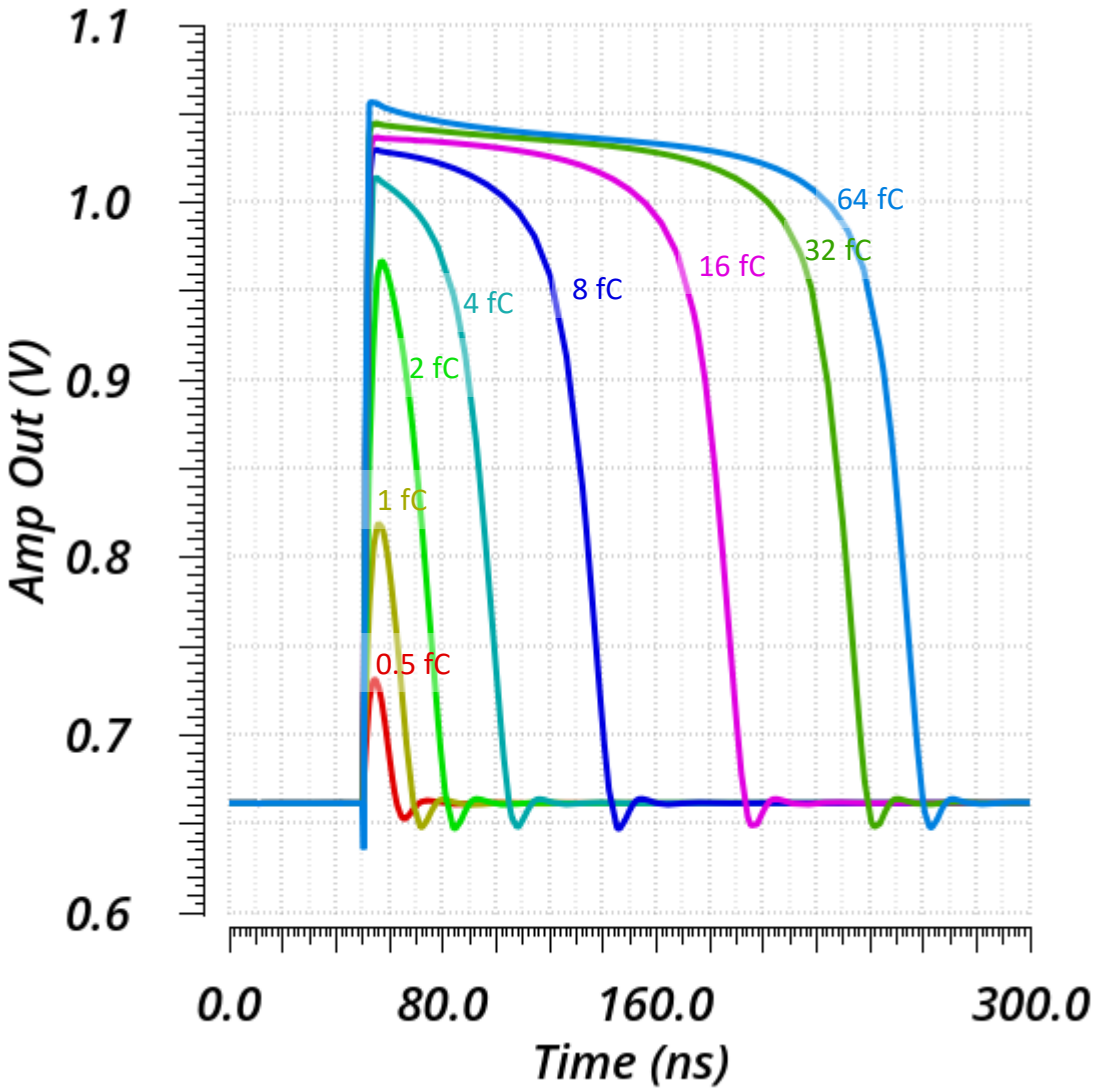
Pixel row



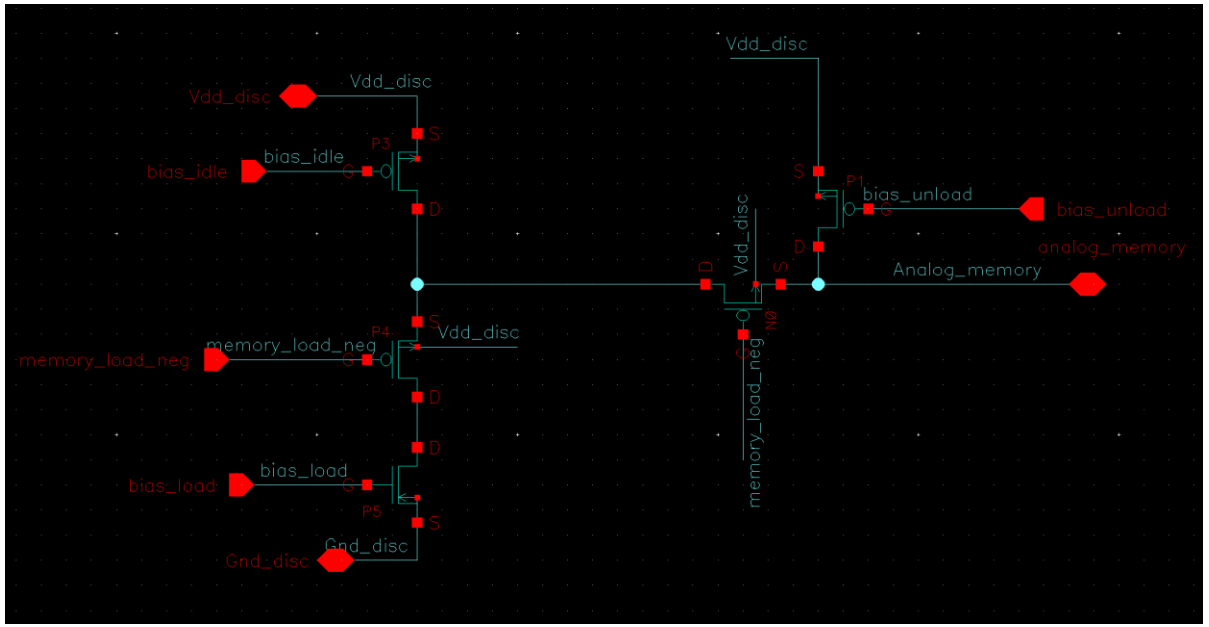
Amplification stage

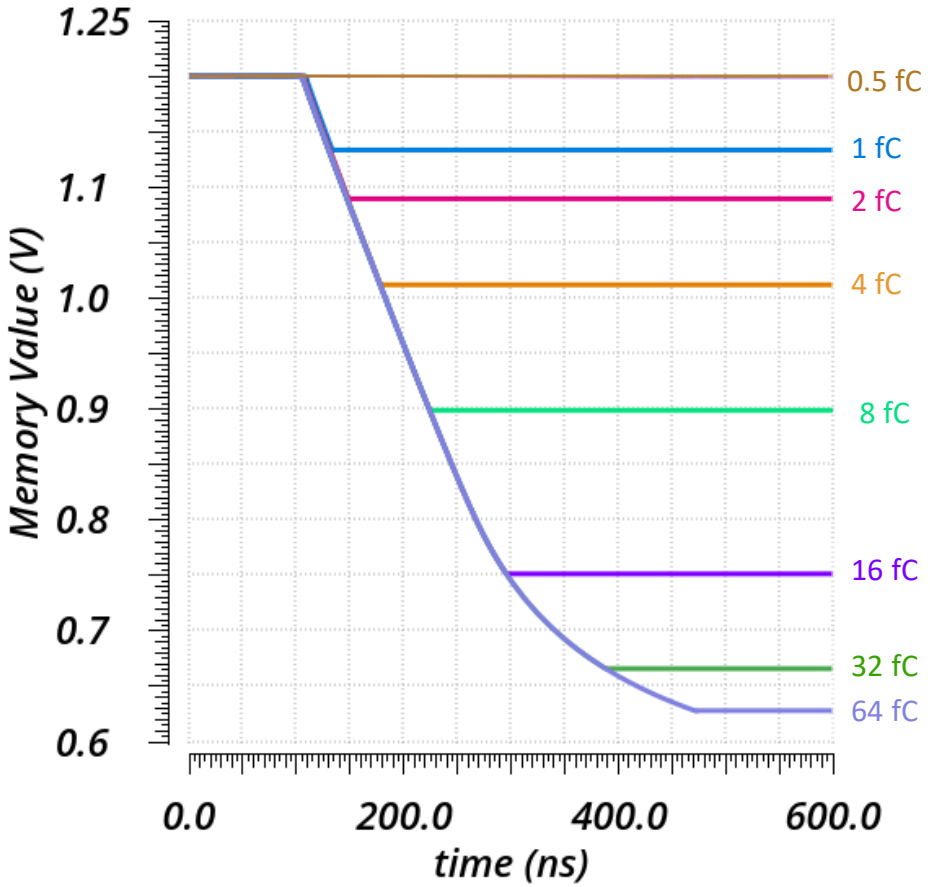


Simulation data

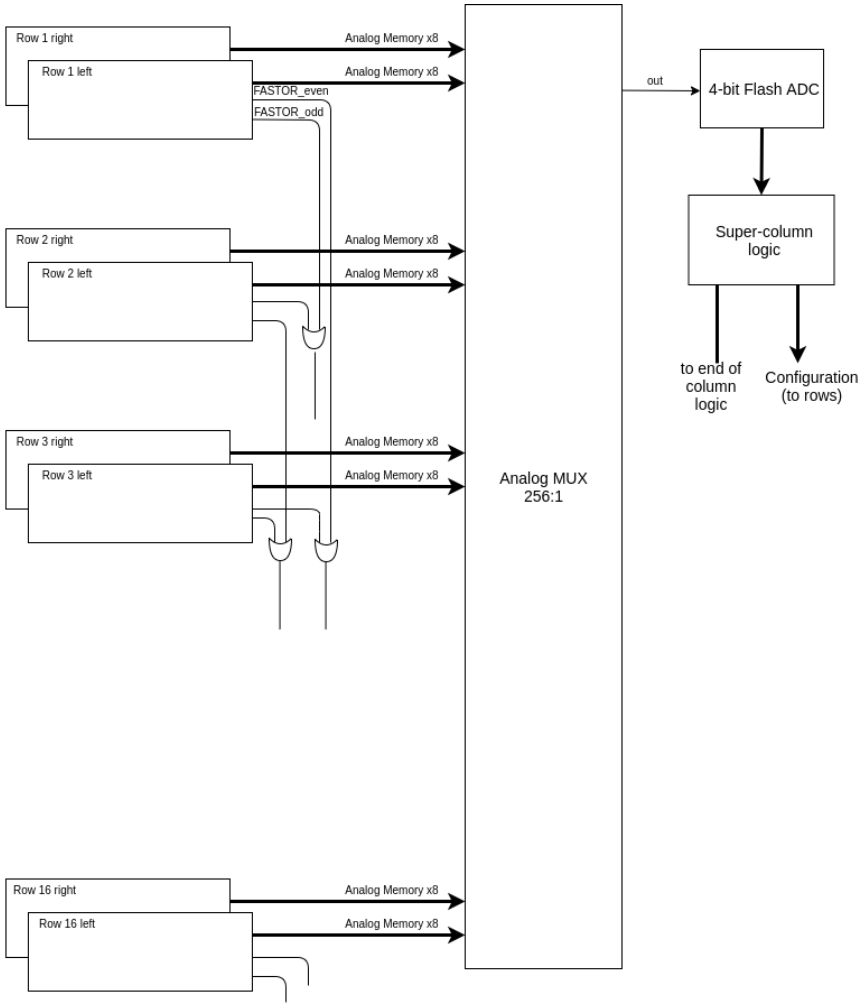


Memory control



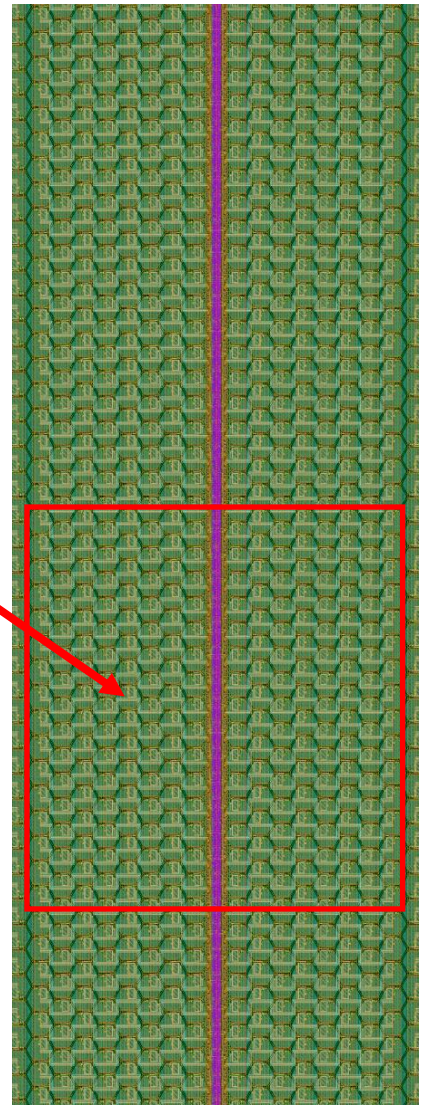


Super-pixel structure

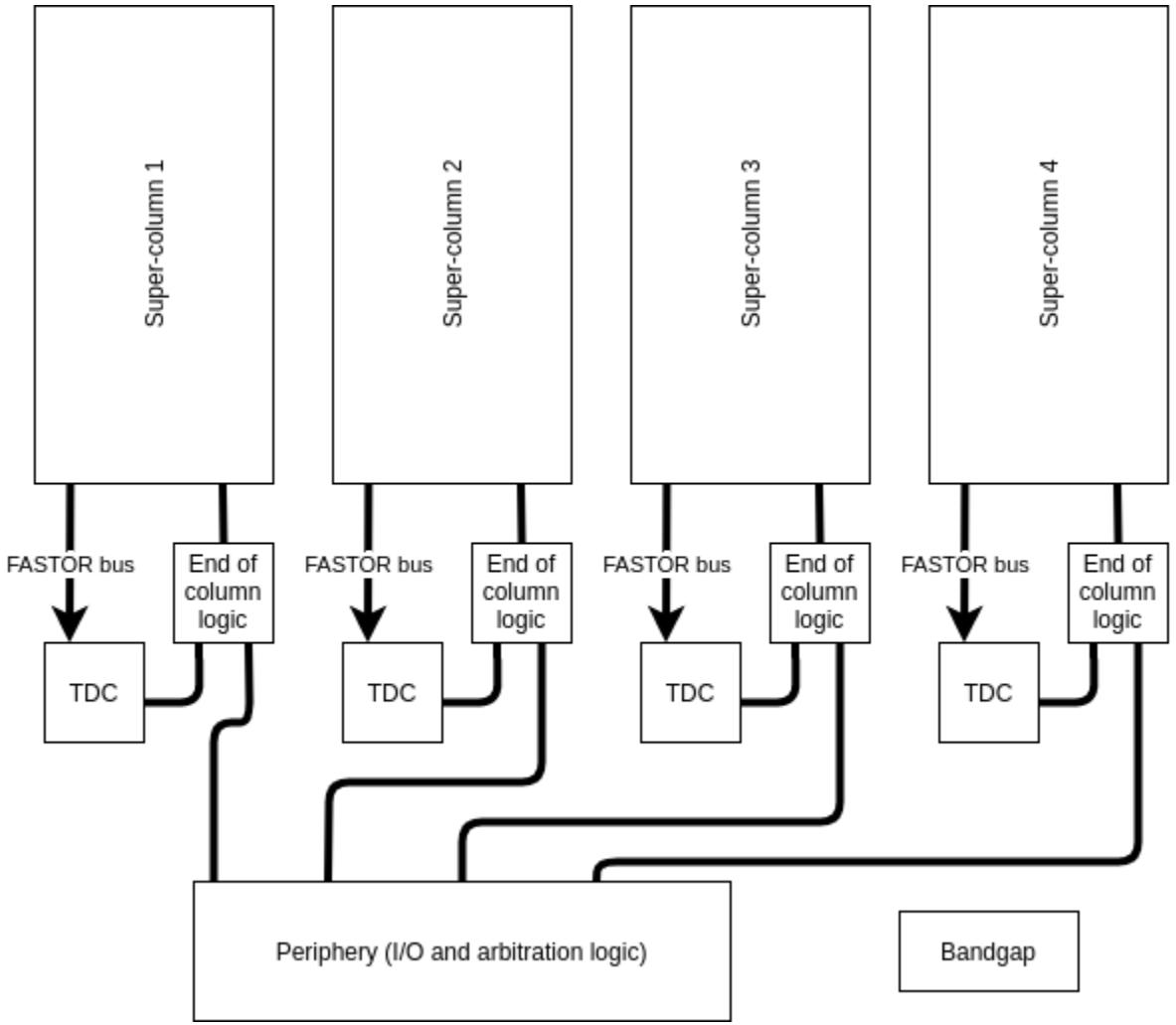


Supercolumn

Super-pixel

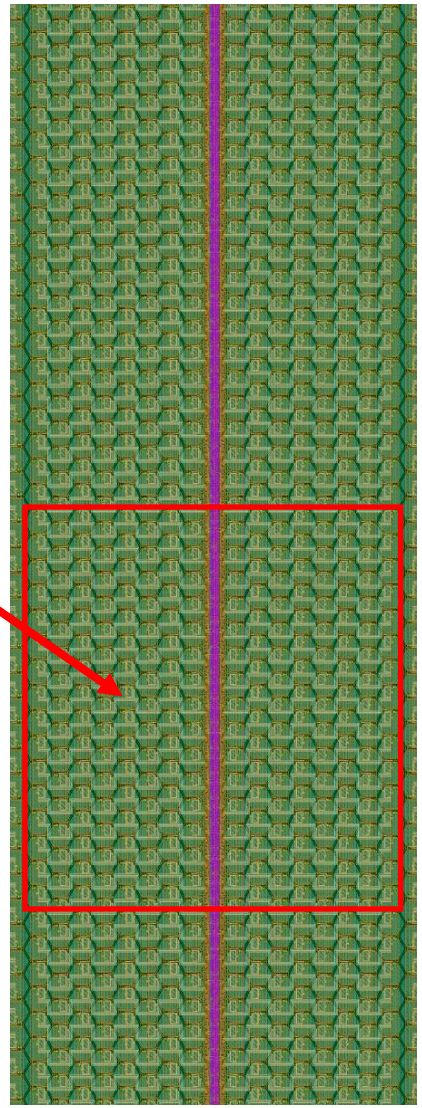


ASIC structure



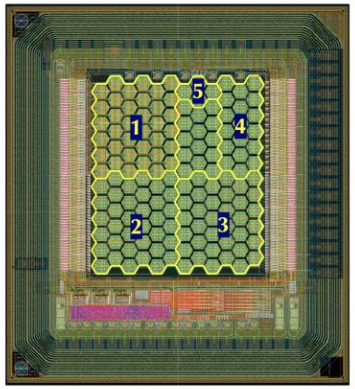
Supercolumn

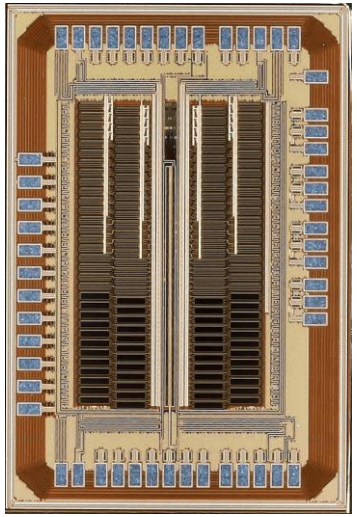
Super-pixel



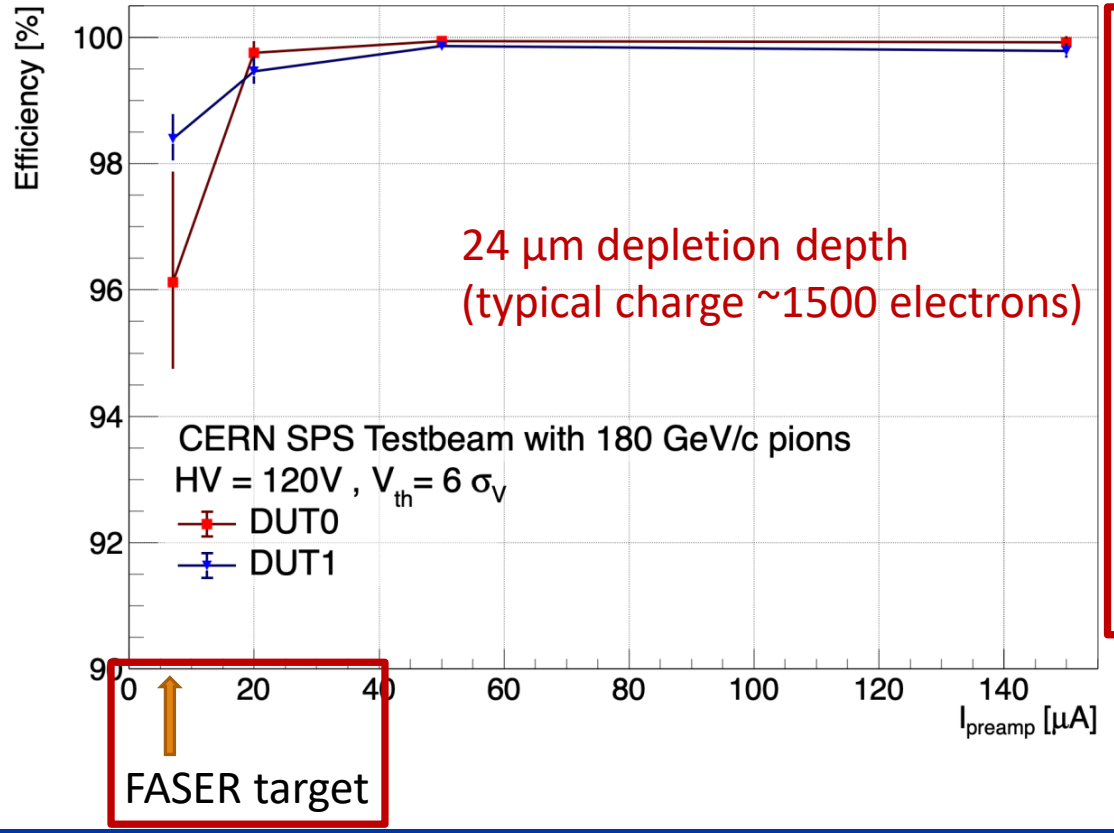
Previous prototypes

Previous development and prototyping





Efficiency to MIPs from test beam measurement.

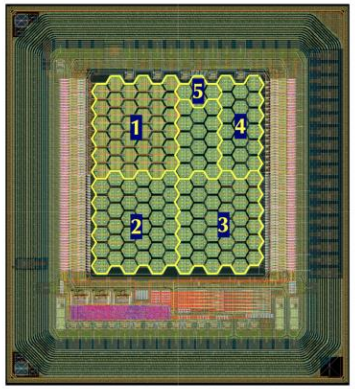


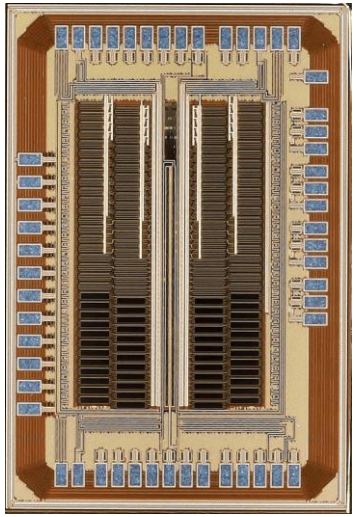
Efficiency for signal events even higher:

- Target 50 µm depletion depth instead of 24 µm.
- Core of the shower has very large charge.
- Reconstruction efficiency obtained for 25ke$^-$ threshold.

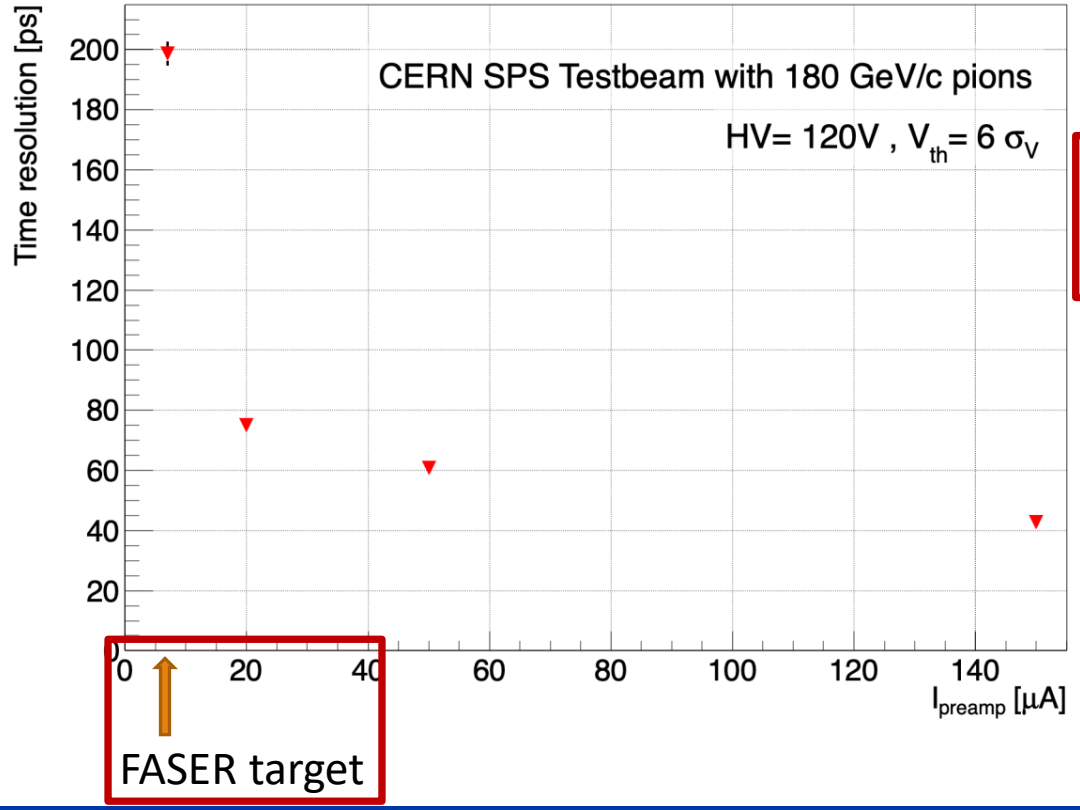
Previous prototypes

Previous development and prototyping





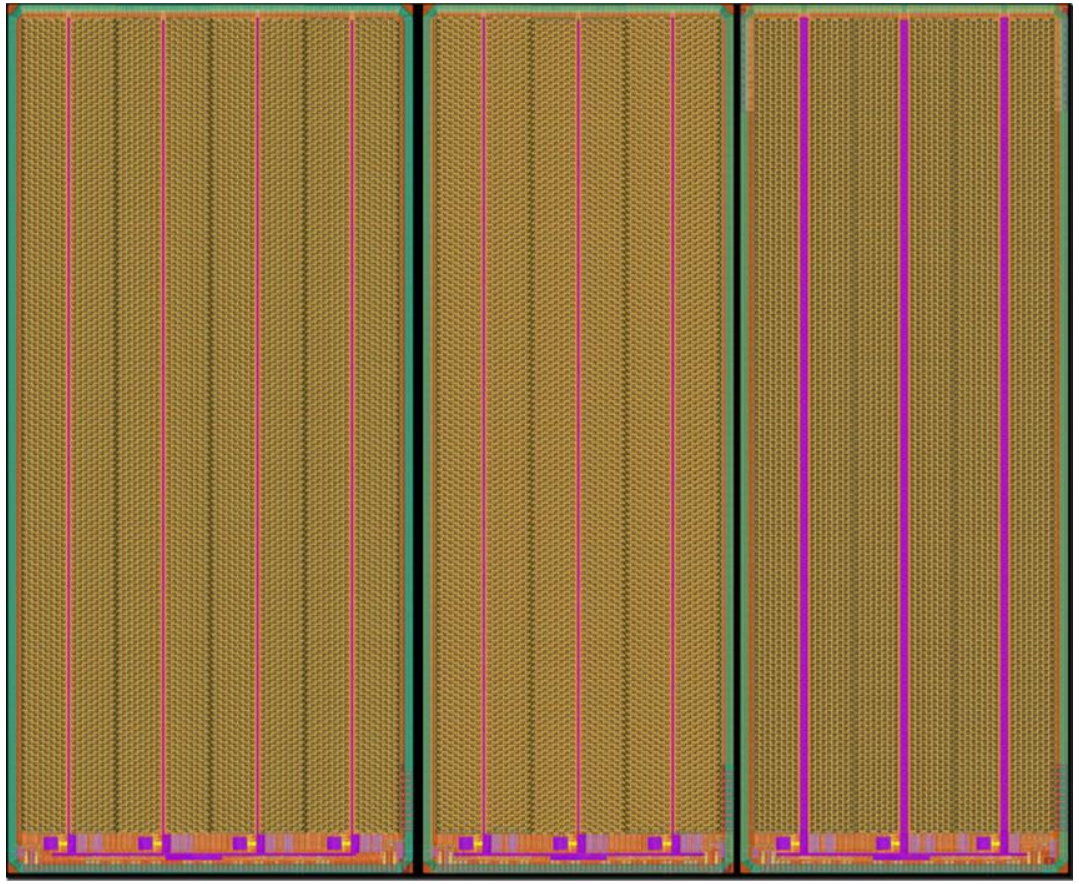
Time resolution to MIPs from test beam measurement.



- Better than 300 ps time resolution expected.
- Not a critical feature, but a nice to have that comes for free.

Pre-production prototypes

Detector ASIC, pre-production:



- **Delivery in March 2022**. Tests start in April.
- Three flavors, with variation of front-end and readout architecture.
- **Final chip will go in production in June 2022**.

Summary

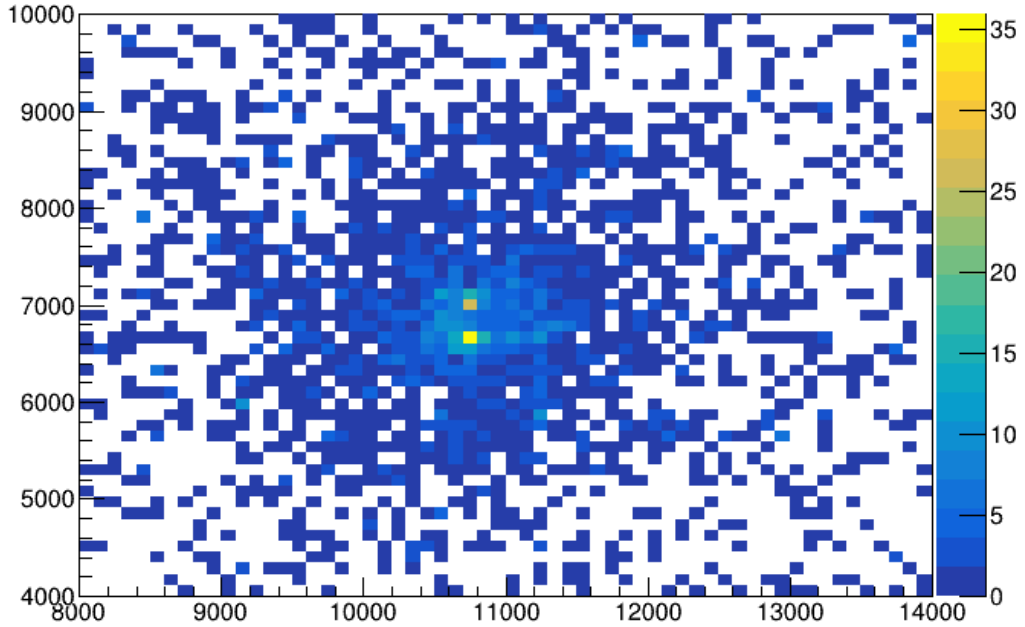
- The new FASER preshower detector will **enable the discrimination of photons** in the final state of LLP decays.
- The design of a monolithic ASIC capable to distinguish clusters from two **ultra-collimated high-energy EM** showers is complete.
- The ASIC will use TOT information with compression of the response to have a **dynamic range ranging from 0.5 fC to 65 fC**.
- The ASIC will use analog memories to store the charge information, enabling the **possibility to read out many pixels at the same time**.
- The new pre-shower will be installed in the winter break 2023/2024 to **take data during LHC Run 3**.

Backup

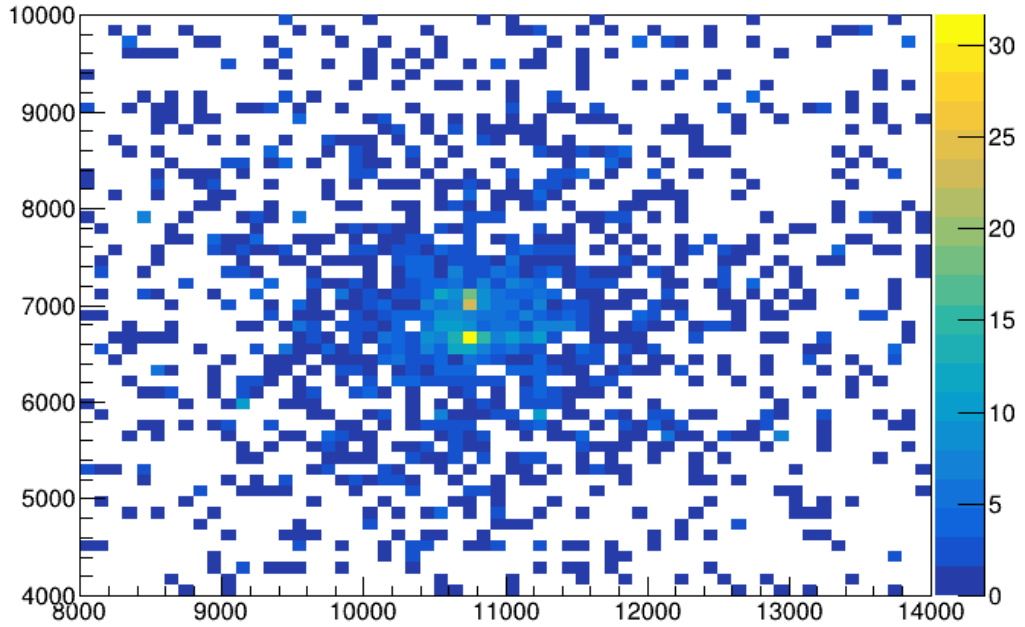
Full detector simulation

- Dedicated module developed for AllPix2, which integrates Monte Carlo simulations from Cadence Virtuoso

Ideal geant4 simulation



Realistic detector simulation



Physics motivations: Physics case

- **Benchmark model: ALP decaying into two photons.**
- LLPs decaying into final states involving neutral pions (light dark scalar boson, sterile neutrino).
- LLPs decaying into all hadronic states: complementary information from the tracker.

Impact on other analyses:

- Improve the precision on the e+e- tracks at the back of the detector: probe lighter/more boosted A'
- May allow to include A' decay after the decay volume, before the 2nd tracking station.
  ⟹ Up to 70% increase in detector volume.
- Adds redundancy to back tracker station.
- Expected impact on the calorimeter energy resolution (under investigation).
  ⟹ Mitigation: use pre-shower data to integrate the energy measurement.
  ⟹ Test beam with pre-production prototype and calorimeter module in August 2022.

No negative impact on FASER new physics searches. Improves 2γ search.

Amalog mux simulation