ATLAS ITk Pixel quad module test beam results

17th (Virtual) "Trento" Workshop on Advanced Silicon Radiation Detectors
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University of Freiburg

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MAX-PLANCK-INSTITUT FÜR PHYSIK

ATLAS EXPERIMENT

Upgrade of the ATLAS experiment

The High-Luminosity LHC (HL-LHC)

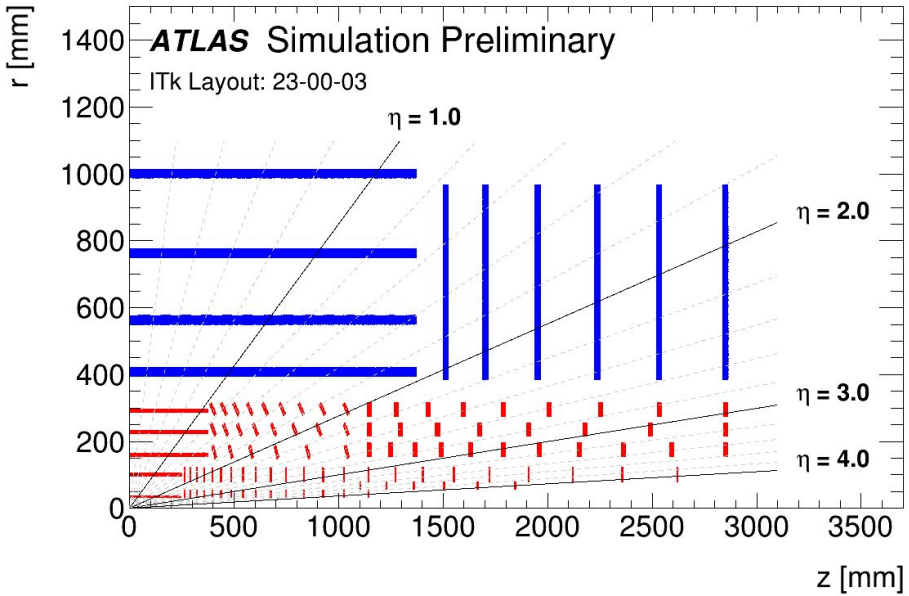
- data taking from 2029
- challenging environment due to increased:
  - instantaneous luminosity
  - pile-up events per bunch crossing
  - radiation damage
- an upgrade of all detector systems of the ATLAS Experiment

The current Inner Detector will be replaced with the **Inner Tracker (ITk)** consisting of silicon **strip** and **pixel** modules.

The ITk Pixel detector will include:

- single-chip 3D sensors in the L0
  - 2x2 cm^2 size;
- quad planar sensors in L1-L4
  - 4x4 cm^2 size.

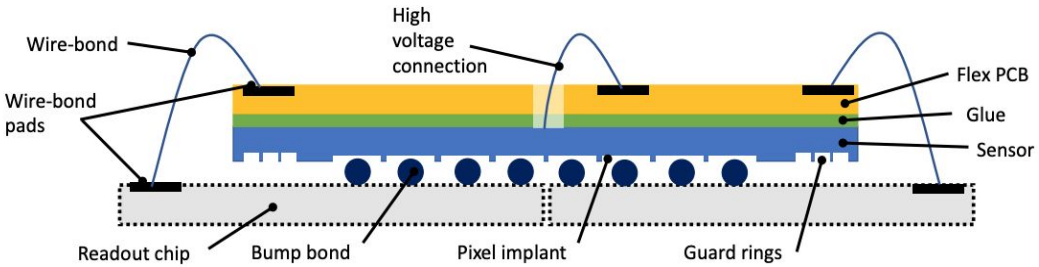
A schematic depiction of the ITk Layout



ATLAS ITk pixel modules assembly and testing

The ITk pixel modules are assembled in two steps:

- **bump-bonding**, where readout chips are attached to the sensor → bare module;
- **module assembly**, where a bare module is connected to the hybrid (flex PCB).

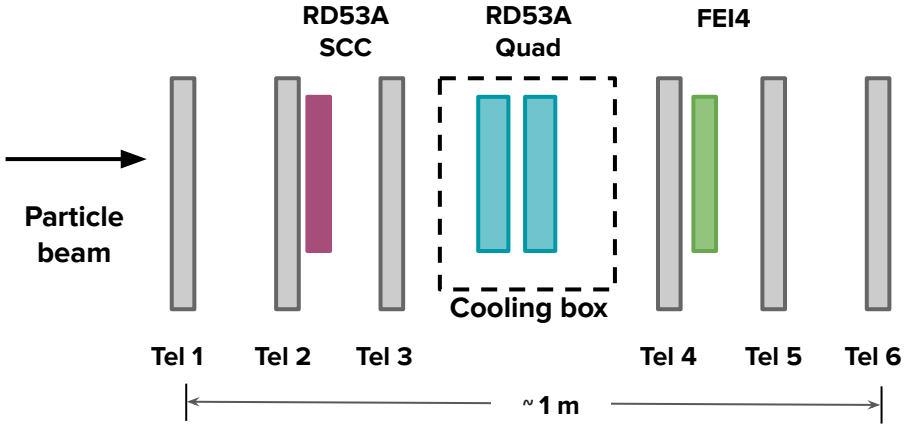


Beyer (2019)

The performance of assembled modules is evaluated in laboratory and **test-beam** measurements.

Experimental setup

- The test-beam measurements are performed at CERN SPS North Area
  - Pion beam of E = **120.0 GeV**
- EUDAQ1 framework is used for the data acquisition
  - Scintillators in coincidence are used for triggering purposes



Beam telescope

RD53A Single chip card (SCC) as a timing reference

FEI4 SCC

RD53A Quad modules with n-in-p planar sensors of 150 µm thickness and 50x50 µm^2 pixel size:

- non-irradiated HPK Q8
- non-irradiated Micron Q2
  - PT biasing structure
- irradiated HPK Q4
  - Fluence: ϕ_{eq} = 5 x 10^{15} n$_{eq}$cm^{-2}

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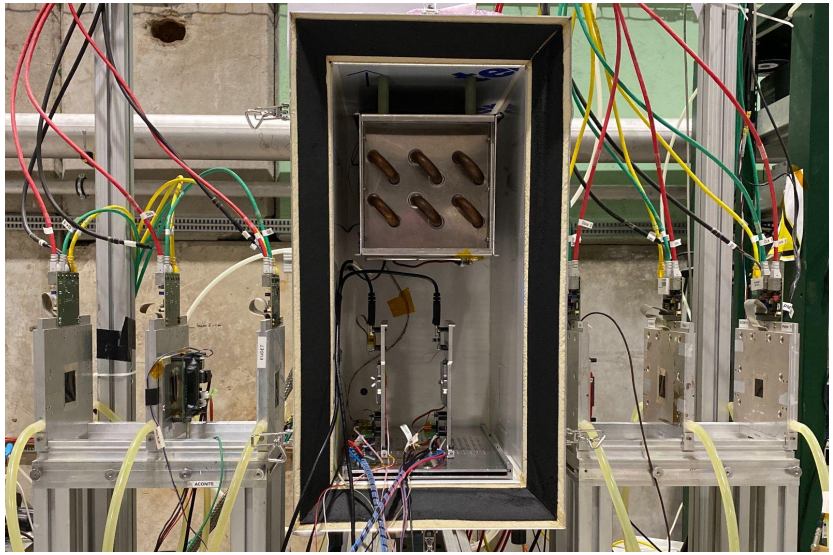
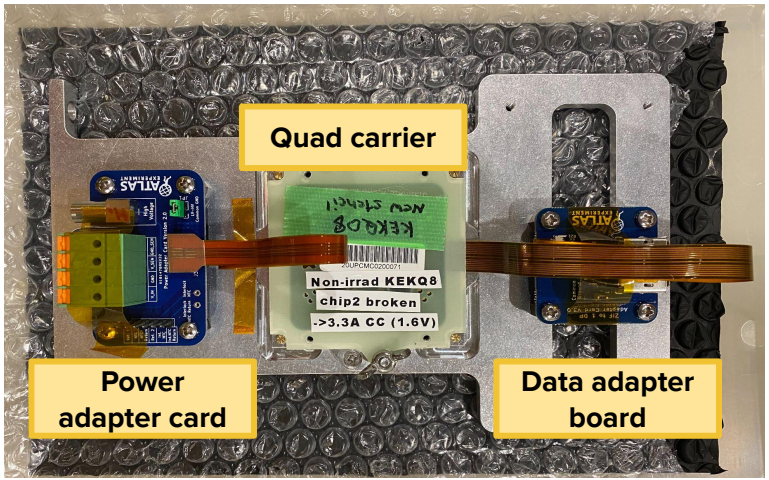


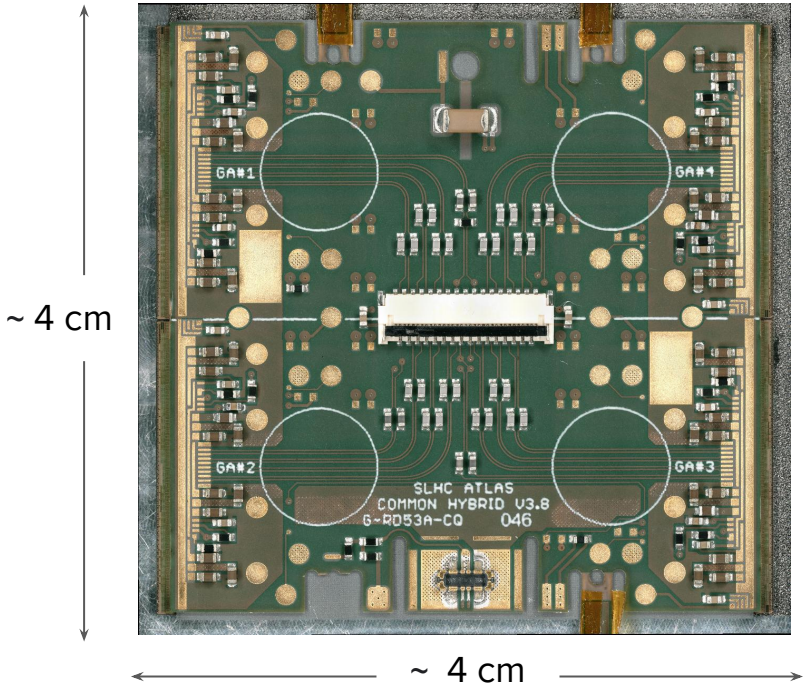
Frame with mounted RD53A quad module



- The position of the module with respect to the beam has been changed in order to scan the different chips

ATLAS ITk RD53A Quad Modules

The layout of the quad module flex PCB



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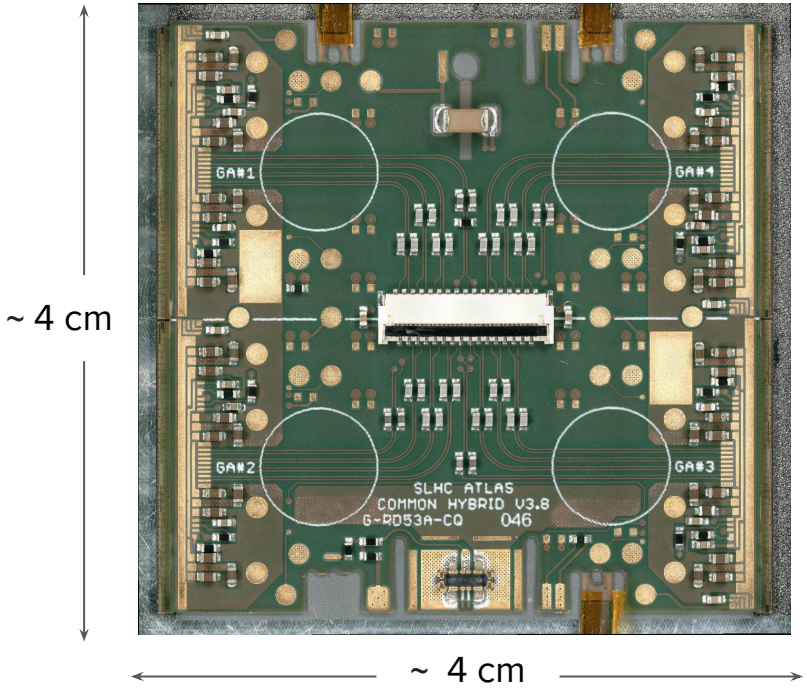
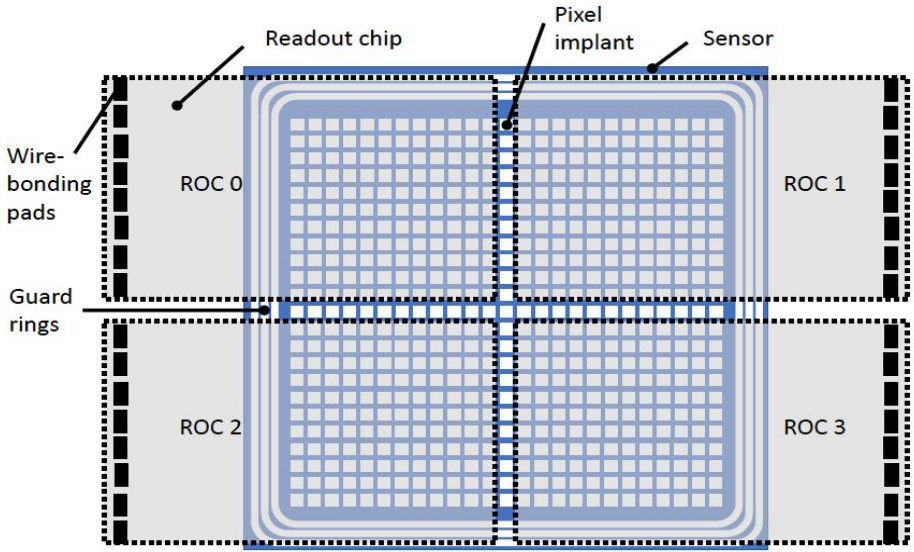
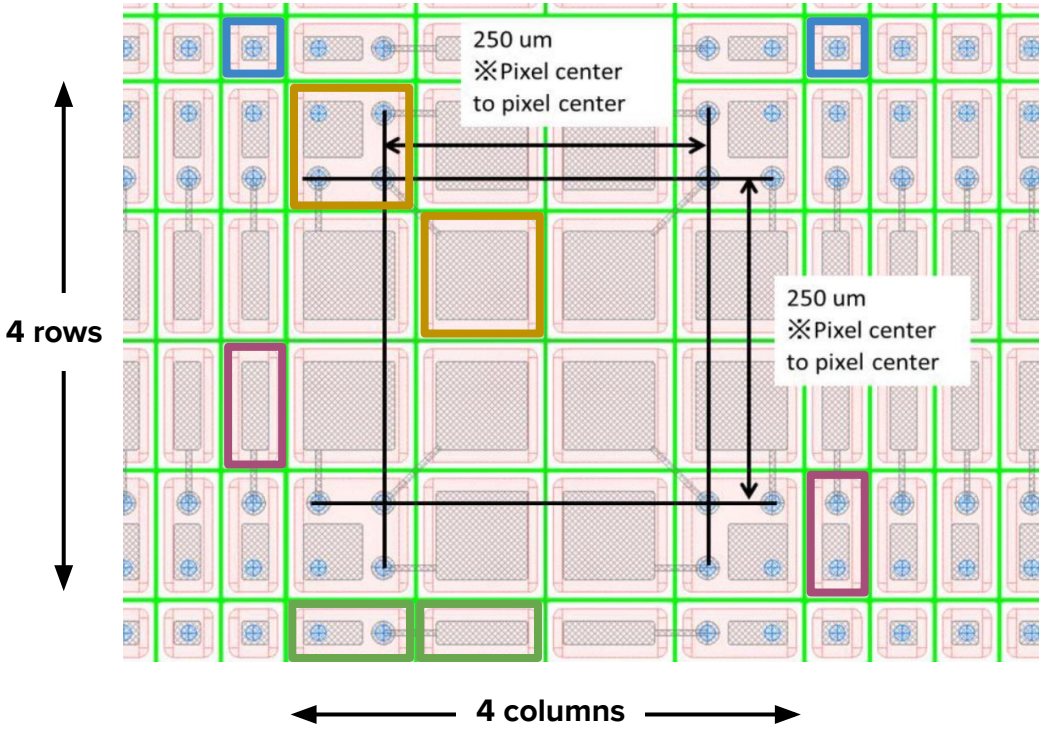


Sketch of quad-module layout



Inter-chip region

- A gap between the four chips bump bonded to the quad sensor
  - Four central columns and rows of the sensor
  - Different pixel size to cover the inter-chip area



Pixel size

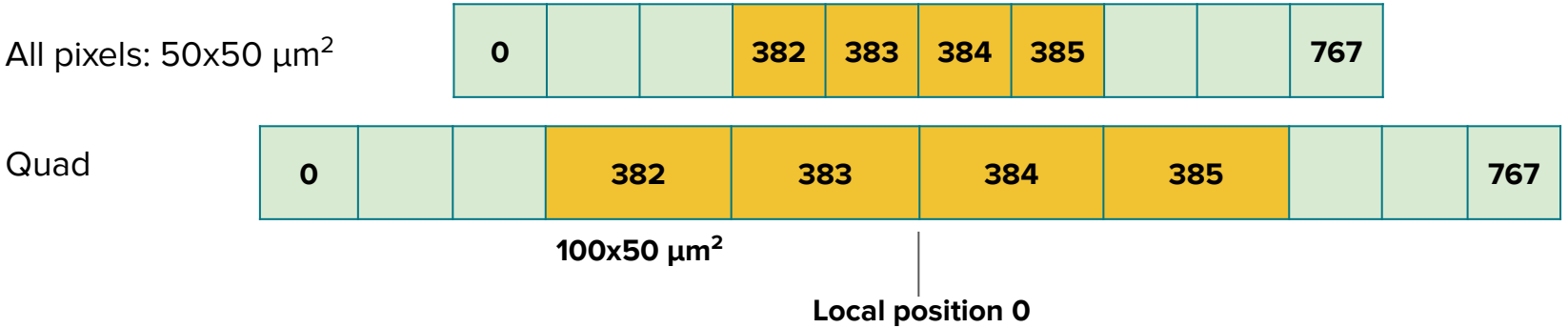
- 50x50 μm^2
- 100x100 μm^2
- 50x100 μm^2
- 100x50 μm^2

Calculation of the local position

- The raw data contain basic pixel hit information: column, row, ToT, LV1 ID
  - Hits close in space are grouped into clusters
  - Column and row of the hit cluster can be converted to the hit position

} In the data reconstruction and analysis software

- The **Corryvreckan** framework is used for the data reconstruction and analysis
  - By default the sensor is expected to have a uniform pixel matrix



- Assuming the hit cluster has column ID: 385

All pixels: 50x50 µm²	Quad
Column: 385 ⟶ Local position: 75 µm	Column: 385 ⟶ Local position: 150 µm

Pixel number refers to the center of the pixel

New geometry class and analysis module

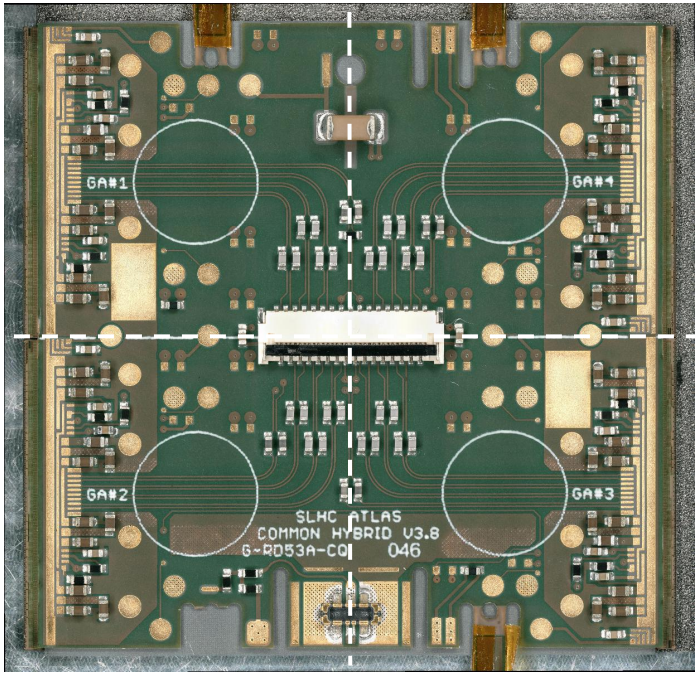
- New geometry class implemented in the Corryvreckan framework - **ITkPixQuad** - where the following functions were modified according to the quad geometry:
  - Calculating the local position based on the column and row;
  - Getting the row and column from the local position;
  - Calculating the size of the detector;
  - Calculating in-pixel position from column/row and local position;

- New analysis module created in the Corryvreckan framework - **AnalysisITkPixQuad** - which can be used to determine:
  - Hit efficiency;
  - Residual distribution in X/Y;
  - Cluster size distribution in X/Y.

  All quantities can be determined separately for:
  - 50x50 μm^2 size pixels;
  - the inter-chip region.

RD53A Quad module layout

- Readout system: hits recorded per chip
- EUDAQ converter: the data from four chips (on quad module) combined into one detector plane
- Corryvreckan framework: the data read in per detector plane



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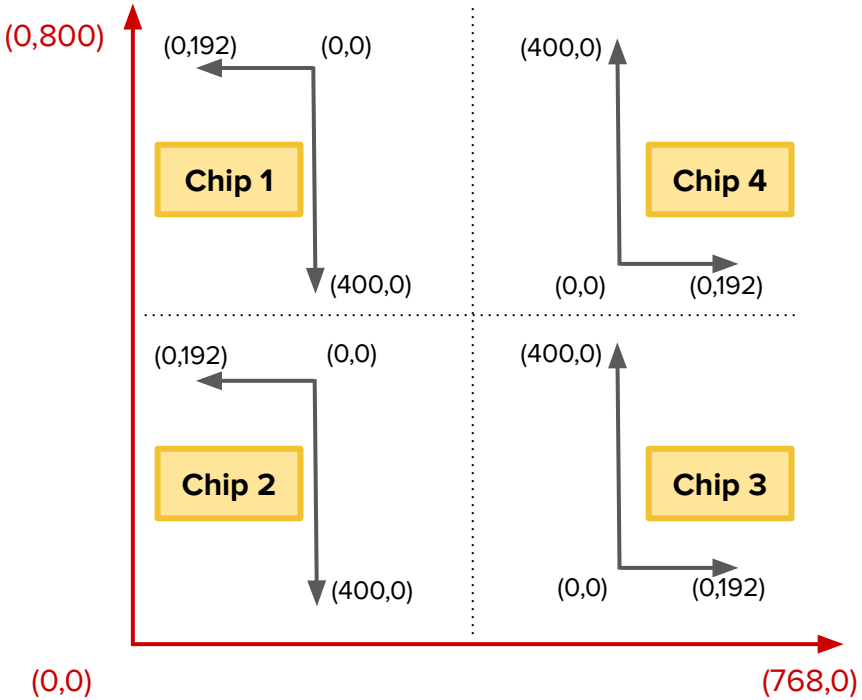

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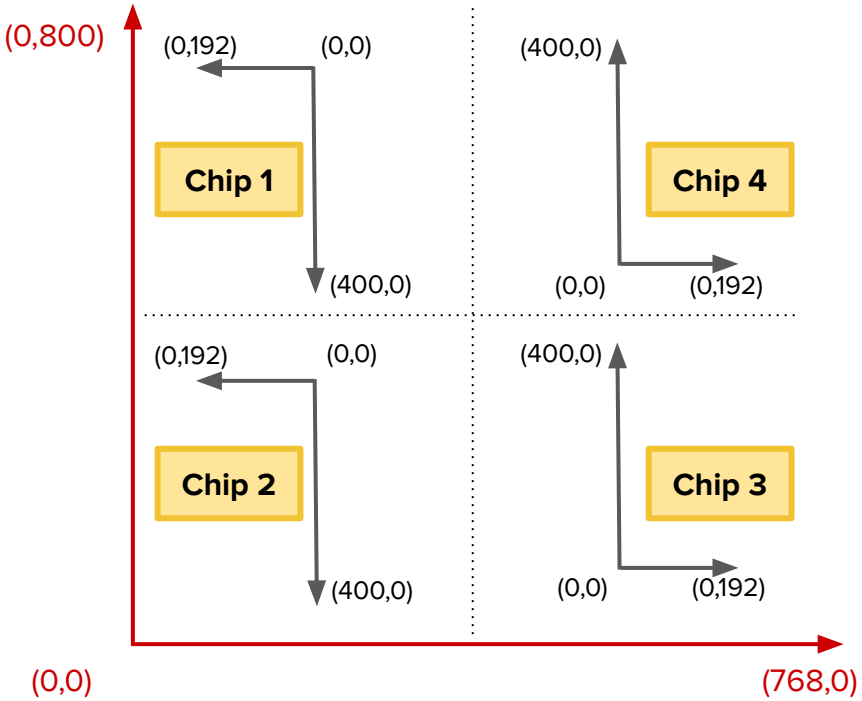
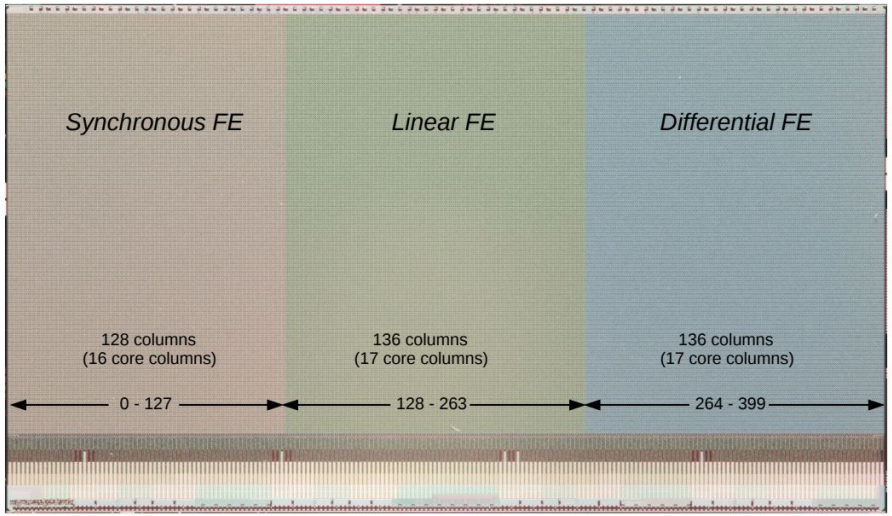


Front end flavors in RD53A chip



- RD53A chip is half size of the final chip

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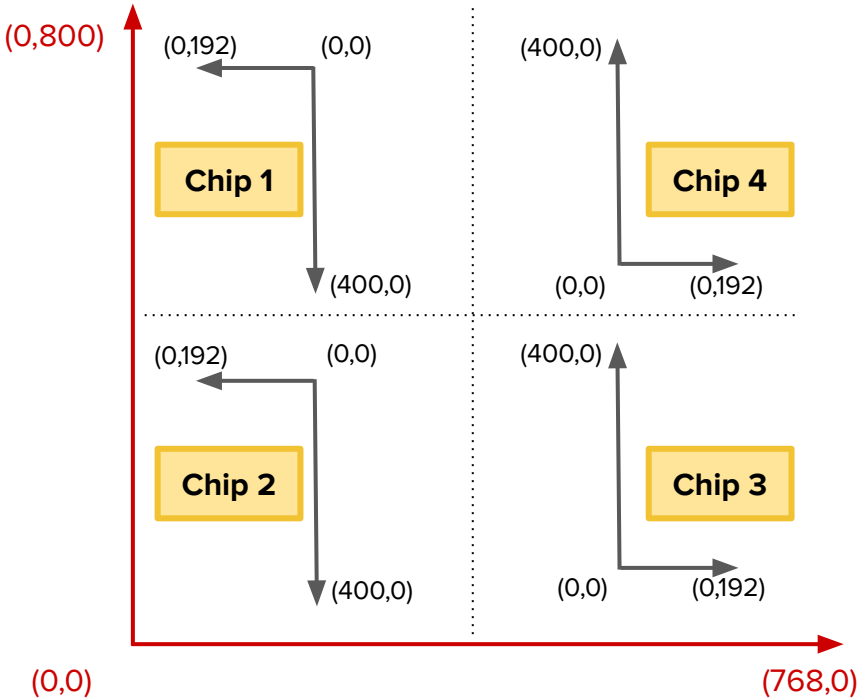

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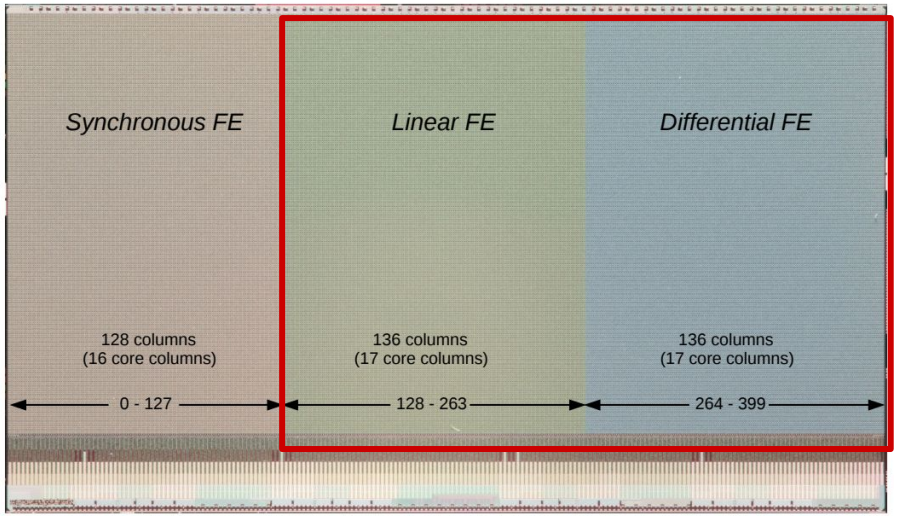
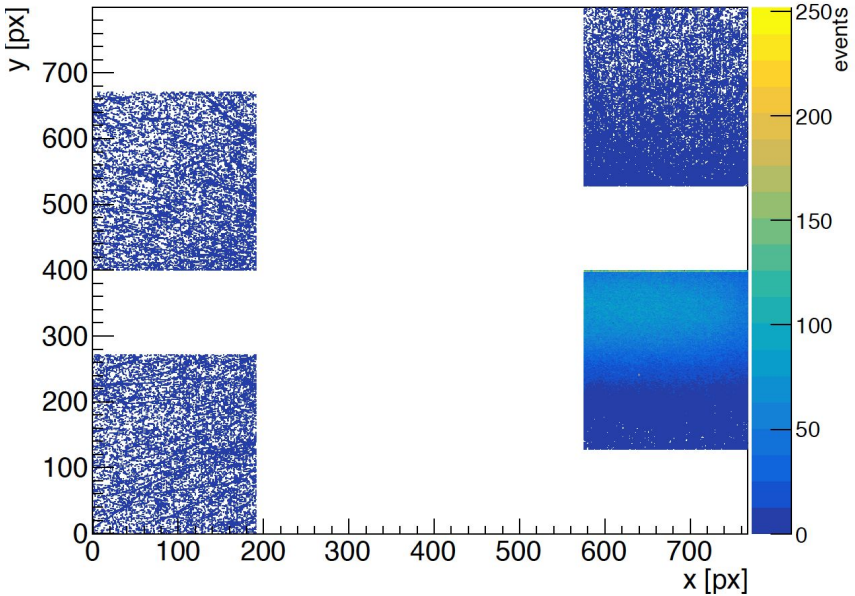


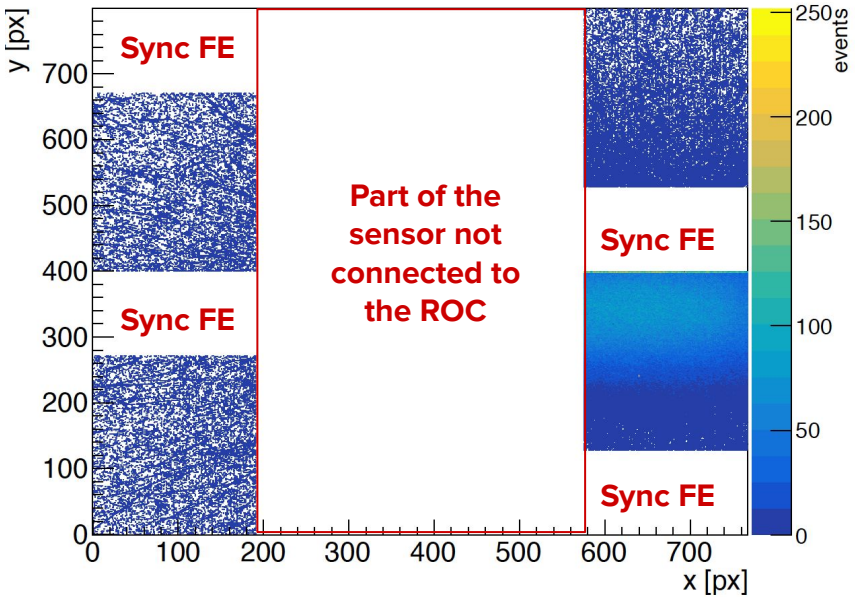
- RD53A chip is half size of the final chip
- Synchronous FE is not used for the data taking

Hit map example



- Box positioned so that the beam is focused on chip 3

Hit map example



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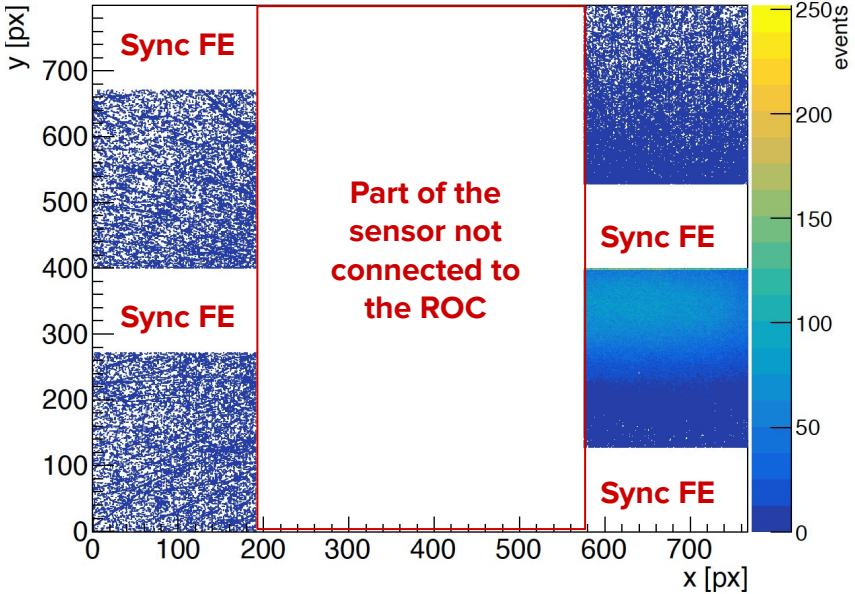

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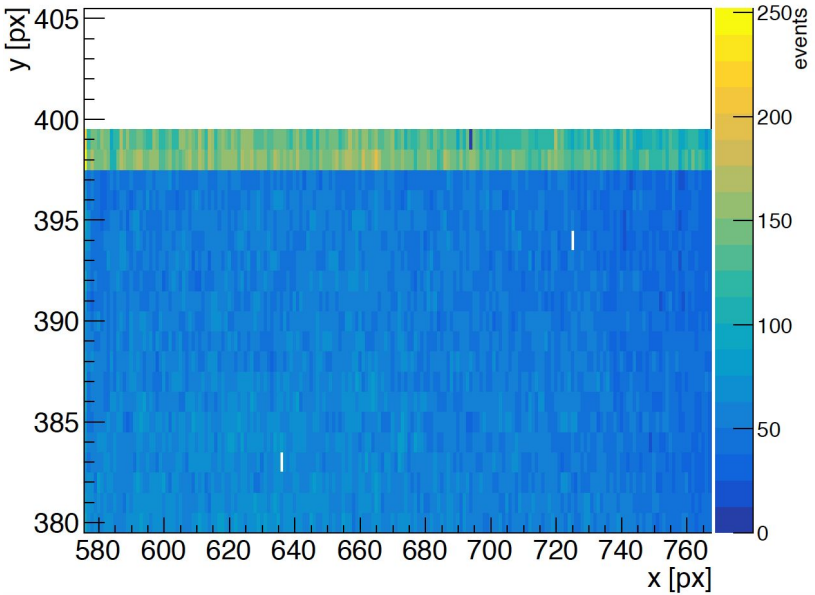
Chip 3



Row **398 and 399:** 50x100 μm^2 pixels - twice as many hits compared to other pixels

Hit efficiency measurement

- **Track reconstruction**
  - A hit on the reference DUT (timing reference) required
  - The LV1 ID information of the hit from the reference DUT is used as the track timestamp
  - Tracks with a timestamp within LV1 limits are considered for the analysis

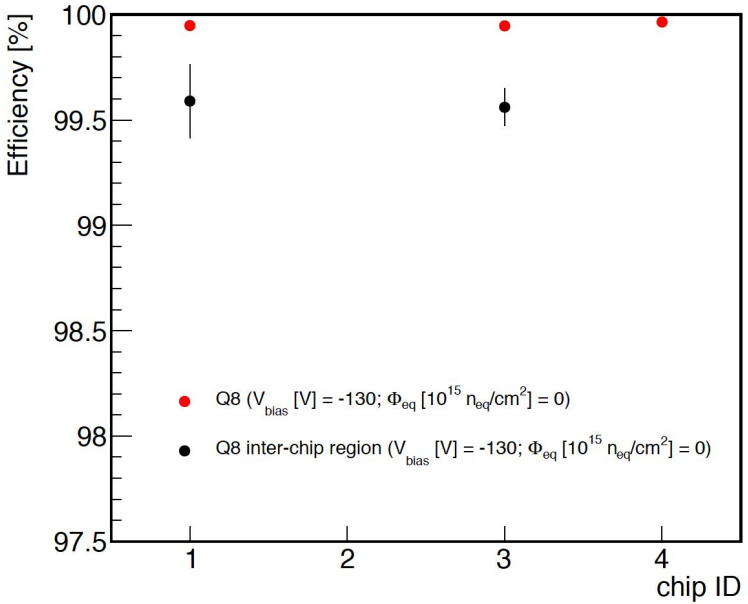
- **DUT cluster association**
  - Clusters on quad modules are assigned to the reconstructed tracks if they are within specified spatial limits
  - Spatial limits: *2*pixel pitch* in both directions

- **Hit efficiency**

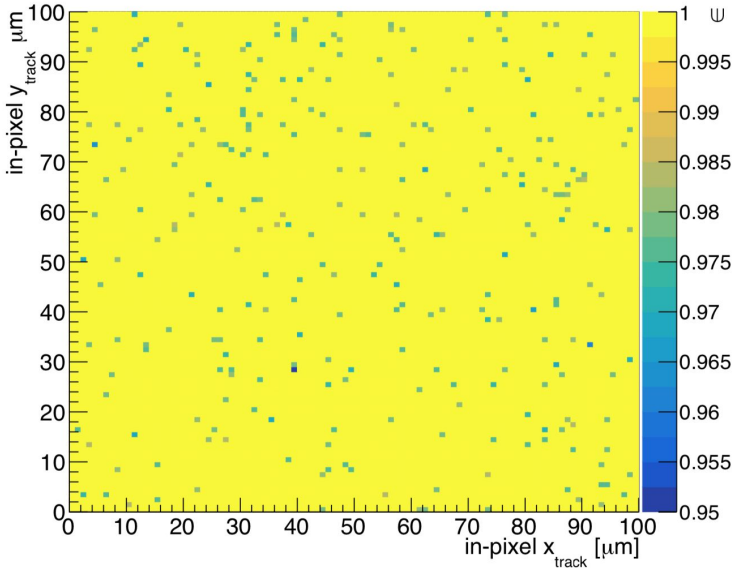
$$\varepsilon = \frac{\text{number of tracks with an assigned cluster on the DUT}}{\text{total number of tracks intersecting the DUT}}$$

DUT - Device Under Test

HPK - Q8



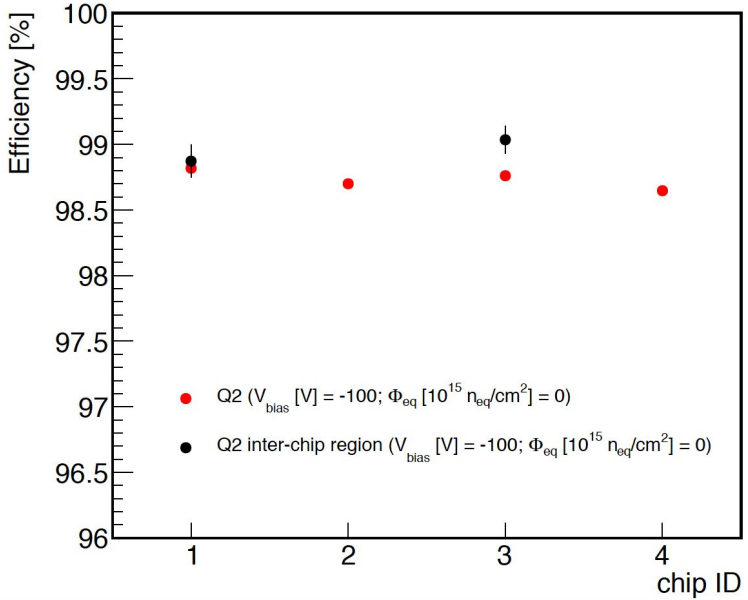
Hit efficiency map



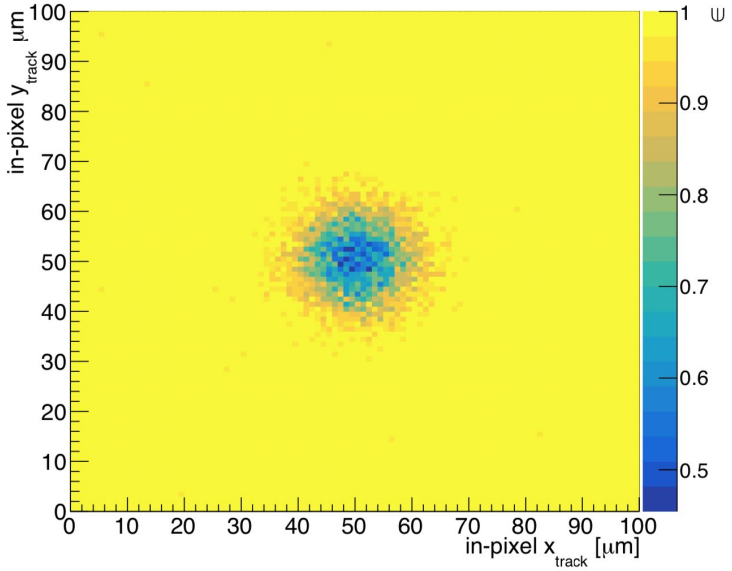
Bias voltage: -130 V

- Chip 2 was disabled
- Hit efficiency > **99.9%** for all 3 measured chips
- Inter - chip region: only column 398 on the chip considered
  - Determined hit efficiency > **99.5%**

Micron - Q2



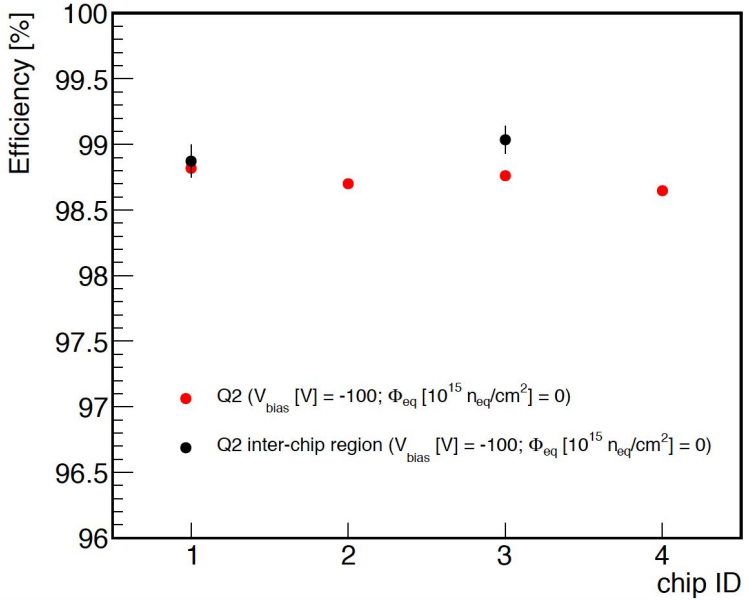
Hit efficiency map



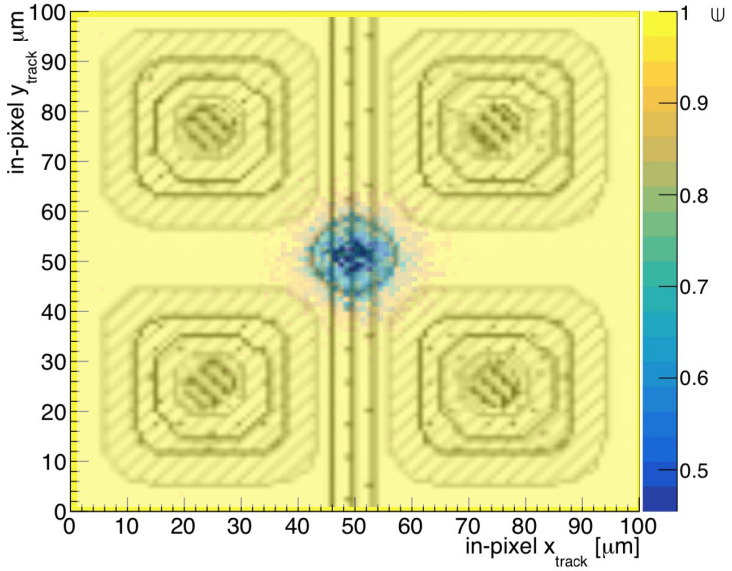
Bias voltage: -100 V

- Hit efficiency > **98.5%** for all 4 measured chips
- Inter - chip region: columns 398 and 399 on the chip considered

Micron - Q2



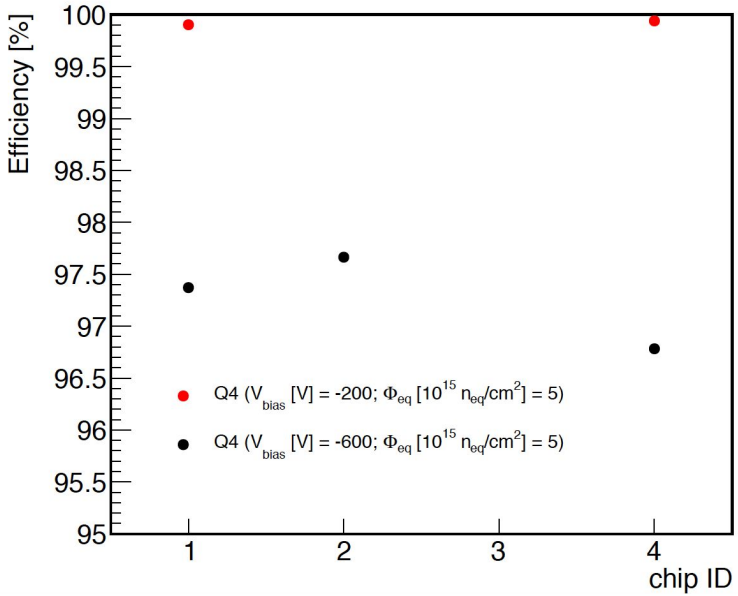
Hit efficiency map



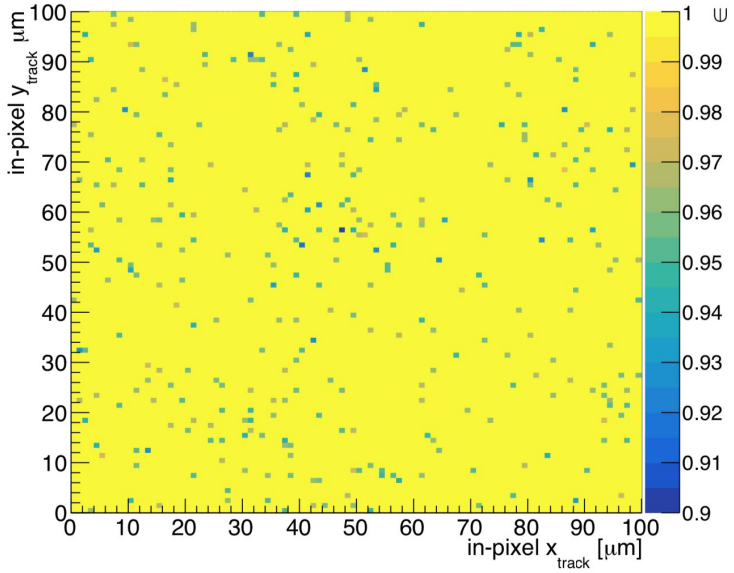
Bias voltage: -100 V

- Hit efficiency > **98.5%** for all 4 measured chips
- Inter - chip region: columns 398 and 399 on the chip considered

HPK - Q4



Hit efficiency map

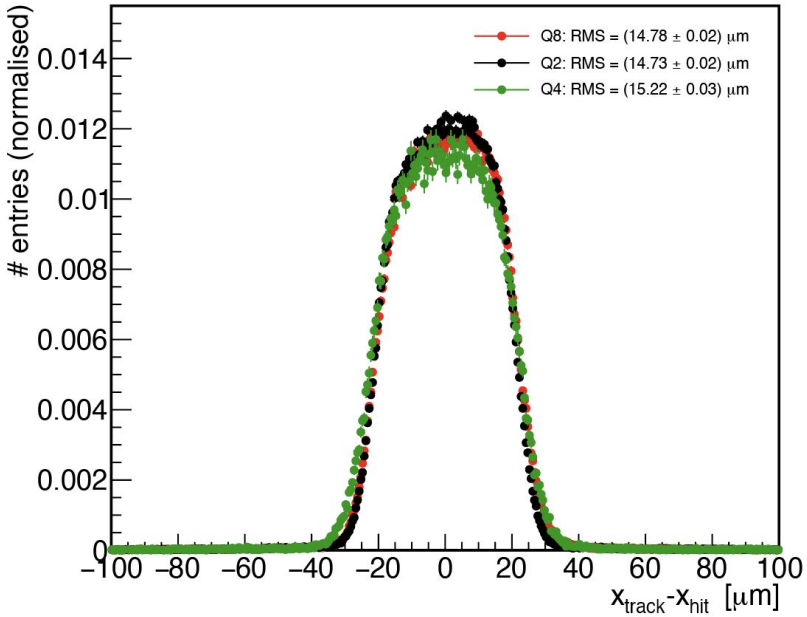


Bias voltage: -600 V

- Chip 3 was disabled
- Hit efficiency around **97%** at - 200V
- Hit efficiency **~ 99.9%** at - 600V
  - Measurement was not performed on chip 2 due to noise.

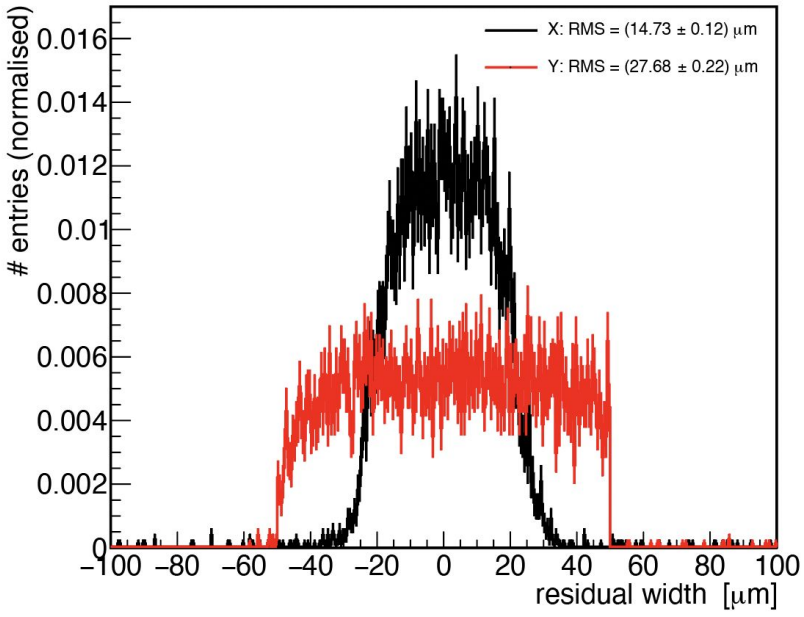
Residual distribution

50x50 µm² pixels: X dimension



Unbiased residuals $r^2 = \sigma^2_{int} + \sigma^2_{tel}$

Q8: inter-chip region



Pixel size: 50x100 µm²

Summary

- 3 RD53A quad modules have been successfully measured during the test-beam campaigns in 2021
  - Two non - irradiated quad modules;
  - One irradiated quad module.

- The data is reconstructed and analysed using the Corryvreckan framework
  - The further development of the framework was performed to allow the analysis of sensors with non-uniform matrices.

- Determined efficiency is within the requirements for the ITk planar sensors
  - Non-irradiated modules > 98%
  - Irradiated modules > 97%
- The functionality of the inter-chip region is verified
- The residual distribution for three measured quads is compatible with the expectation for 50x50 μm^2 size pixels and the inter-chip region