Development of a backside biased HV-CMOS sensor in a 150 nm process node for particle detection

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Motivation: HV-CMOS Sensor: Radiation Tolerance

Existing HV-CMOS sensor radiation performance achieved so far compared to other experiments:

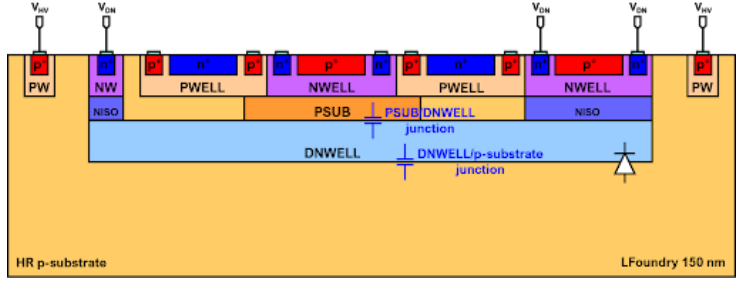
	FCC-hh	HL-LHC	HV-CMOS performance
Radiation tolerance	10^{16} - 8x10^{17} n_{eq} /cm^2	10^{16} n_{eq} /cm^2	2 × 10^{15} n_{eq}/cm^2
Pixel size	$25 x 50 \mu m^2$	$50 x 50 \mu m^2$	$50 x 50 \mu m^2$

Design and measurements I am going to present:

1.Test structures used to measure IV for high radiation tolerance.

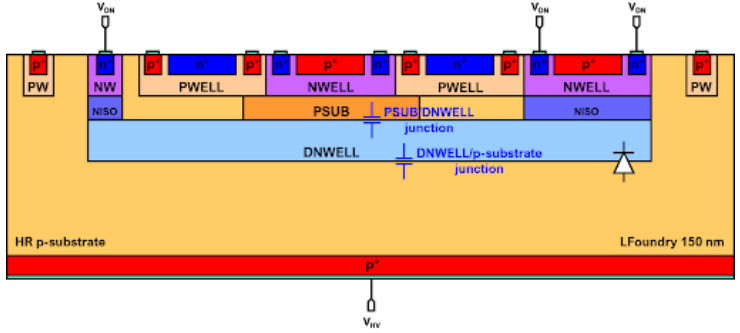
2. Circular transistors to mitigate leakage current and hence to obtain higher radiation tolerance.

High Voltage Biasing Configuration



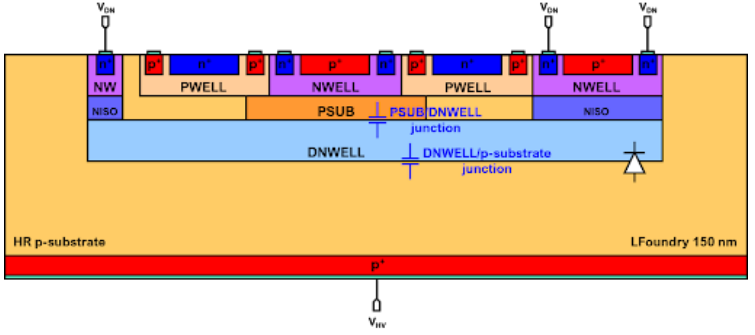
(1) Topside Biasing

- Standard substrate biasing in HV-CMOS sensors.



(2) Backside biasing with floating contact on top

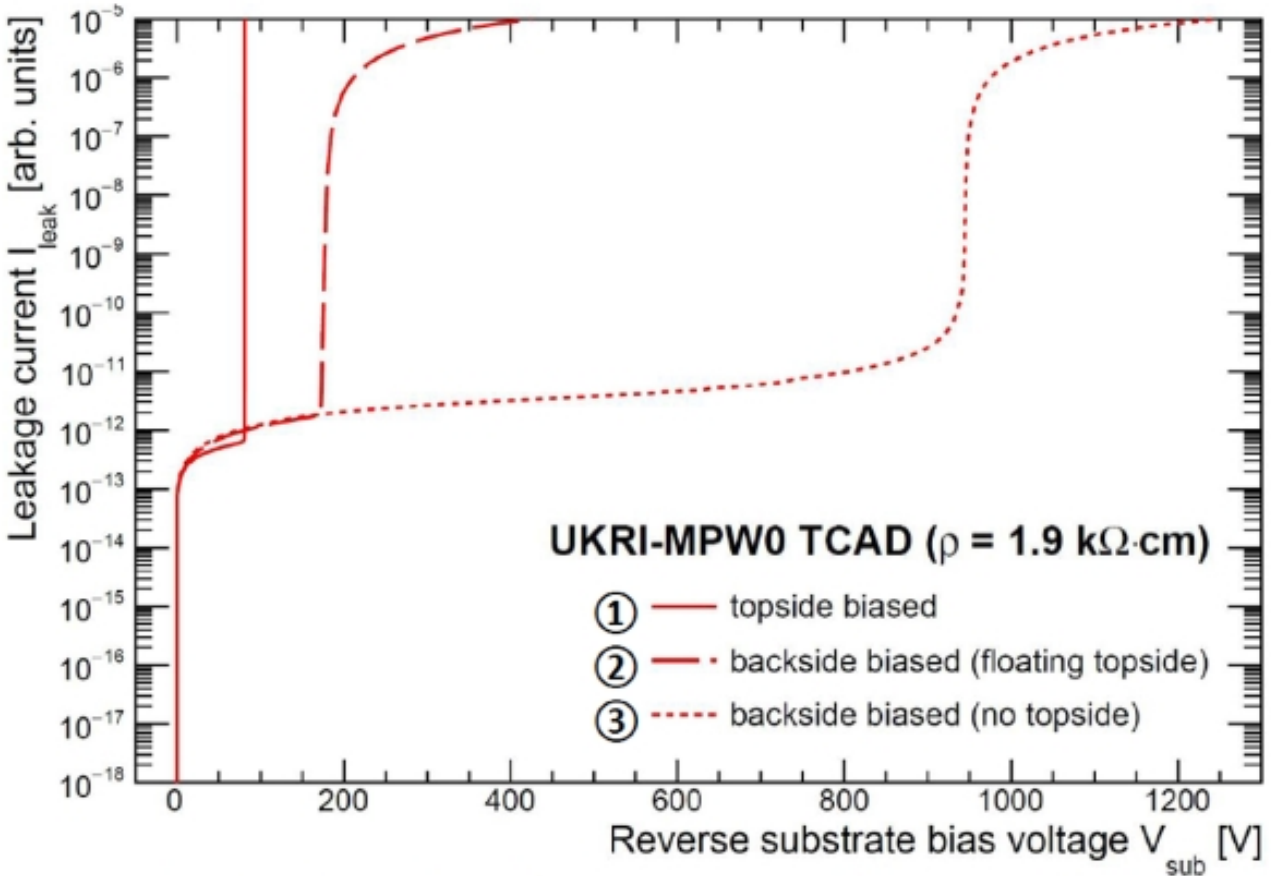
- Improved radiation tlerance upto 10^{15} $n_{eq}.cm^{-2}$ on thin substrate (doi:10.1016/j.nima.2018.07.022)



(3) Backside biased pixel with no topside contacts

SELECTED CONFIGURATION

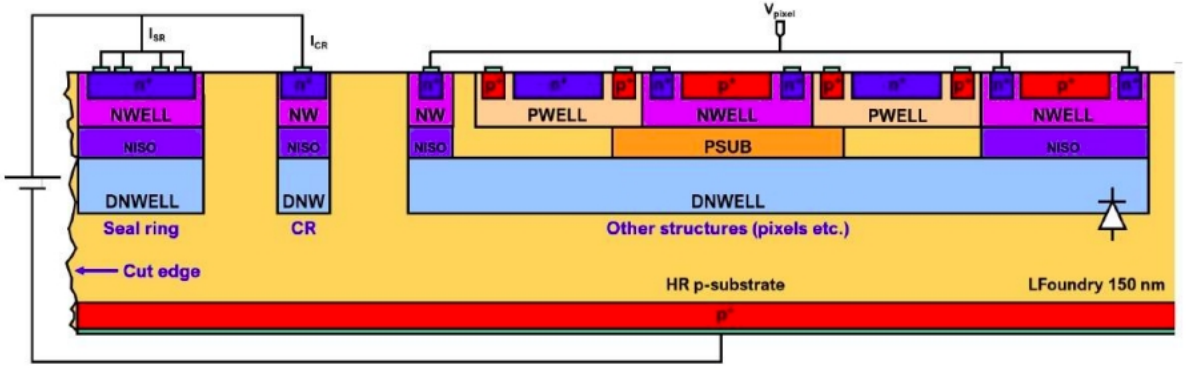
Simulations for High Voltage Biasing Configuration



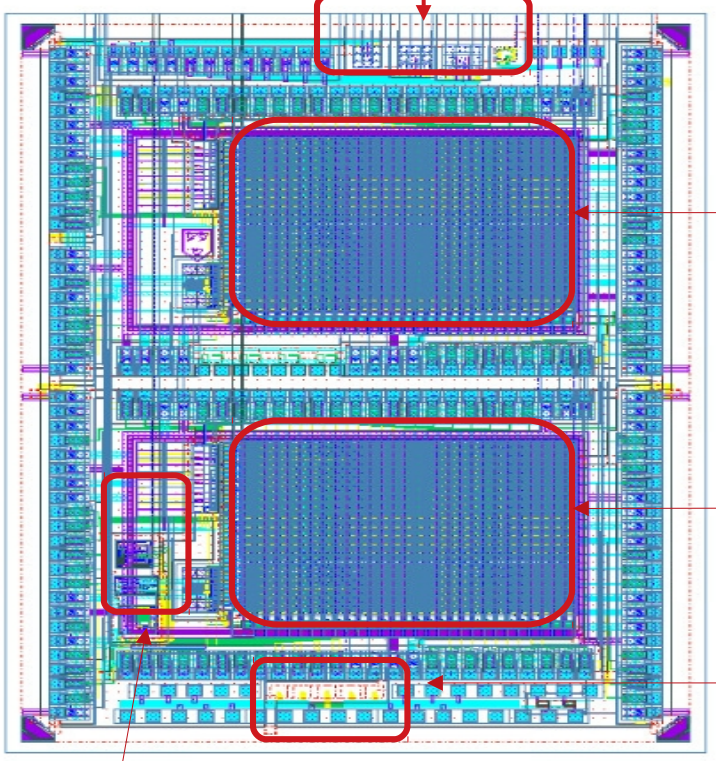
Simulated I-V curves using TCAD (By M. Franks)

UKRI-MPW0 – Chip cross-section with rings

Chip ring is a current terminating structure.
From chip edge and inwards:
– **Current Terminating Ring (CTR)** Collects the major part of the cut edge generated current (I_LEAK ↑)
– **Clean-up Ring (CR)** Collected I_LEAK is only a small fraction of the edge current and bulk current
Decouples high leakage current generated at the detector cut edge from sensing pixels
– Current terminating ring and clean-up ring are biased to the same potential
– In our case the current terminating ring works, as well, as a seal ring to protect the design from the mechanical stress and dirt generated during dicing

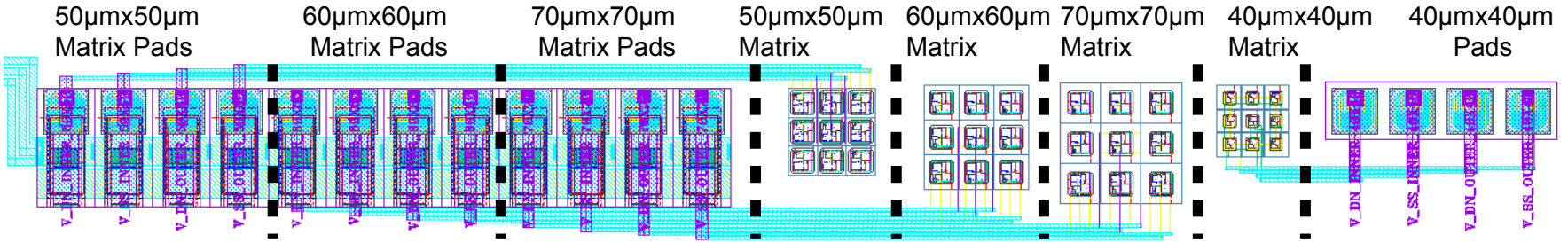


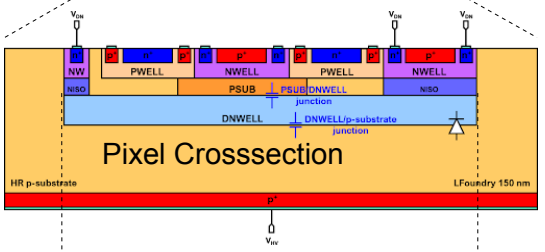
UKRI-MPW0 (Proof of Concept) Chip Layout

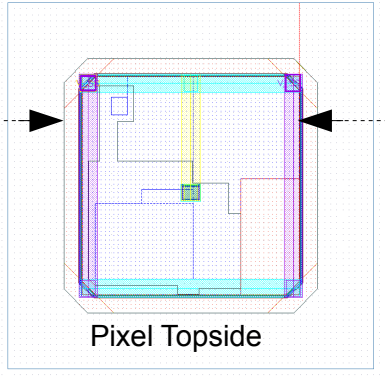


- *Two wafers with 1.9kΩ·cm resistivity.*
- *Samples are thinned to 280 µm*
- *Wafer 1 backside processed using plasma immersion ion implantation with laser annealing and*
- *Wafer 2 backside processed using beamline implantation with rapid thermal annealing*

Teststructures Pixel Matrices

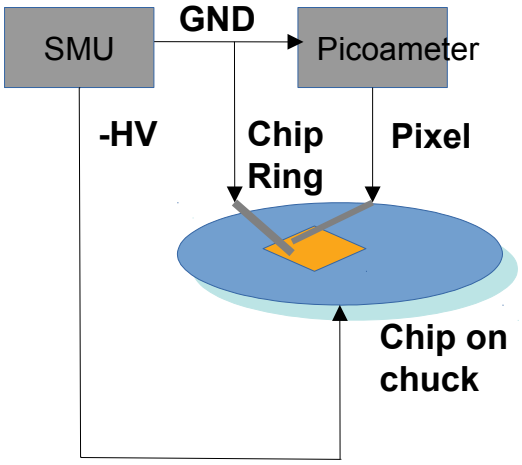




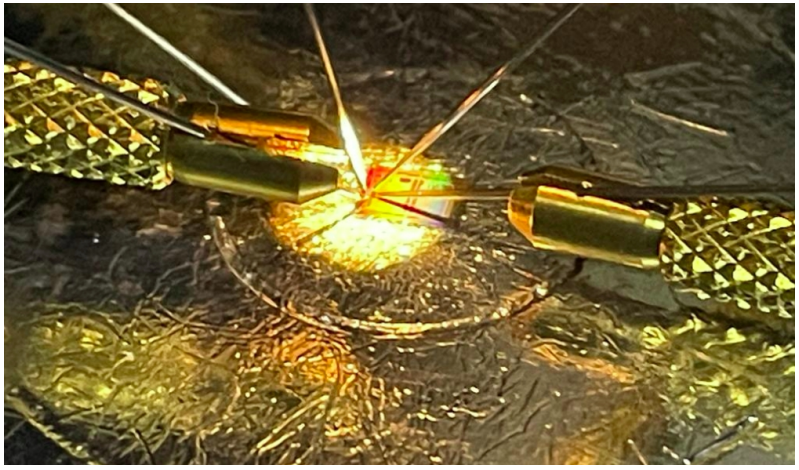


Pixel size [µm x µm]	DNWELL size [µm x µm]	DNWELL-DNWELL spacing [µm]
50 x 50	41.66 x 41.66	8.34
60 x 60	41.66 x 41.66	18.34
70 x 70	41.66 x 41.66	28.34
40 x 40	21.66 x 21.66	18.34

Connection for the Measurement

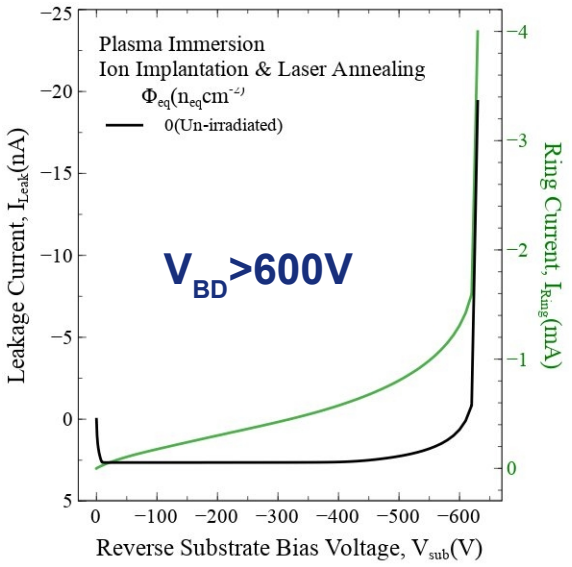


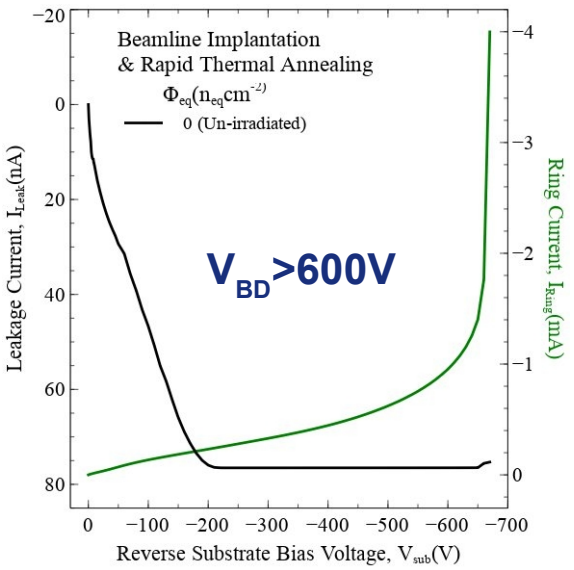
Connection to measure IV



Measuring IV using probe station needle

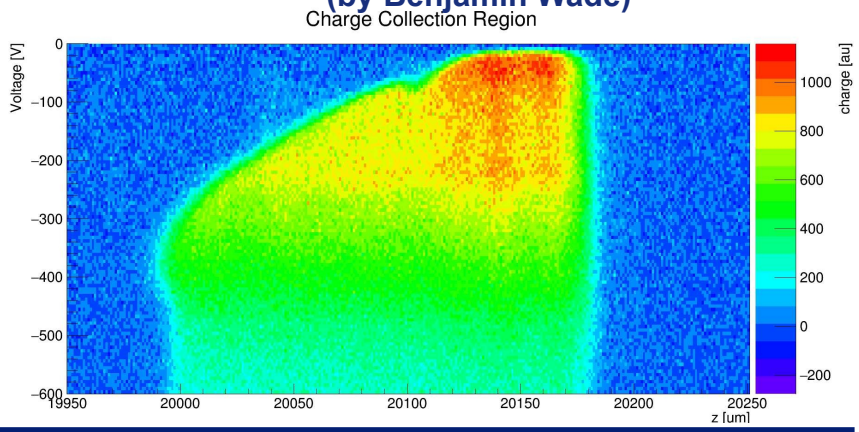
I-V of Test Structure Diodes before Irradiation



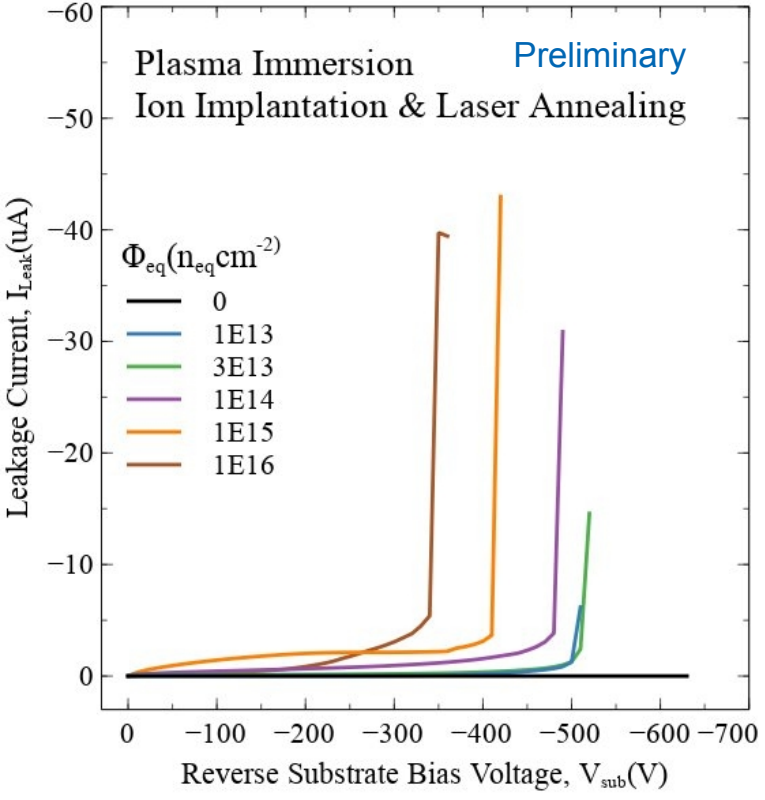


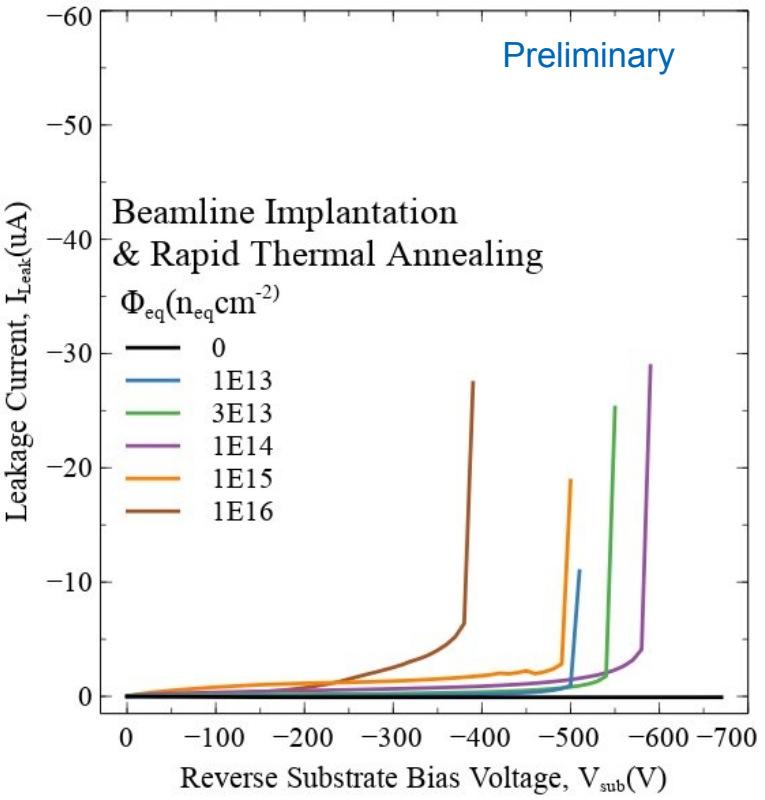
Currently eTCT is being performed

(by Benjamin Wade)



I-V of Test Structure Diodes after Irradiation





- Leakage current increases as expected from silicon sensors It is dominated by bulk current.
- We don't see leakage current > 0, but this is still there most likely.

Breakdown Voltage, V_{BD}

Annealing Type	Fluence (n_{eq}/cm^2)	V_BD (When current reached compliance)	V_BD (k Method)	V_BD (ILD Method)
Plasma +Laser	0	630.00	620.03	620.03
	1.00E+13	510.00	500.00	500.00
	3.00E+13	490.00	470.05	470.05
	1.00E+14	490.00	480.05	480.05
	1.00E+15	420.00	410.03	410.03
	1.00E+16	360.02	340.02	340.02

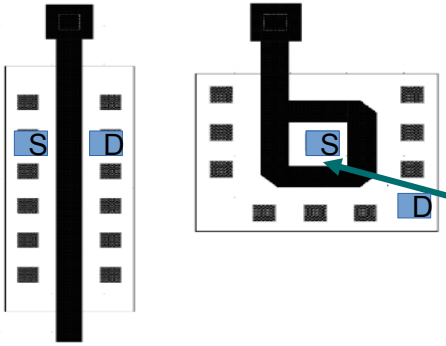
Two parameters calculated in order to determine breakdown voltage

$$k = \frac{dI/dV}{I/V}$$

$$ILD = \frac{1}{I} \cdot \frac{dI(V)}{dV}^{-1}$$

Annealing Type	Fluence (n_{eq}/cm^2)	V_BD (When current reached compliance)	V_BD (k Method)	V_BD (ILD Method)
Beamline +RTA	0	670.00	670.00	670.00
	1.00E+13	510.00	500.04	500.04
	3.00E+13	550.00	540.00	540.00
	1.00E+14	590.00	580.00	580.00
	1.00E+15	490.00	480.00	480.00
	1.00E+16	390.04	380.04	380.04

Why we use Encl. Layout Transistors (ELT)



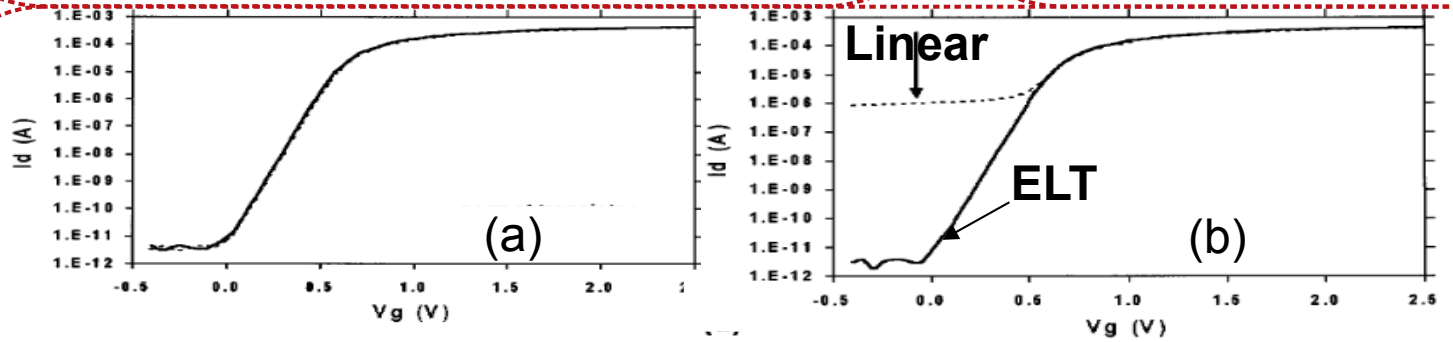
Xue, Fan, *et al* Journal of Semicond. 32.8 (2011): 084002.

(a) Linear transistor & (b) radiation-hardened enclosed layout transistor

ELTs

- are annular transistors.
- In radiation environment prevents the onset of leakage current.
- source in the middle brings the substrate contact closer to the source and reduces the leakage current.
- Less gate oxide ionization.

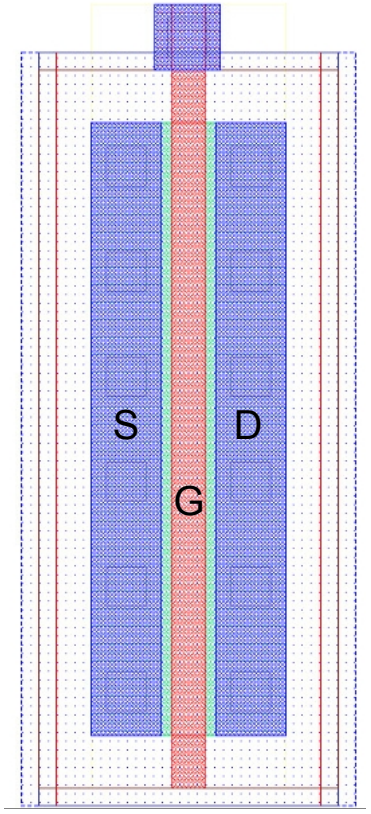
Design challenge: ELTs may require huge space due to big aspect (W/L) ratio.



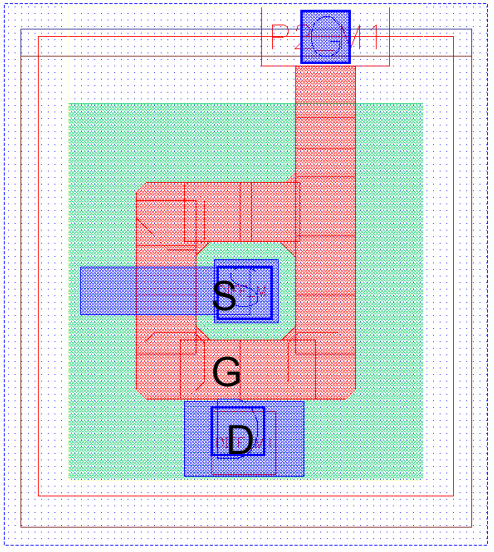
Snoeys et al. (2002). IEEE Trans. on Nucl. Sci. 49. 1829 - 1833. 10.1109/TNS.2002.801534.

(a)ELT & Linear Transistor measurements prior to irradiation (b)ELT & Linear Transistor measurements after irradiation

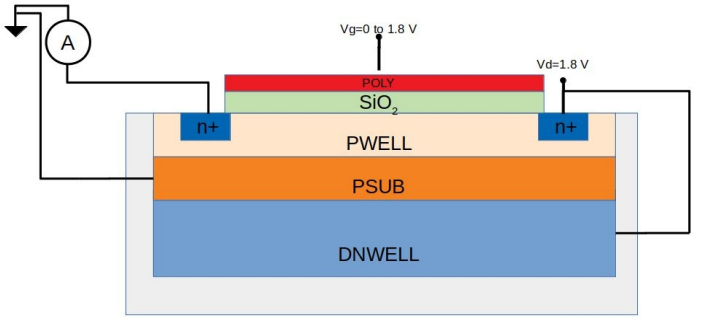
UKRI-MPW0 ELT Teststructure



Linear Transistors



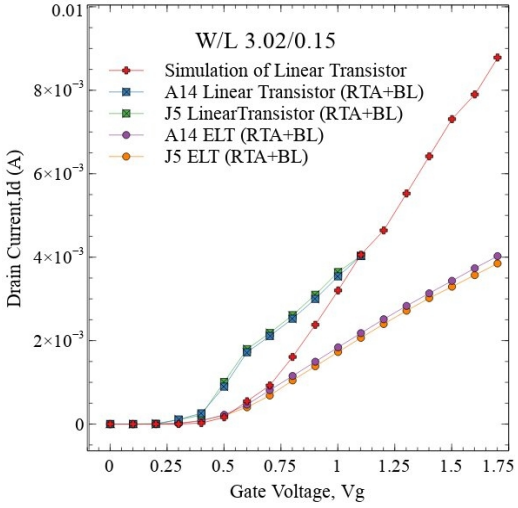
ELT



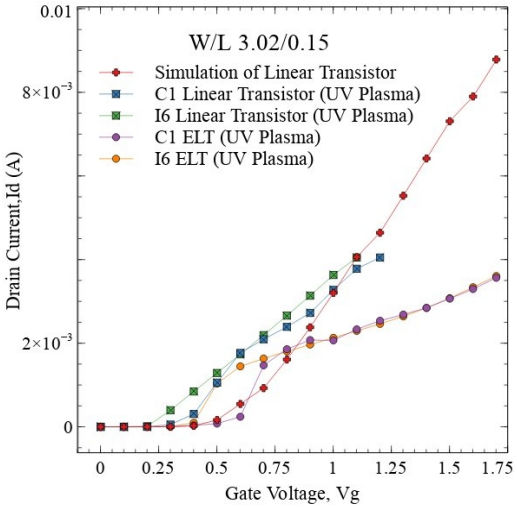
Conection for the Test

- Designed & measured ELT and Linear transistors with two different dimensions, two different implantation processes.
- The unirradiated measured results are in close proximity with the simulated values.
- Next task-TID irradiation.

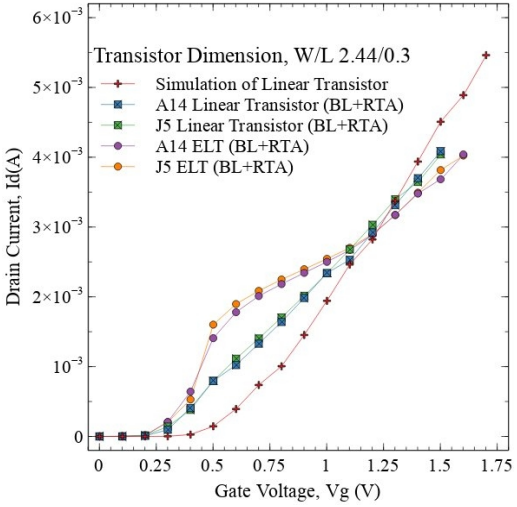
Transfer Curve for ELT and Lin. Transistors



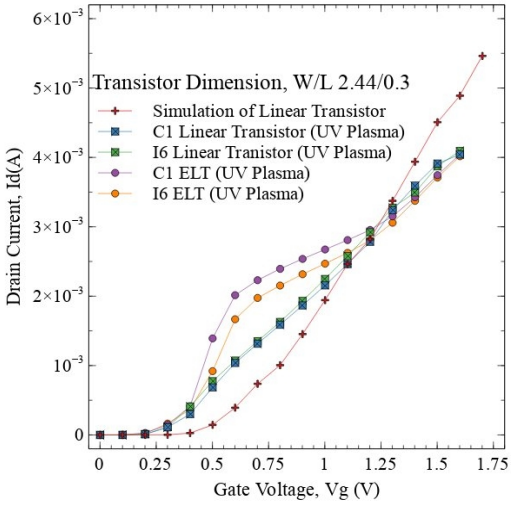
Beamline Implantation+ Rapid Thermal Annealing



Plasma Immersion, Ion Immersion and Laser Annealing



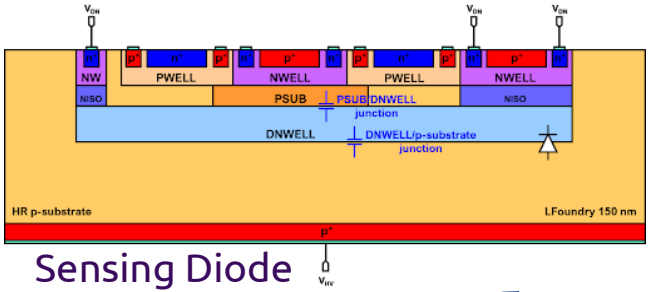
Beamline Implantation+ Rapid Thermal Annealing



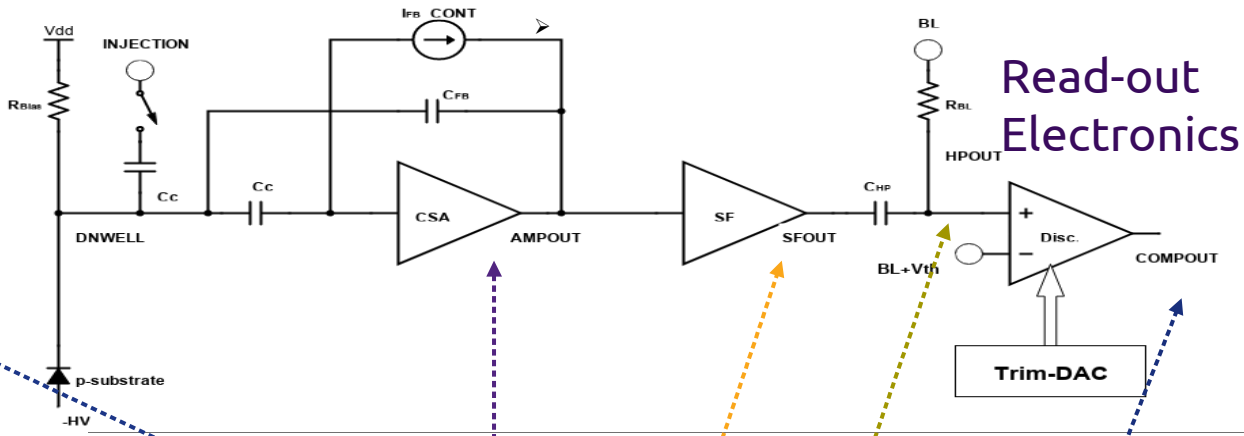
Plasma Immersion, Ion Immersion and Laser Annealing

Note: These results are before irradition

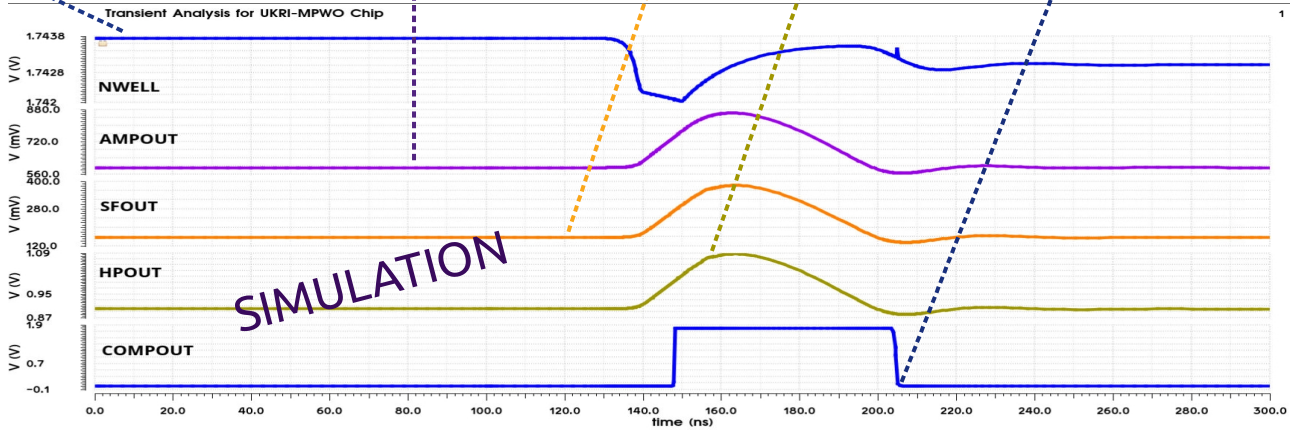
ELT based Pixel Schematic for Active Matrix



Sensing Diode

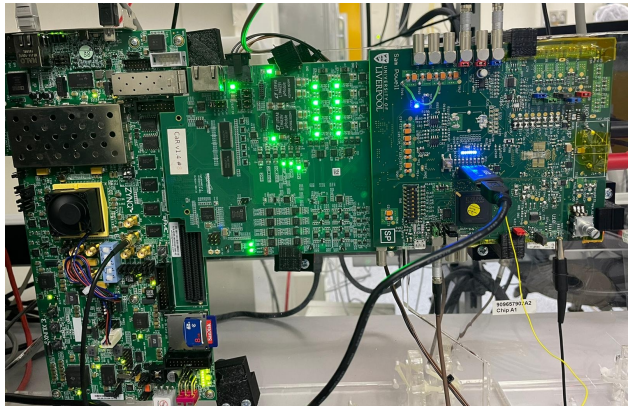


Read-out Electronics

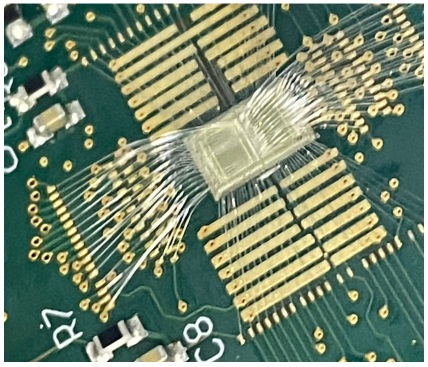


Each pixel has sensing diode and read-out-electronics. Read-out-electronics contains a charge sensing amplifier (CSA), source-follower, HP filter and a comparator.

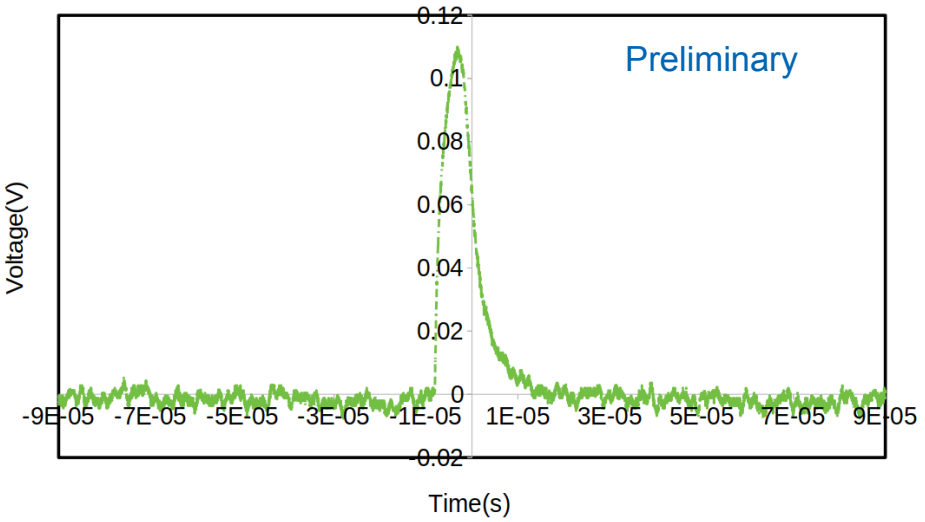
ELT based Pixel Schematic in UKRI-MPW0



DAQ based on Caribou
for UKRI-MPW0
(by Sam Powel)

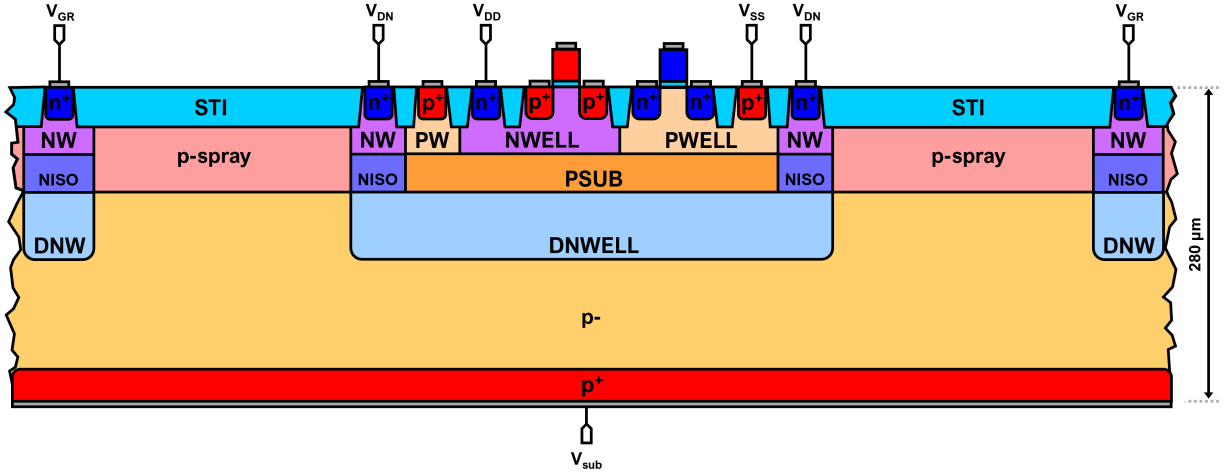


Bonded Chip



Measured SFOUT from ^{90}Sr source
at V_{bias}=450V(Single Shot)

Future Developments



- For using floating p-stop, TCAD simulations show that this still causes regions of high electric field to form (high enough for avalanche multiplication and therefore breakdown to occur) near biased n-type wells (e.g. pixels, guard ring NWELL...) which we think limits the maximum achievable breakdown voltage.

- Therefore, We would now possibly like to look into p-spray which is not available from the foundry we use at the moment.

Main Achievements & Future Works

Main Achievements:

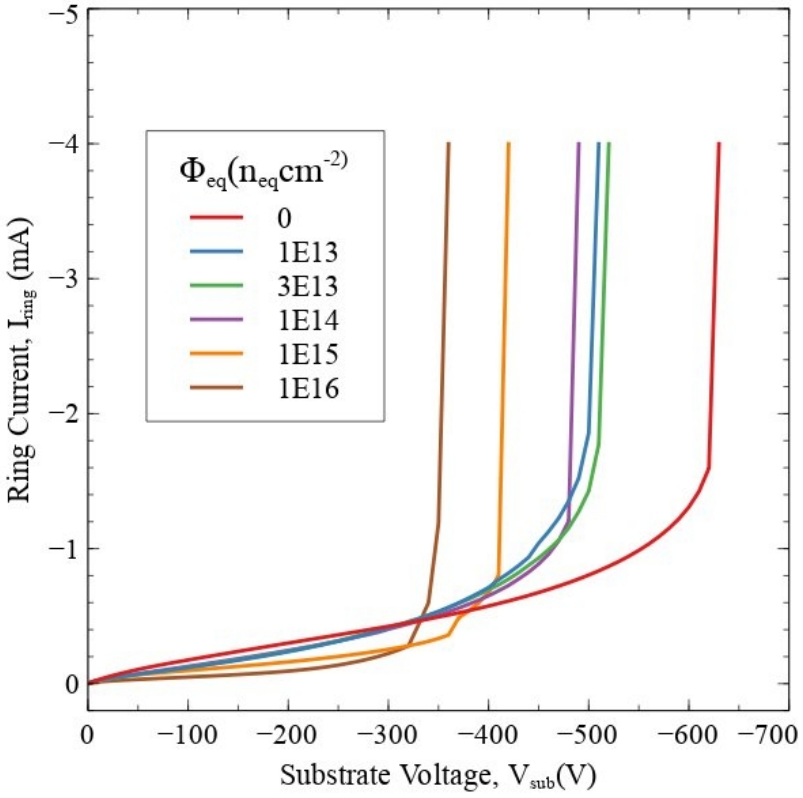
- Proof of concept HV-CMOS sensor with a very high breakdown voltage has been shown.
- Matrix reacts to ^{90}Sr source in the case of ELT based pixels.

Future Work:

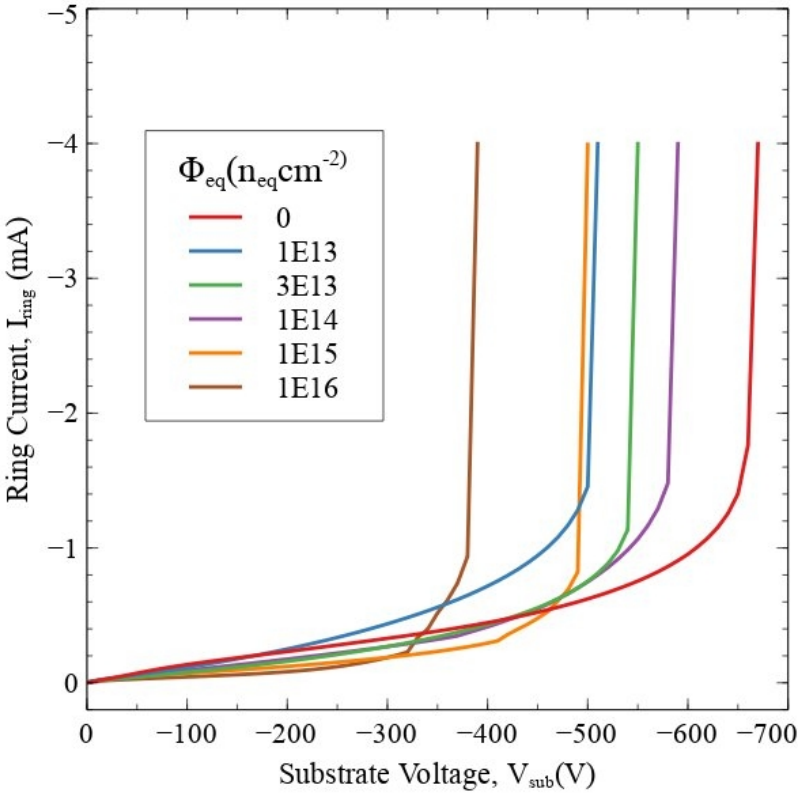
- Examining the source of positive leakage in test structure I-V measurements.
- Edge-TCT measurement is ongoing.
- Conducting TID irradiation and post-irradiation measurements on the ELT teststructures.
- Measuring the other signals (COMPOUT, HITMAP, ToT) of the ELT based active matrix. Both at unirradiated and post-irradiated stages.

Thank You

Backup Slide



Backside processed using plasma immersion ion implantation with laser annealing



Backside processed using beamline implantation with rapid thermal annealing